

NTLJS2103P

Power MOSFET

-12 V, -7.7 A, μ Cool™ Single P-Channel, 2x2 mm, WDFN Package

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88 Package
- Lowest $R_{DS(on)}$ Solution in 2x2 mm Package
- 1.2 V $R_{DS(on)}$ Rating for Operation at Low Voltage Logic Level Gate Drive
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- High Side Load Switch
- DC-DC Converters (Buck and Boost Circuits)
- Optimized for Battery and Load Management Applications in Portable Equipment
- Li-Ion Battery Linear Mode Charging

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	-12	V
Gate-to-Source Voltage		V_{GS}	± 8.0	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-5.9	A
		$T_A = 85^\circ\text{C}$	-4.2	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	-7.7	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.9	W
		$t \leq 5 \text{ s}$	3.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	-3.5	A
		$T_A = 85^\circ\text{C}$	-2.5	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	0.7	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-24	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode) (Note 2)		I_S	-2.7	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

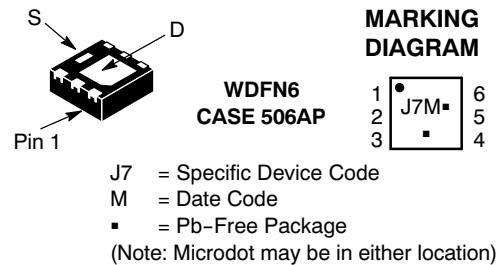
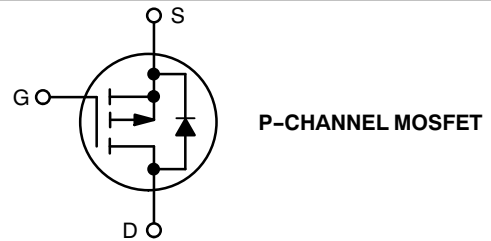
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size, (30 mm², 2 oz Cu).



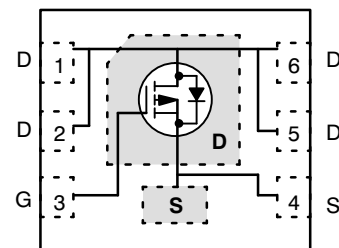
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<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX (Note 1)
-12 V	25 m Ω @ -4.5 V	-5.9 A
	35 m Ω @ -2.5 V	-5.3 A
	45 m Ω @ -1.8 V	-2.0 A
	60 m Ω @ -1.5 V	-1.0 A
	95 m Ω @ -1.2 V	-0.2 A



PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NTLJS2103PTAG	WDFN6 (Pb-Free)	3000/Tape & Reel
NTLJS2103PTBG	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	65	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	38	
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	180	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-12			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$, Ref to 25°C		-8.0		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$			-1.0	μA
					-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			± 0.1	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.3		-0.8	V
Negative Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.6		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -5.9\text{ A}$		25	40	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$		25	40	
		$V_{GS} = -2.5\text{ V}, I_D = -5.3\text{ A}$		35	50	
		$V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$		35	50	
		$V_{GS} = -1.8\text{ V}, I_D = -2.0\text{ A}$		45	75	
		$V_{GS} = -1.5\text{ V}, I_D = -1.0\text{ A}$		60	100	
Forward Transconductance	g_{FS}	$V_{DS} = -6.0\text{ V}, I_D = -2.0\text{ A}$		8.8		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -6.0\text{ V}$		1157		pF
Output Capacitance	C_{OSS}			290		
Reverse Transfer Capacitance	C_{RSS}			171		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -9.6\text{ V}, I_D = -5.9\text{ A}$		12.8	15	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.4		
Gate-to-Source Charge	Q_{GS}			1.6		
Gate-to-Drain Charge	Q_{GD}			3.6		
Gate Resistance	R_G			15.7		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -8.0\text{ V}, I_D = -5.9\text{ A}, R_G = 2.0\ \Omega$		8.0		ns
Rise Time	t_r			27		
Turn-Off Delay Time	$t_{d(OFF)}$			74		
Fall Time	t_f			88		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$	0.62	1.0	V
			$T_J = 85^\circ\text{C}$	0.56		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -1.0\text{ A}$		60	85	ns
Charge Time	t_a			21		
Discharge Time	t_b			39		
Reverse Recovery Time	Q_{RR}			50		

5. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

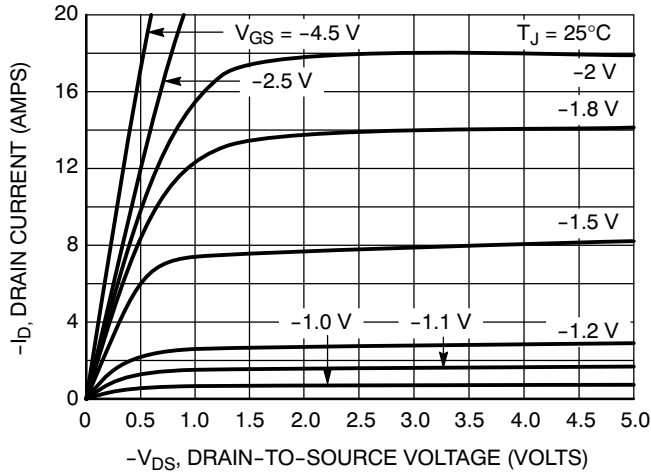


Figure 1. On-Region Characteristics

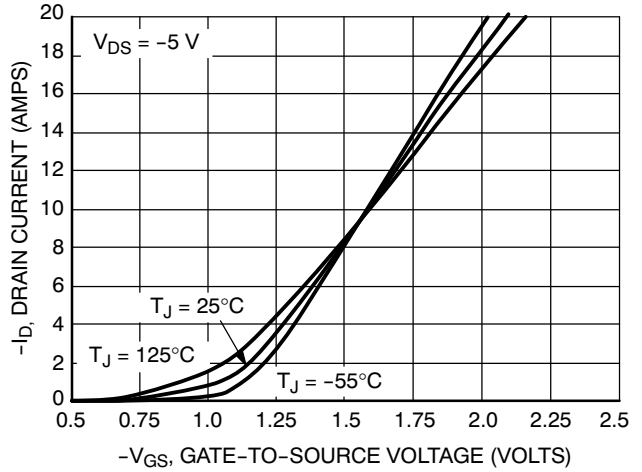


Figure 2. Transfer Characteristics

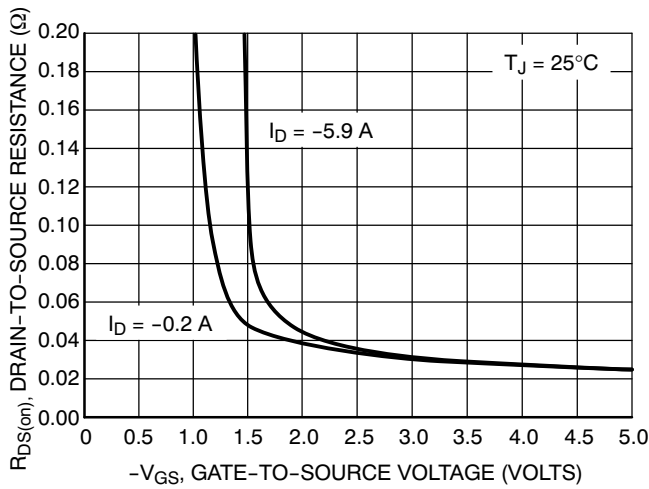


Figure 3. On-Resistance vs. Gate-to-Source Voltage

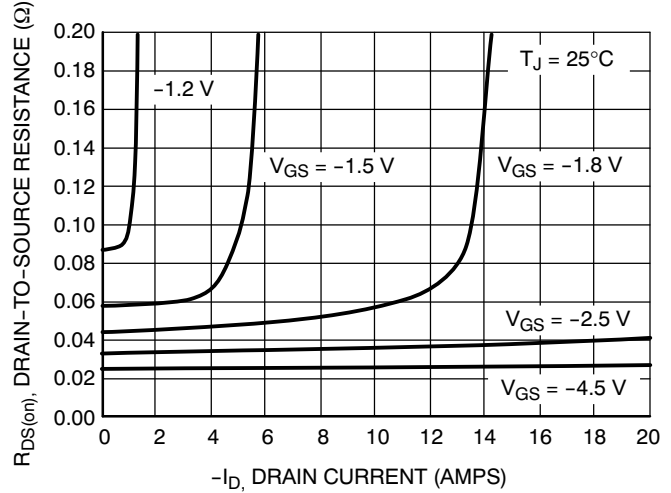


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

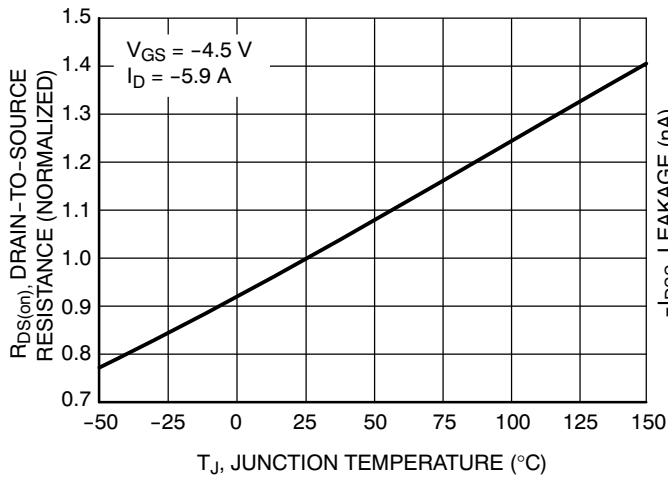


Figure 5. On-Resistance Variation with Temperature

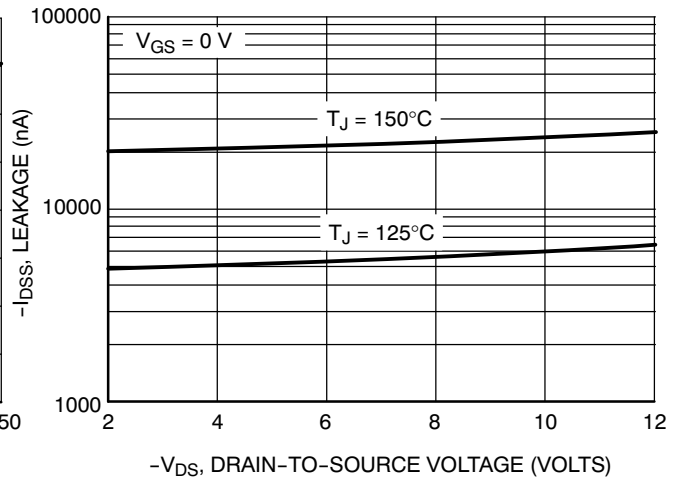


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

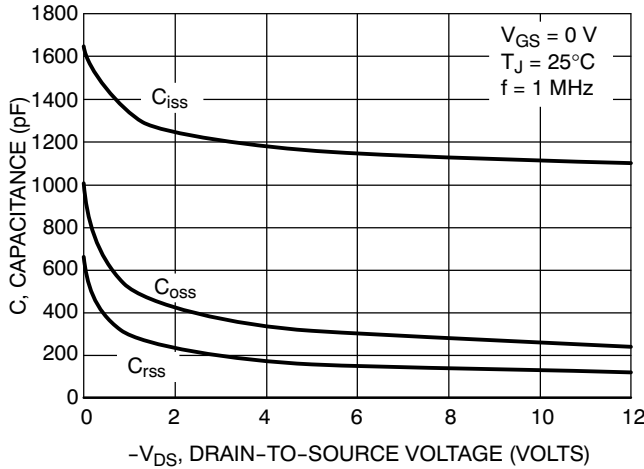


Figure 7. Capacitance Variation

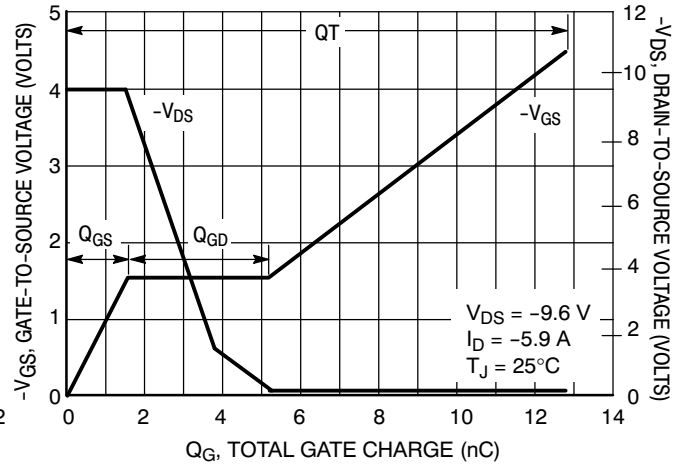


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

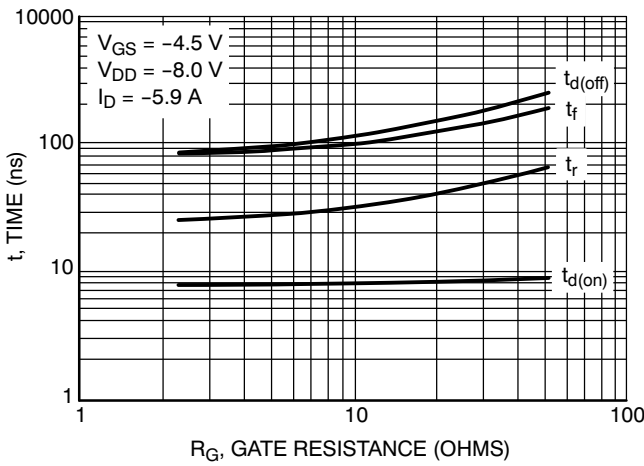


Figure 9. Resistive Switching Time Variation versus Gate Resistance

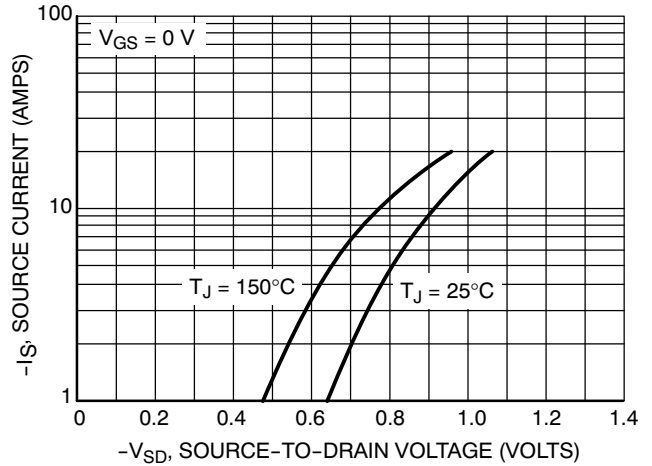


Figure 10. Diode Forward Voltage vs. Current

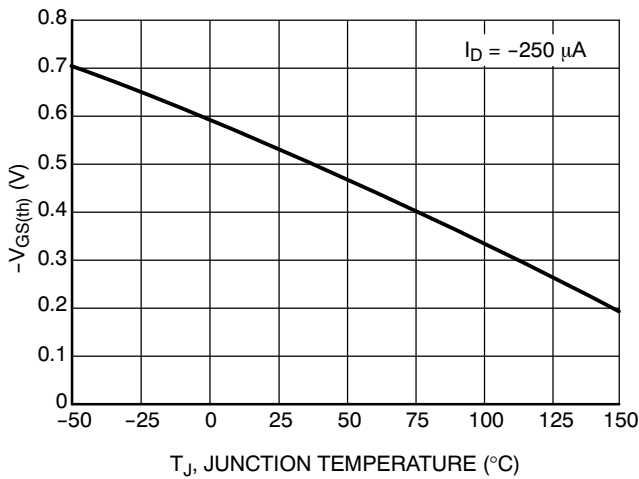


Figure 11. Threshold Voltage

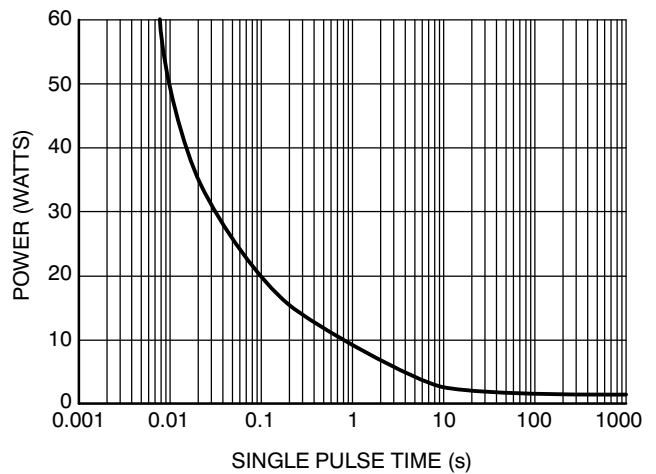


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

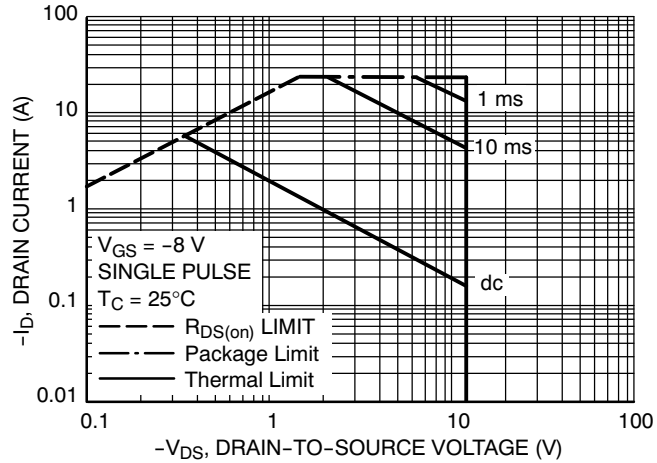


Figure 13. Maximum Rated Forward Biased Safe Operating Area

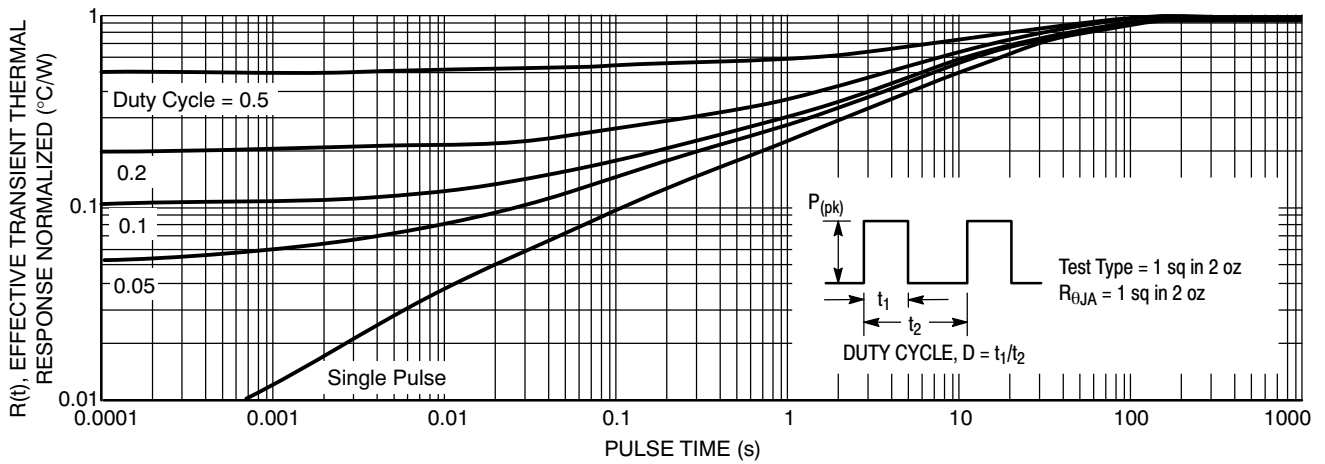
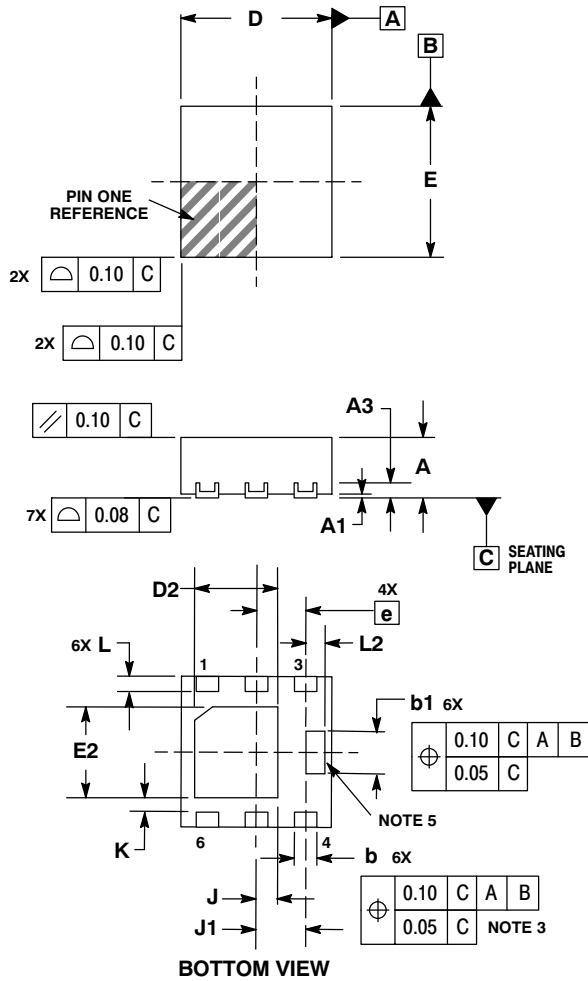


Figure 14. FET Thermal Response

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PACKAGE DIMENSIONS

WDFN6 2x2
CASE 506AP-01
ISSUE B



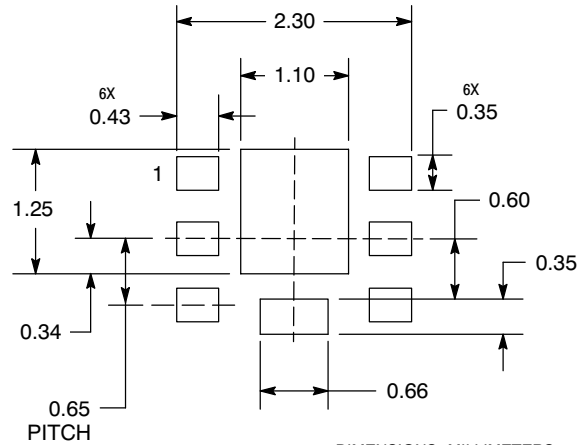
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

- STYLE 1:**
1. DRAIN
 2. DRAIN
 3. GATE
 4. SOURCE
 5. DRAIN
 6. DRAIN

SOLDERMASK DEFINED MOUNTING FOOTPRINT



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