

# NTMS4800N

## Power MOSFET 30 V, 8 A, N-Channel, SOIC-8

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- SOIC-8 Surface Mount Package Saves Board Space
- This is a Pb-Free Device

### Applications

- DC-DC Converters
- Printers

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	6.4	A
		$T_A = 70^\circ\text{C}$	5.1	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	1.29	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	4.9	A
		$T_A = 70^\circ\text{C}$	3.9	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	0.75	W
Continuous Drain Current $R_{\theta JA}$ , $t < 10$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	8.0	A
		$T_A = 70^\circ\text{C}$	6.4	
Power Dissipation $R_{\theta JA}$ , $t < 10$ s (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	2.0	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$	$I_{DM}$	32	A
Operating Junction and Storage Temperature	$T_J$ , $T_{stg}$	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	2.0	A	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 11$ A <sub>pk</sub> , $L = 1.0$ mH, $R_G = 25 \Omega$ )	$E_{AS}$	60.5	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for $t = 10$ s)	$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	97	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t < 10$ s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Foot (Drain)	$R_{\theta JF}$	25	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	167	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad, 1 oz Cu
2. Surface-mounted on FR4 board using the minimum recommended pad size

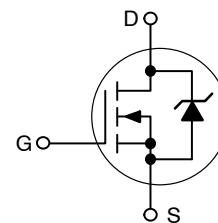


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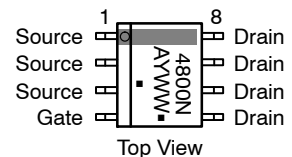
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
30 V	20 m $\Omega$ @ 10 V	8 A
	27 m $\Omega$ @ 4.5 V	

### N-Channel



SO-8  
CASE 751  
STYLE 12

### MARKING DIAGRAM/ PIN ASSIGNMENT



4800N = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4800NR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMS4800N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			26		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$		12.5	20	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$		20	27	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 7.5\text{ A}$		21		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		940		pF
Output Capacitance	$C_{oss}$			225		
Reverse Transfer Capacitance	$C_{rss}$			125		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 7.5\text{ A}$		7.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	$Q_{GS}$			3.3		
Gate-to-Drain Charge	$Q_{GD}$			3.2		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 7.5\text{ A}$		15.2		nC

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 6.0\ \Omega$		9.4		ns
Rise Time	$t_r$			4.0		
Turn-Off Delay Time	$t_{d(off)}$			21		
Fall Time	$t_f$			6.5		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.0	V
			$T_J = 125^\circ\text{C}$		0.59		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 2.0\text{ A}$		17.8		ns	
Charge Time	$t_a$			8.3			
Discharge Time	$t_b$			9.5			
Reverse Recovery Charge	$Q_{RR}$			8.0			nC

## PACKAGE PARASITIC VALUES

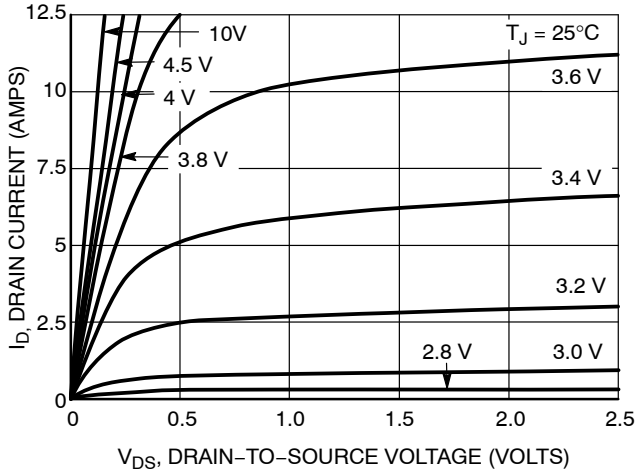
Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.66		nH
Drain Inductance	$L_D$			0.20		nH
Gate Inductance	$L_G$			1.5		nH
Gate Resistance	$R_G$			1.5	3.0	$\Omega$

3. Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .

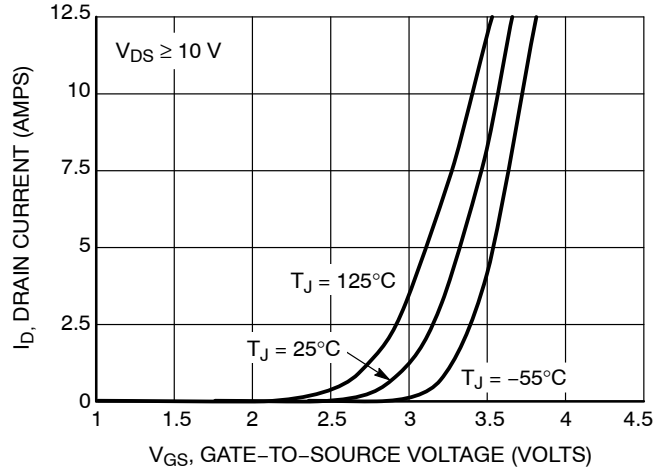
4. Switching characteristics are independent of operating junction temperatures.

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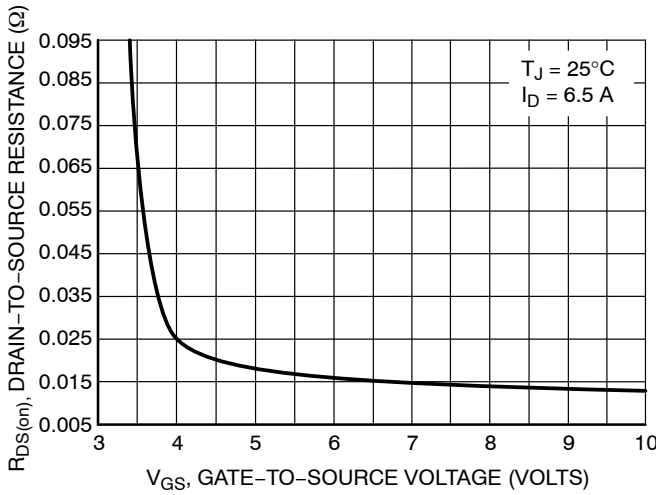
## TYPICAL PERFORMANCE CURVES



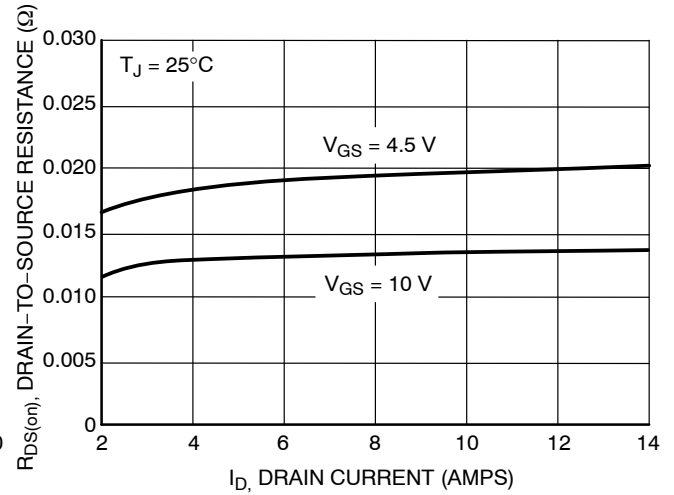
**Figure 1. On-Region Characteristics**



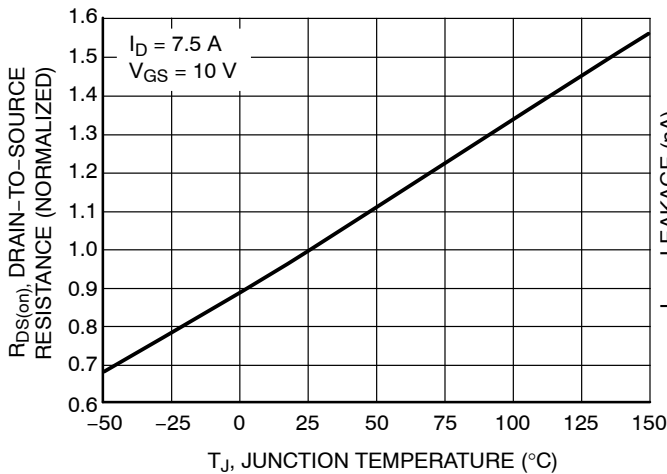
**Figure 2. Transfer Characteristics**



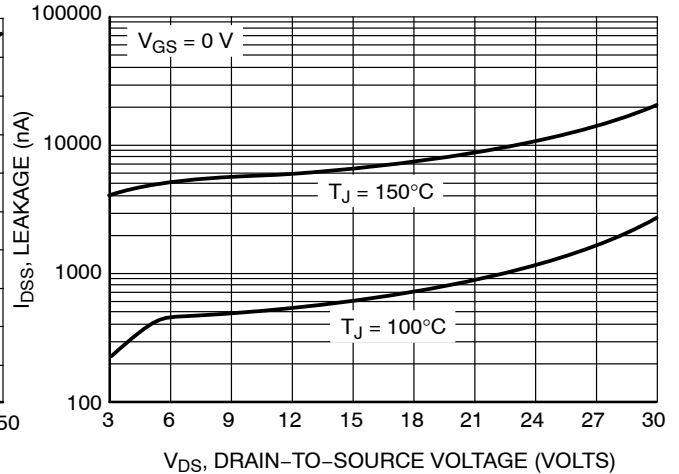
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

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## TYPICAL PERFORMANCE CURVES

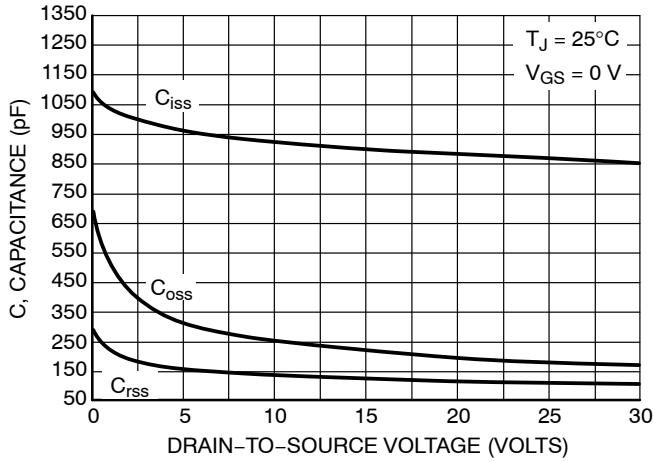


Figure 7. Capacitance Variation

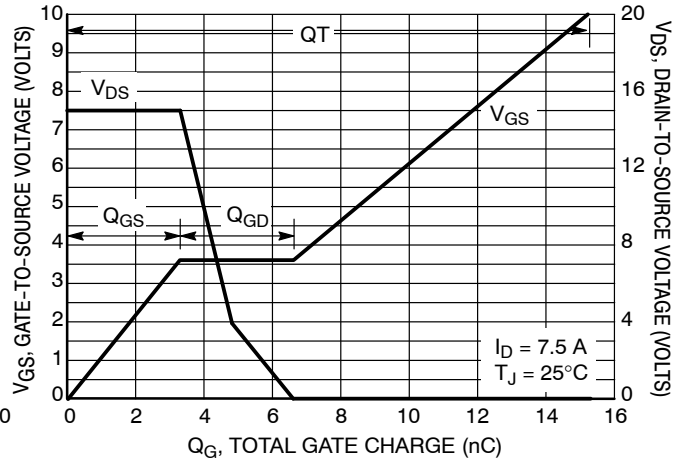


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

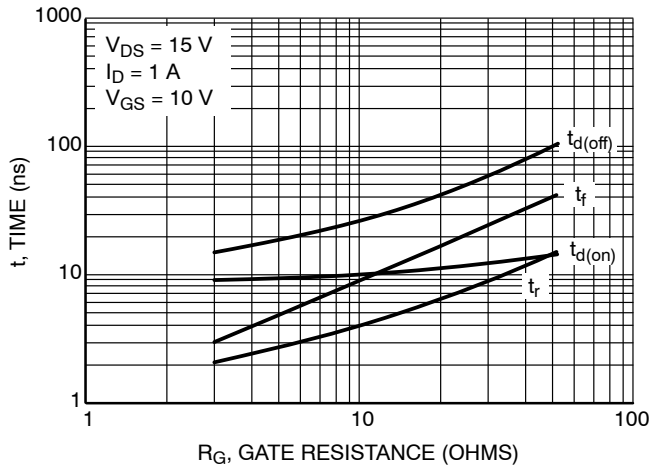


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

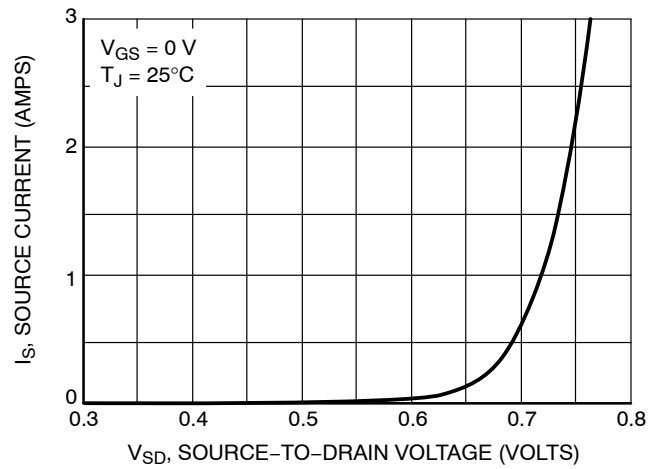


Figure 10. Diode Forward Voltage vs. Current

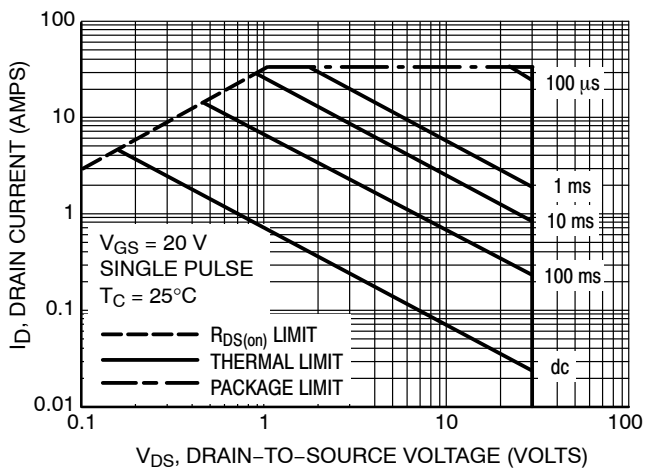


Figure 11. Maximum Rated Forward Biased Safe Operating Area

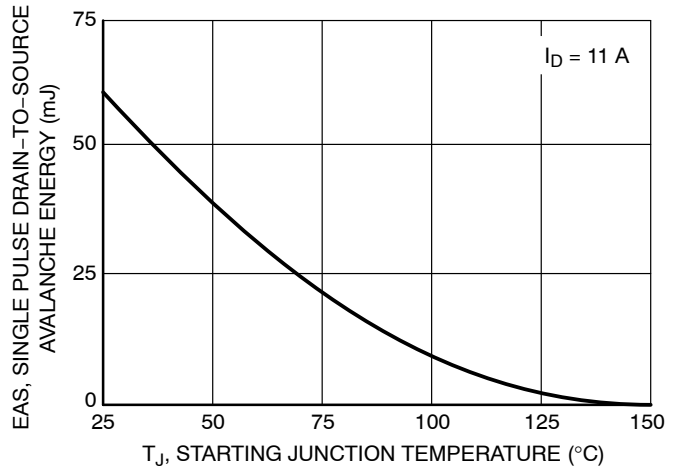
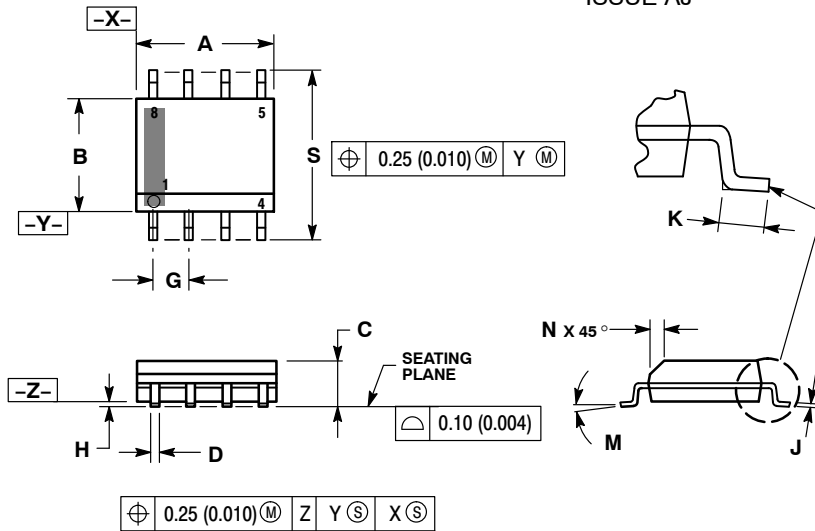


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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## PACKAGE DIMENSIONS

SOIC-8  
CASE 751-07  
ISSUE AJ

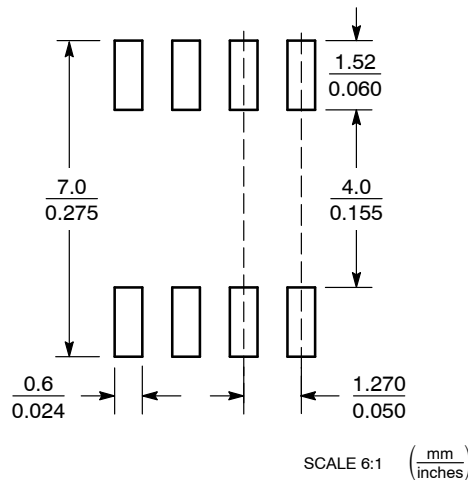


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



STYLE 12:

- PIN 1. SOURCE
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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