

NTTFS4823N

Power MOSFET

30 V, 50 A, Single N-Channel, μ 8FL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- This is a Pb-Free Device

Applications

- DC-DC Converters
- High Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	12.6	A
		$T_A = 85^\circ\text{C}$	9.1	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	2.1	W
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	I_D	$T_A = 25^\circ\text{C}$	17.5	A
		$T_A = 85^\circ\text{C}$	12.6	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	P_D	$T_A = 25^\circ\text{C}$	4.0	W
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	$T_C = 25^\circ\text{C}$	7.1	A
		$T_C = 85^\circ\text{C}$	5.1	
Power Dissipation $R_{\theta JC}$ (Note 2)	P_D	$T_C = 25^\circ\text{C}$	0.66	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	50	A
		$T_C = 85^\circ\text{C}$	36	
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	$T_C = 25^\circ\text{C}$	32.9	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	150	A
Current Limited by Pkg.	$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	90	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	33	A	
Drain to Source DV/DT	dV/dt	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 25$ A _{pk} , $L = 0.1$ mH, $R_G = 25 \Omega$)	E_{AS}	31	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

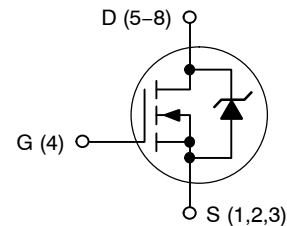


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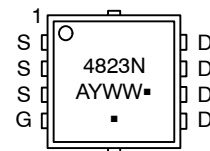
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	10.5 m Ω @ 10 V	50 A
	17.5 m Ω @ 4.5 V	

N-Channel MOSFET



MARKING DIAGRAM



4823N = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS4823NTAG	WDFN8 (Pb-Free)	1500/Tape & Reel
NTTFS4823NTWG	WDFN8 (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.8	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	59.4	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	190.2	
Junction-to-Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	31.1	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
 4. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5	1.9	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V to } 11.5\text{ V}$	$I_D = 20\text{ A}$		8.1	10.5	m Ω
			$I_D = 10\text{ A}$		8.0		
		$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$		13.5	17.5	
			$I_D = 10\text{ A}$		13		
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 20\text{ A}$		34		S	

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		750		pF
Output Capacitance	C_{oss}			175		
Reverse Transfer Capacitance	C_{rss}			100		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		6.5	9.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.8		
Gate-to-Source Charge	Q_{GS}			2.5		
Gate-to-Drain Charge	Q_{GD}			2.9		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		15		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		12		ns
Rise Time	t_r			22		
Turn-Off Delay Time	$t_{d(off)}$			14		
Fall Time	t_f			4		

5. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0		ns
Rise Time	t_r			18		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			2.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 20\text{ A}$	$T_J = 25^\circ\text{C}$		0.93	1.1	V
			$T_J = 125^\circ\text{C}$		0.83		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V},$ $dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 20\text{ A}$			13		ns
Charge Time	t_a				7.5		
Discharge Time	t_b				5.5		
Reverse Recovery Charge	Q_{RR}				4.0		

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.38		nH
Drain Inductance	L_D			0.054		
Gate Inductance	L_G			1.3		
Gate Resistance	R_G			0.65	2.0	

5. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

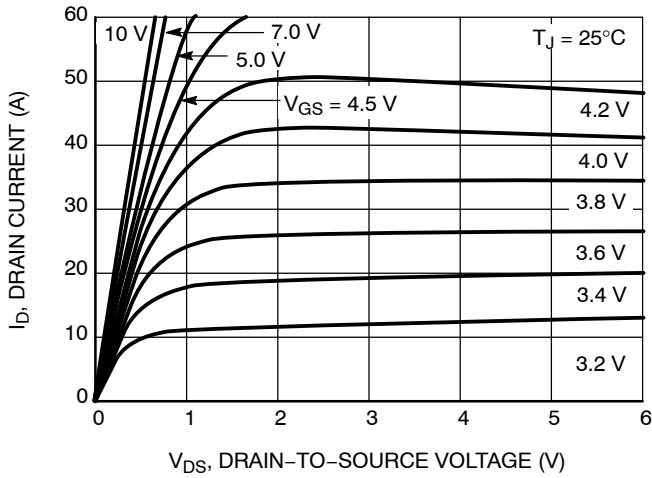


Figure 1. On-Region Characteristics

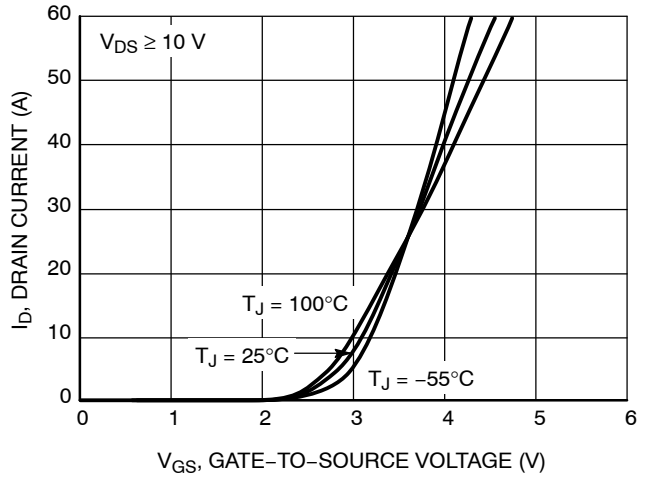


Figure 2. Transfer Characteristics

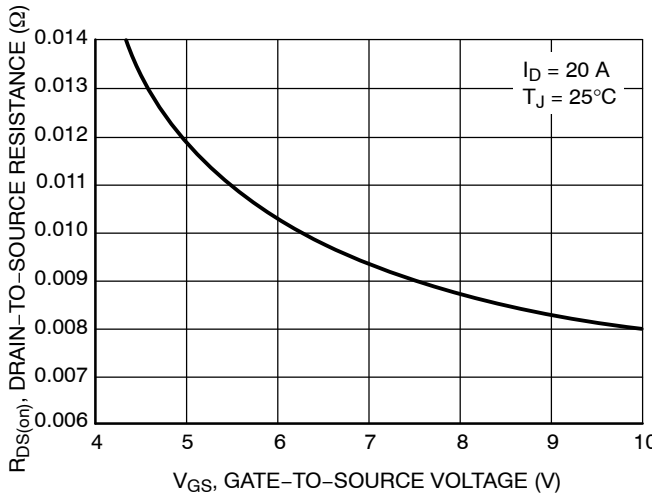


Figure 3. On-Resistance vs. Gate-to-Source Voltage

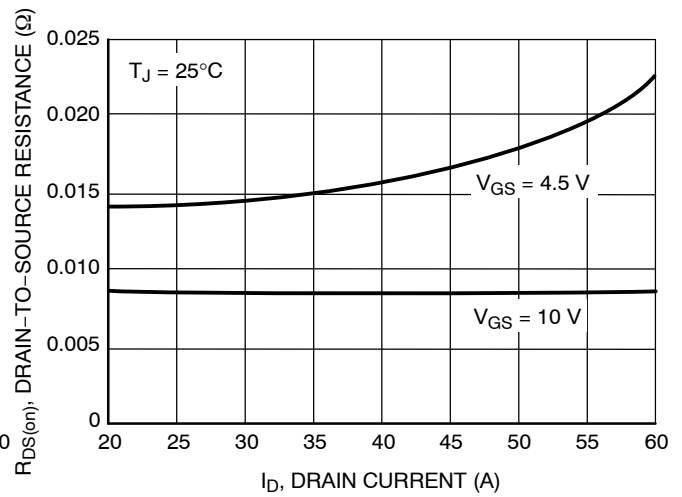


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

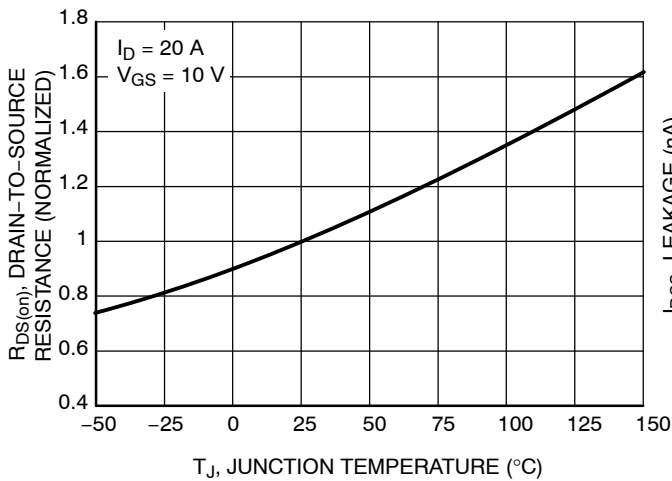


Figure 5. On-Resistance Variation with Temperature

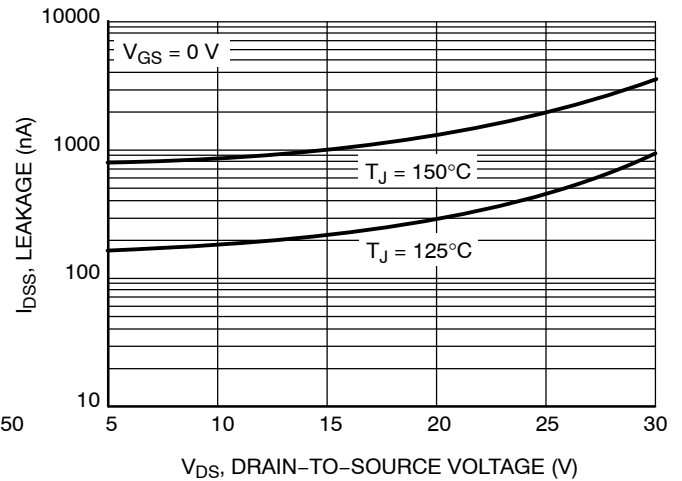


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

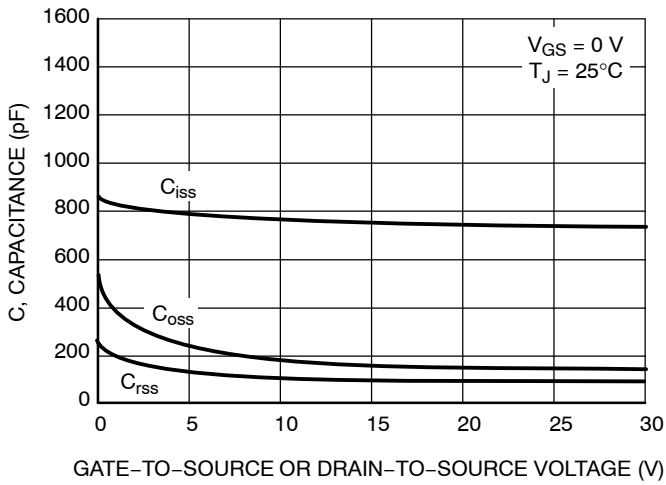


Figure 7. Capacitance Variation

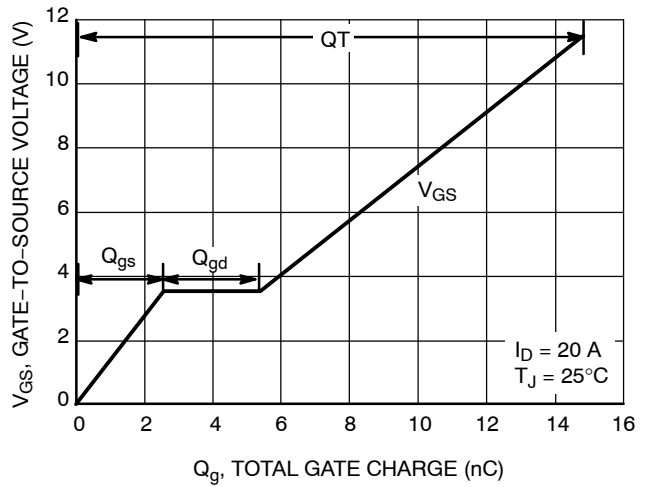


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

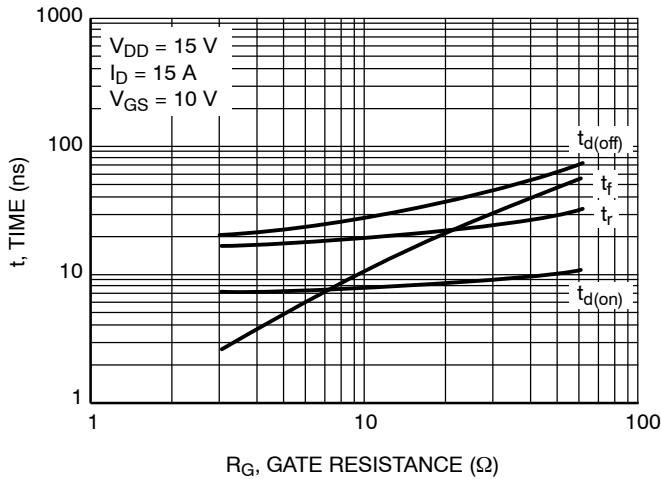


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

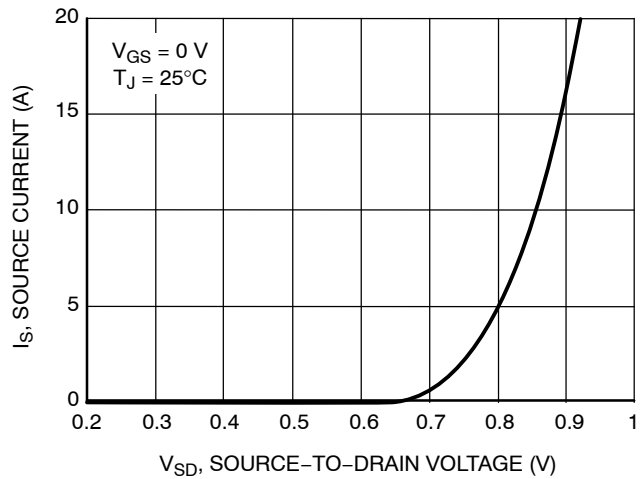


Figure 10. Diode Forward Voltage vs. Current

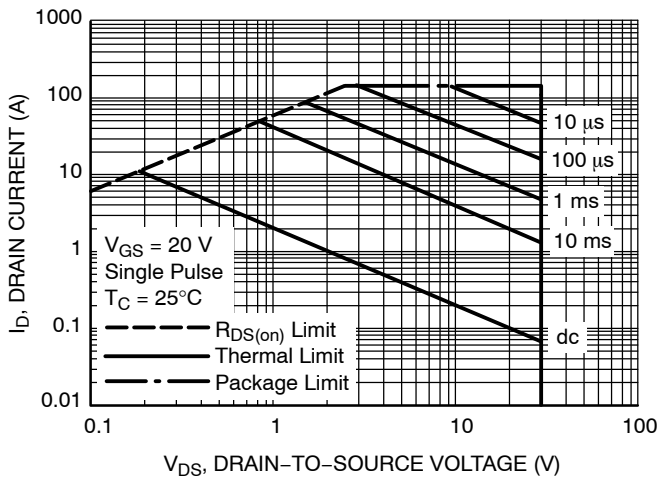


Figure 11. Maximum Rated Forward Biased Safe Operating Area

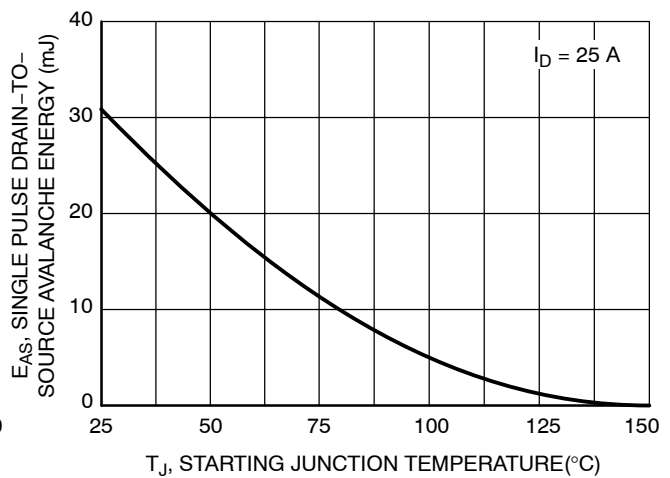
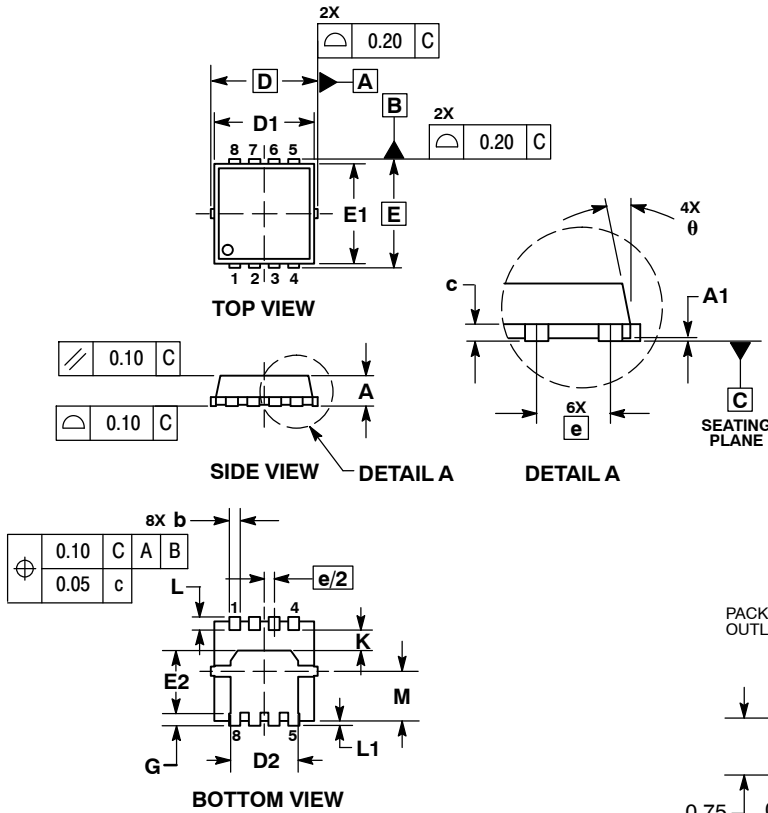


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P
CASE 511AB-01
ISSUE B

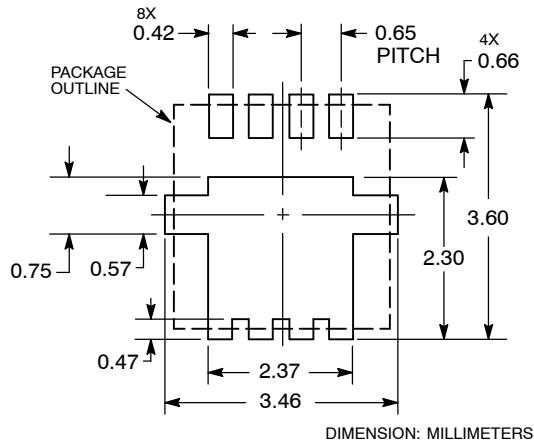


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.64	---	---	0.025	---	---
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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