Preliminary

256K X 36 Bit Synchronous High Speed SRAM with Burst Counter and Flow-through Data Output

Document Title

256K X 36 Bit Synchronous High Speed SRAM with Burst Counter and Flow-through Data Output

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	July 13, 2005	Preliminary

A63P83361

Preliminary

256K X 36 Bit Synchronous High Speed SRAM with Burst Counter and Flow-through Data Output

Features

- Fast access times: 6.5/7.5/8.0 ns(153/133/117 MHz)
- Single 2.5V±5% power supply
- Synchronous burst function
- Individual Byte Write control and Global Write
- Three separate chip enables allow wide range of options for CE control, address pipelining
- Selectable BURST mode
- SLEEP mode (ZZ pin) provided
- Available in 100-pin LQFP package
- Industrial operating temperature range: -45°C to +125°C for -I series

General Description

The A63P83361 is a high-speed SRAM containing 9M bits of bit synchronous memory, organized as 256K words by 36 bits.

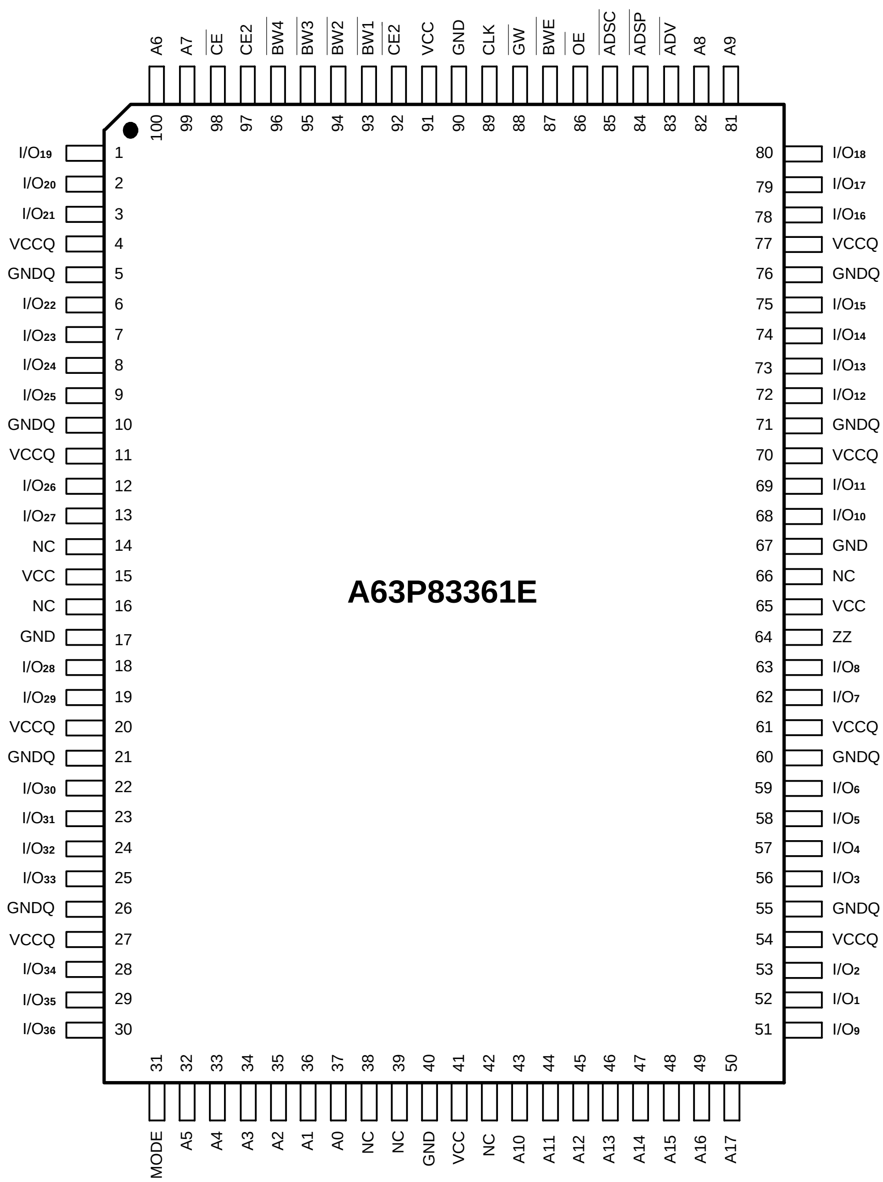
The A63P83361 combines advanced synchronous peripheral circuitry, 2-bit burst control, input registers, output buffer and a 256K X 36 SRAM core to provide a wide range of data RAM applications.

The positive edge triggered single clock input (CLK) controls all synchronous inputs passing through the registers. Synchronous inputs include all addresses (A0 - A17), all data inputs (I/O$_{1}$ - I/O$_{36}$), active LOW chip enable ($\overline{CE}$), two additional chip enables (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$), byte write enables ($\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and Global Write ($\overline{GW}$). Asynchronous inputs include output enable ($\overline{OE}$), clock (CLK), BURST mode (MODE) and SLEEP mode (ZZ).

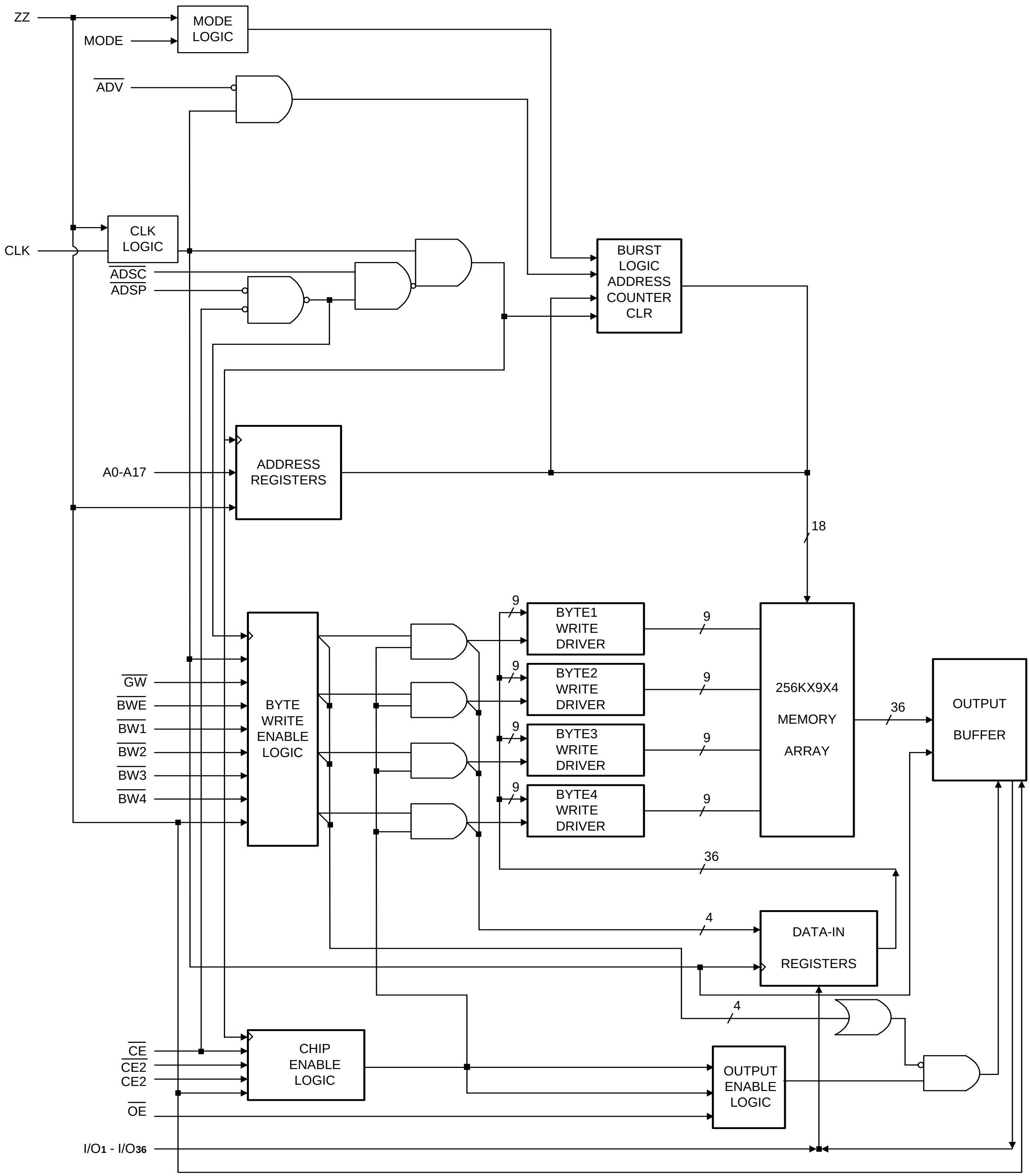
Burst operations can be initiated with either the address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pin. Subsequent burst sequence burst addresses can be internally generated by the A63P83361 and controlled by the burst advance ($\overline{ADV}$) pin. Write cycles are internally self-timed and synchronous with the rising edge of the clock (CLK).

This feature simplifies the write interface. Individual Byte enables allow individual bytes to be written. $\overline{BW1}$ controls I/O$_{1}$ - I/O$_{9}$, $\overline{BW2}$ controls I/O$_{10}$ - I/O$_{18}$, $\overline{BW3}$ controls I/O$_{19}$ - I/O$_{27}$, and $\overline{BW4}$ controls I/O$_{28}$ - I/O$_{36}$, all on the condition that $\overline{BWE}$ is LOW. $\overline{GW}$ LOW causes all bytes to be written.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	Description
32 – 37, 43 - 50, 81, 82, 99, 100	A0 - A17	Address Inputs
89	CLK	Clock
87, 93 - 96	$\overline{\text{BWE}}$, $\overline{\text{BW1}}$ - $\overline{\text{BW4}}$	Byte Write Enables
88	$\overline{\text{GW}}$	Global Write
86	$\overline{\text{OE}}$	Output Enable
92, 97, 98	$\overline{\text{CE2}}$,CE2, $\overline{\text{CE}}$	Chip Enables
83	$\overline{\text{ADV}}$	Burst Address Advance
84	$\overline{\text{ADSP}}$	Processor Address Status
85	$\overline{\text{ADSC}}$	Controller Address Status
31	MODE	Burst Mode: HIGH or NC (Interleaved burst) LOW (Linear burst)
64	ZZ	Asynchronous Power-Down (Snooze): HIGH (Sleep) LOW or NC (Wake up)
1,2, 3, 6 - 9, 12, 13, 18, 19, 22 - 25, 28, 29,30,51, 52, 53, 56 - 59, 62, 63, 68, 69, 72 - 75, 78, 79,80	I/O_1- I/O_{36}	Data Inputs/Outputs
1, 14, 16, 30, 38, 39, 42, 43, 51, 66, 80	NC	No Connection
15, 41, 65, 91	VCC	Power Supply
17, 40, 67, 90	GND	Ground
4, 11, 20, 27, 54, 61, 70, 77	VCCQ	Isolated Output Buffer Supply
5, 10, 21, 26, 55, 60, 71, 76	GNDQ	Isolated Output Buffer Ground

Synchronous Truth Table (See Notes 1 Through 5)

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	I/O Operation
Deselected Cycle, Power-down	NONE	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Dout
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	Din
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Dout
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Dout
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Dout
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	Din
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	Din
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Dout
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Dout
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	Din
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	Din

Notes: 1. X = "Disregard", H = Logic High, L = Logic Low.

2. $\overline{\text{WRITE}}$ = L means:

   1) Any $\overline{\text{BWx}}$ ($\overline{\text{BW1}}$, $\overline{\text{BW2}}$, $\overline{\text{BW3}}$, or $\overline{\text{BW4}}$) and $\overline{\text{BWE}}$ are low or

   2) $\overline{\text{GW}}$ is low.

3. All inputs except $\overline{\text{OE}}$ must be synchronized with setup and hold times around the rising edge (L-H) of CLK.

4. For write cycles that follow read cycles, $\overline{\text{OE}}$ must be HIGH before the input data request setup time and held HIGH throughout the input data hold time.

5. $\overline{\text{ADSP}}$ LOW always initiates an internal Read at the L-H edge of CLK. A Write is performed by setting one or more byte write enable signals and $\overline{\text{BWE}}$ LOW or $\overline{\text{GW}}$ LOW for the subsequent L-H edge of CLK. Refer to the Write timing diagram for clarification.

Write Truth Table

Operation	$\overline{\text{GW}}$	$\overline{\text{BWE}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	$\overline{\text{BW4}}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Linear Burst Address Table (MODE = LOW)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

Interleaved Burst Address Table (MODE = HIGH or NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

Absolute Maximum Ratings*

Power Supply Voltage (VCC) . . . . -0.5V to +3.6V
Voltage Relative to GND for any Pin Except VCC (Vin, Vout) . . . . -0.5V to VCC +0.5V
Power Dissipation (P_D) 2W
Storage Temperature (Tbias) . . . . -65°C to 150 °C
Storage Temperature (Tstg) . . . . -55°C to 125°C

Operating Ranges

Ambient Temperature

Commercial (C) Devices . . . . 0°C to +70°C
Industrial (I) Devices . . . . -45°C to +125°C

V_{CC} & V_{CCQ} Supply Voltages

V_{CC} for all devices . . .. +2.5V
V_{CCQ} for all devices . . .. +2.5V
Operating ranges define those limits between which the functionally of the device is guaranteed.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(0°C ≤ T_A ≤ 70°C, VCC, VCCQ = 2.5V+5% or 2.5V-5%, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VCC	Supply Voltage (Operating Voltage Range)	2.375	2.5	2.625	V	
VCCQ	Isolated Input Buffer Supply	2.375	2.5	2.625	V	
GND	Supply Voltage to GND	0.0	-	0.0	V	
V_{IH}	Input High Voltage	1.7	-	VCC+0.3	V	1, 2
V_{IHQ}	Input High Voltage (I/O Pins)	1.7	-	VCC+0.3	V	
V_{IL}	Input Low Voltage	-0.3	-	0.7	V	1, 2

DC Electrical Characteristics

(0°C ≤ T_A ≤ 70°C, VCC, VCCQ = 2.5V+5% or 2.5V-5%, unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions	Note
$\lvert I_{LI} \rvert$	Input Leakage Current	-	±2.0	μA	All inputs V_{IN} = GND to VCC	
$\lvert I_{LO} \rvert$	Output Leakage Current	-	±2.0	μA	$\overline{OE}$ = V_{IH}, Vout = GND to VCC	
I_{CC1}	Supply Current	-	300	mA	Device selected; VCC = max. Iout = 0mA, all inputs = V_{IH} or V_{IL} Cycle time = t_{KC} min.	3, 11
I_{SB1}	Standby Current	-	180	mA	Device deselected; VCC = max. All inputs are fixed. All inputs ≥ VCC - 0.2V or ≤ GND + 0.2V Cycle time = t_{KC} min.	11
I_{SB2}		-	150	mA	ZZ ≥ VCC - 0.2V	
V_{OL}	Output Low Voltage	-	1.0	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	1.6	-	V	I_{OH} = -4 mA	

Capacitance

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	3	4	pF	T_A = 25 C; f = 1MHz VCC = 2.5V
$C_{I/O}$	Input/Output Capacitance	4	5	pF	

* These parameters are sampled and not 100% tested.

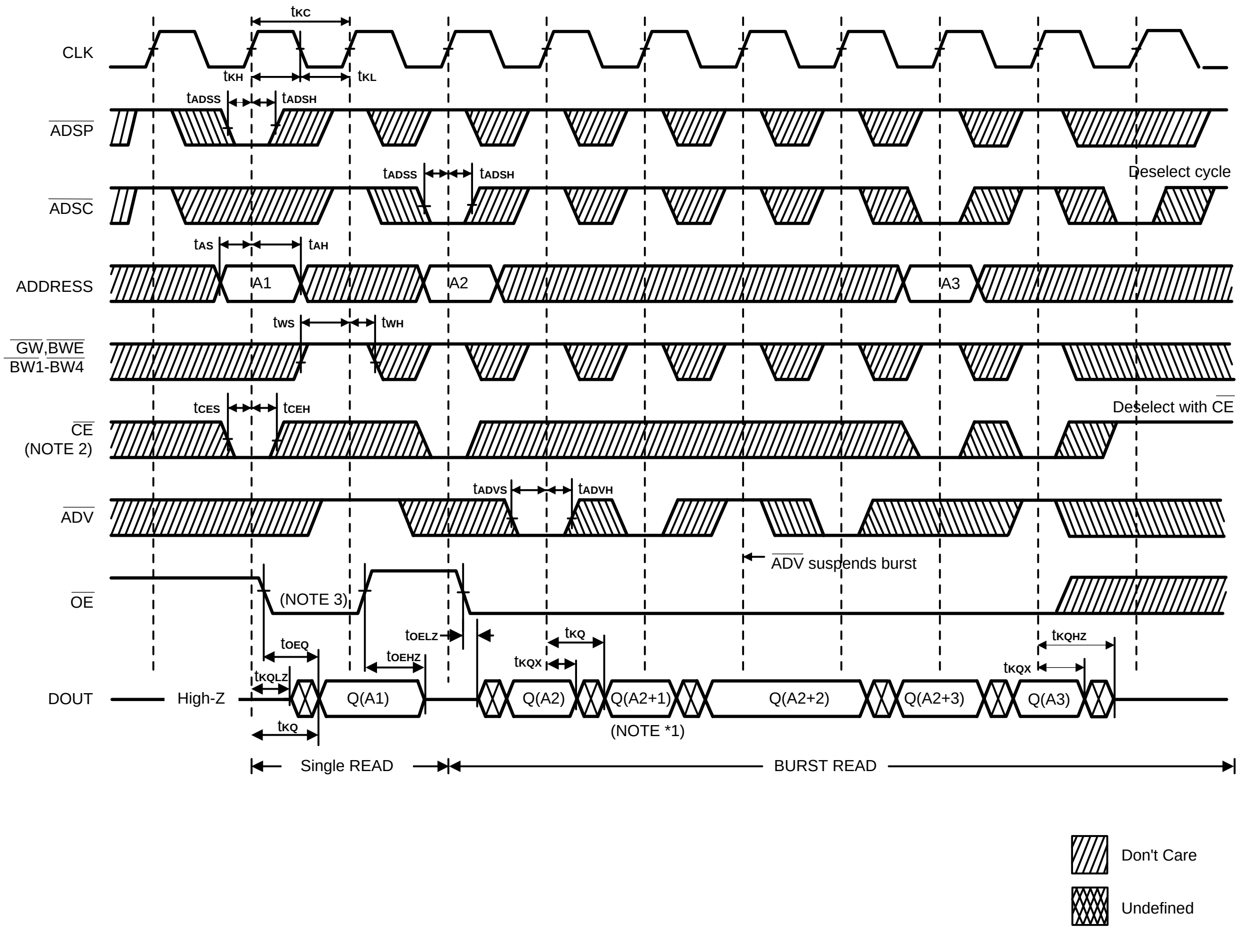
AC Characteristics (0°C ≤ T_A ≤ 70°C, VCC = 2.5V+5% or 2.5V-5%)

Symbol	Parameter	-6.5		-7.5		-8.5		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{KC}	Clock Cycle Time	7.5	-	8.5	-	10	-	ns	
T_{KH}	Clock High Time	2.5	-	2.8	-	3.0	-	ns	
T_{KL}	Clock Low Time	2.5	-	2.8	-	3.0	-	ns	
T_{KQ}	Clock to Output Valid	-	6.5	-	7.5	-	8.5	ns	
t_{KQX}	Clock to Output Invalid	3.0	-	3.0	-	3.0	-	ns	
t_{KQLZ}	Clock to Output in Low-Z	2.5	-	2.5	-	2.5	-	ns	5, 6
t_{KQHZ}	Clock to Output in High-Z	-	3.5	-	3.5	-	5.0	ns	5, 6
t_{OEQ}	$\overline{OE}$ to Output Valid	-	3.5	-	3.5	-	5.0	ns	8
t_{OELZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	5, 6
t_{OEHZ}	$\overline{OE}$ to Output in High-Z	-	3.5	-	3.5	-	5.0	ns	5, 6
Setup Times									
T_{AS}	Address	1.5	-	2.0	-	2.0	-	ns	7, 9
t_{ADSS}	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	1.5	-	2.0	-	2.0	-	ns	7, 9
t_{ADVS}	Address Advance ($\overline{ADV}$)	1.5	-	2.0	-	2.0	-	ns	7, 9
t_{WS}	Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	1.5	-	2.0	-	2.0	-	ns	7, 9
T_{DS}	Data-in	1.5	-	1.5	-	2.0	-	ns	7, 9
t_{CES}	Chip Enable ($\overline{CE}$, CE2, $\overline{CE2}$)	1.5	-	2.0	-	2.0	-	ns	7, 9
Hold Times									
T_{AH}	Address	0.5		0.5		0.5		ns	7, 9
t_{ADSH}	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	0.5		0.5		0.5		ns	7, 9
t_{AAH}	Address Advance ($\overline{ADV}$)	0.5		0.5		0.5		ns	7, 9
t_{WH}	Write Signal ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$,$\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	0.5		0.5		0.5		ns	7, 9
T_{DH}	Data-in	0.5		0.5		0.5		ns	7, 9
t_{CEH}	Chip Enable ($\overline{CE}$, CE2, $\overline{CE2}$)	0.5		0.5		0.5		ns	7, 9

Notes:

1. All voltages refer to GND.
2. Overshoot: $V_{IH} \le +2V$ for $t \le t_{KC}/2$.
   Undershoot: $V_{IL} \ge -0.7V$ for $t \le t_{KC}/2$.
   Power-up: $V_{IH} \le +2$ and $VCC \le 1.7V$
   for $t \le 200ms$
3. I_{CC1} is given with no output current. I_{CC1} increases with greater output loading and faster cycle times.
4. Test conditions assume the output loading shown in Figure 1, unless otherwise specified.
5. For output loading, $C_L = 5pF$, as shown in Figure 2. Transition is measured $\pm150mV$ from steady state voltage.
6. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{QELZ}.
7. A WRITE cycle is defined by at least one Byte Write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
8. $\overline{OE}$ has no effect when a Byte Write enable is sampled LOW.
9. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and the chip is enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW to remain enabled.
10. The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the given DC values. AC I/O curves are available upon request.
11. "Device Deselected" means device is in POWER-DOWN mode, as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
12. MODE pin has an internal pulled-up, and ZZ pin has an internal pulled-down. All of then exhibit an input leakage current of $10\mu A$.
13. Snooze (ZZ) input is recommended that users plan for four clock cycles to go into SLEEP mode and four clocks to emerge from SLEEP mode to ensure no data is lost.

Timing Waveforms



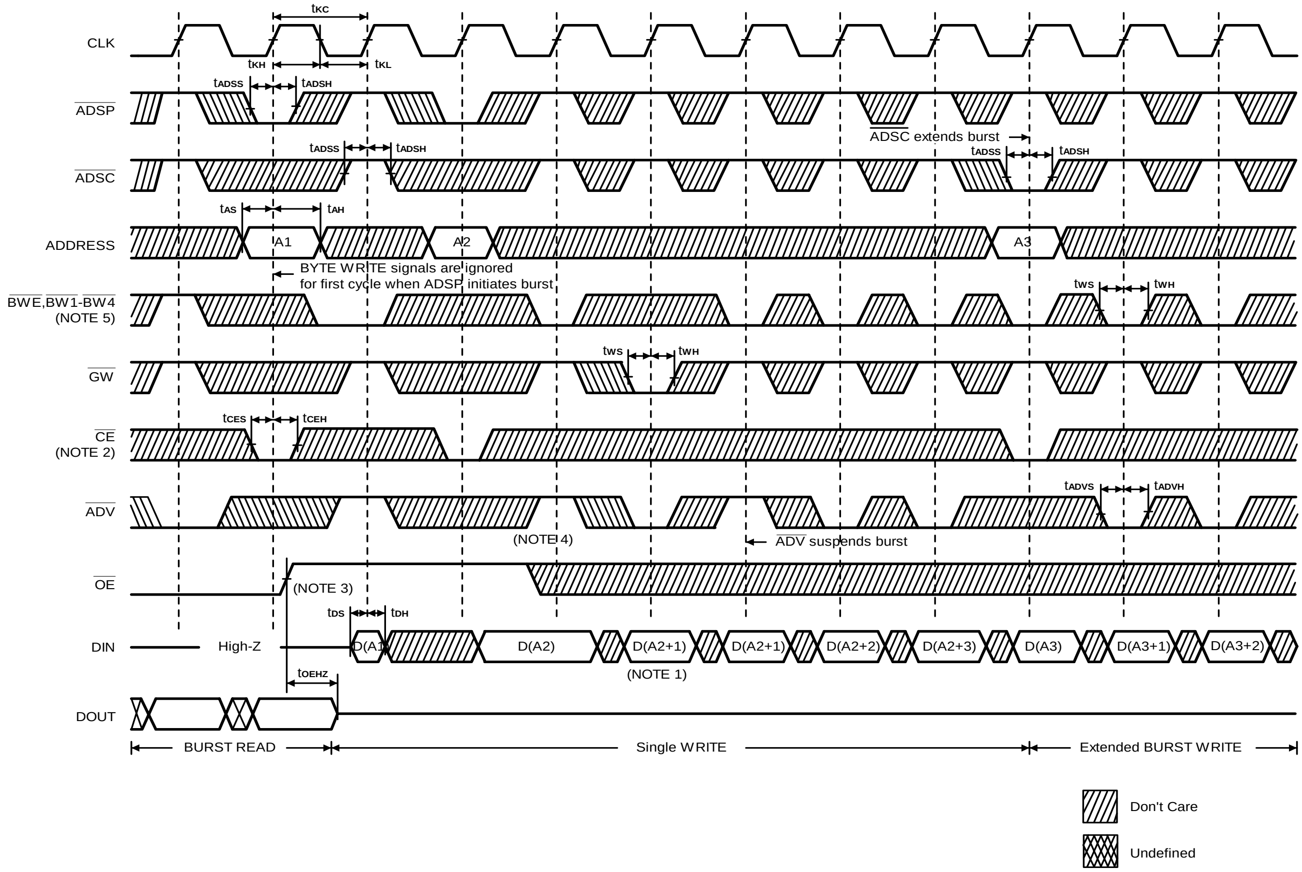
Read Timing

Notes: 1. QA(2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

2. $\overline{CE}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

Timing Waveforms (continued)

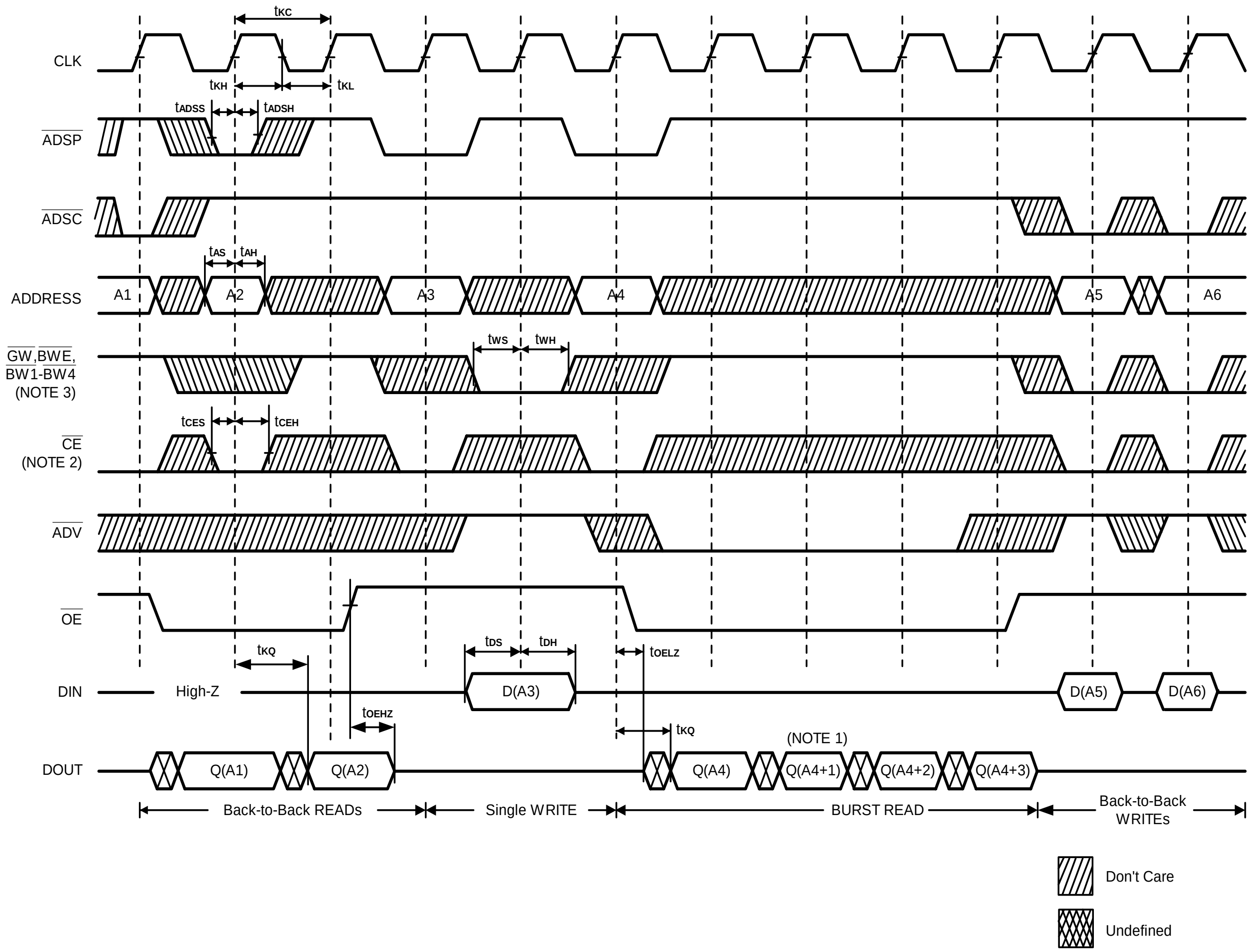


Write Timing

Notes: 1. D(A2) refers to output from address A2. D(A2+1) refers to output from the internal burst address immediately following A2.

2. Timing for $\overline{CE2}$ and CE2 is identical to that for $\overline{CE}$. As shown in the above diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup, and held HIGH throughout the data hold period. This prevents input/output data contention for the period prior to the time Byte Write enable inputs are sampled.
4. $\overline{ADV}$ must be HIGH to permit a Write to the loaded address.
5. Byte Write enables are decided by means of a Write truth table.

Timing Waveforms (continued)



Read/Write Timing

Notes: 1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}$ is LOW and CE2 is HIGH, When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed.

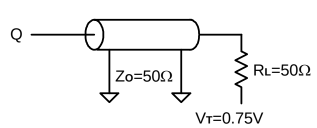
4. Byte Write enables are decided by means of a Write truth table.

5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$

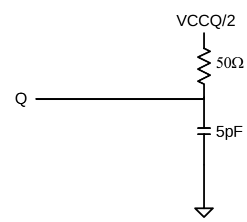
AC Test Conditions

Input Pulse Levels	GND to 3V
Input Rise and Fall Times	1 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	VccQ/2
Output Load	See Figures 1 and 2

Figure 1. Output Load Equivalent Figure



2. Output Load Equivalent

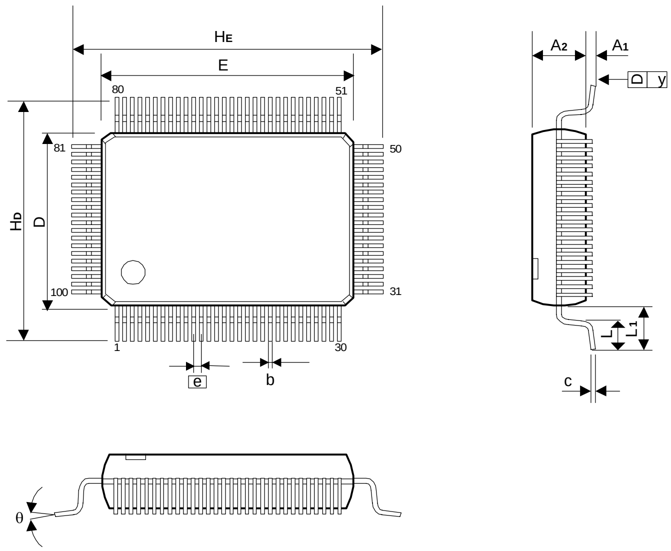


Ordering Information

Part No.	Access Times (ns)	Frequency (MHz)	Package
A63P83361E-6.5	6.5	153	100L LQFP
A63P83361E-6.5F	6.5	153	100L Pb-Free LQFP
A63P83361E-7.5	7.5	133	100L LQFP
A63P83361E-7.5F	7.5	133	100L Pb-Free LQFP
A63P83361E-8	8	117	100L LQFP
A63P83361E-8F	8	117	100L Pb-Free LQFP

Package Information

LQFP 100L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A_1	0.002	-	-	0.05	-	-
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.011	0.013	0.015	0.27	0.32	0.37
c	0.005	-	0.008	0.12	-	0.20
H_E	0.860	0.866	0.872	23.35	22.00	22.15
E	0.783	0.787	0.791	19.90	20.00	20.10
H_D	0.624	0.630	0.636	15.85	16.00	16.15
D	0.547	0.551	0.555	13.90	14.00	14.10
$\boxed{e}$	0.026 BSC			0.65 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.1
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.