

FEATURES

- Single-channel, 1024-position resolution
- 20 k Ω nominal resistance
- Calibrated 1% nominal resistor tolerance (resistor performance mode mode)
- Rheostat mode temperature coefficient: 35 ppm/ $^{\circ}$ C
- Voltage divider temperature coefficient: 5 ppm/ $^{\circ}$ C
- Single-supply operation: 9 V to 33 V
- Dual-supply operation: ± 9 V to ± 16.5 V
- SPI-compatible serial interface
- Wiper setting readback

APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation: gain and offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, and time constants
- Programmable power supply
- Low resolution DAC replacement
- Sensor calibration

GENERAL DESCRIPTION

The AD5293 is a single-channel, 1024-position digital potentiometer¹ with <1% end-to-end resistor tolerance error. The AD5293 performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. This device is capable of operating at high voltages and supporting both dual-supply operation at ± 10.5 V to ± 15 V and single-supply operation at 21 V to 30 V.

¹ In this data sheet, the terms digital potentiometer and RDAC are used interchangeably.

FUNCTIONAL BLOCK DIAGRAM

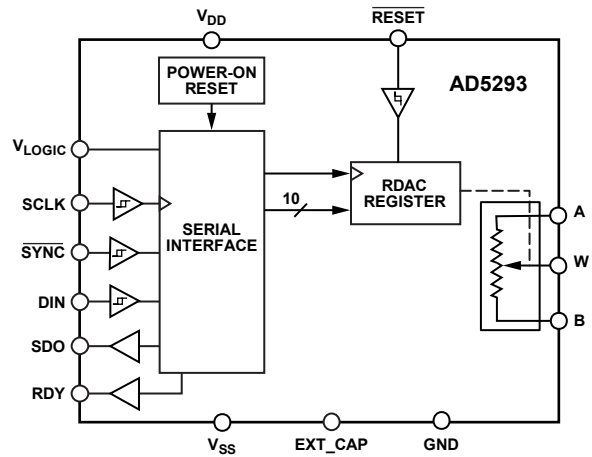


Figure 1.

07875-001

The AD5293 offers guaranteed industry-leading low resistor tolerance errors of $\pm 1\%$ with a nominal temperature coefficient of 35 ppm/ $^{\circ}$ C. The low resistor tolerance feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5293 is available in a compact 14-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of -40° C to $+105^{\circ}$ C.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Write Protection	14
Applications.....	1	Basic Operation	14
Functional Block Diagram	1	Shutdown Mode.....	14
General Description	1	Reset	15
Revision History	2	Resistor Performance Mode.....	15
Specifications.....	3	Daisy-Chain Operation	15
Electrical Characteristics	3	RDAC Architecture.....	16
Resistor Performance (R-PERF) Mode Code Range	4	Programming the Variable Resistor.....	16
Interface Timing Specifications.....	5	Programming the Potentiometer Divider	16
Timing Diagrams.....	6	EXT_CAP Capacitor.....	17
Absolute Maximum Ratings.....	7	Terminal Voltage Operating Range.....	17
Thermal Resistance	7	Applications Information	18
ESD Caution.....	7	High Voltage DAC.....	18
Pin Configuration and Function Descriptions.....	8	Programmable Voltage Source with Boosted Output.....	18
Typical Performance Characteristics	9	High Accuracy DAC	18
Test Circuits.....	13	Audio Volume Control	19
Theory of Operation	14	Outline Dimensions	20
Serial Data Interface.....	14	Ordering Guide.....	20
Shift Register	14		
RDAC Register.....	14		

REVISION HISTORY**4/09—Revision 0: Initial Version**

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{DD} = 21\text{ V to }33\text{ V}$, $V_{SS} = 0\text{ V}$; $V_{DD} = 10.5\text{ V to }16.5\text{ V}$, $V_{SS} = -10.5\text{ V to }-16.5\text{ V}$; $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$, $V_A = V_{DD}$, $V_B = V_{SS}$, $-40^\circ\text{C} < T_A < +105^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity ²	R-DNL	R_{WB}	-1		+1	LSB
Resistor Integral Nonlinearity ²	R-INL	$ V_{DD} - V_{SS} = 26\text{ V to }33\text{ V}$	-2		+2	LSB
	R-INL	$ V_{DD} - V_{SS} = 21\text{ V to }26\text{ V}$	-3		+3	LSB
Nominal Resistor Tolerance (R-Perf Mode) ³	$\Delta R_{AB}/R_{AB}$	See Table 2	-1	± 0.5	+1	%
Nominal Resistor Tolerance (Normal Mode)	$\Delta R_{AB}/R_{AB}$			± 20		%
Resistance Temperature Coefficient ⁴	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W			60	100	Ω
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity ⁵	DNL		-1		+1	LSB
Integral Nonlinearity ⁵	INL		-1.5		+1.5	LSB
Voltage Divider Temperature Coefficient ⁴	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	-8		0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		8	LSB
RESISTOR TERMINALS						
Terminal Voltage Range ⁶	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B ⁴	C_A, C_B	f = 1 MHz, measured to GND, code = half-scale		50		pF
Capacitance W ⁴	C_W	f = 1 MHz, measured to GND, code = half-scale		65		pF
Common-Mode Leakage Current	I_{CM}	$V_A = V_B = V_W$		± 1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}	$V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$	2.0	JEDEC compliant		V
Input Logic Low	V_{IL}	$V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$			0.8	V
Input Current	I_{IL}	$V_{IN} = 0\text{ V or }V_{LOGIC}$			± 1	μA
Input Capacitance ⁴	C_{IL}			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage	V_{OH}	$R_{PULL_UP} = 2.2\text{ k}\Omega\text{ to }V_{LOGIC}$	$V_{LOGIC} - 0.4$			V
Output Low Voltage	V_{OL}	$R_{PULL_UP} = 2.2\text{ k}\Omega\text{ to }V_{LOGIC}$			GND + 0.4	V
Tristate Leakage Current			-1		+1	μA
Output Capacitance ⁴	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	$V_{SS} = 0\text{ V}$	9		33	V
Dual-Supply Power Range	V_{DD}/V_{SS}		± 9		± 16.5	V
Positive Supply Current	I_{DD}	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$		0.1	2	μA
Negative Supply Current	I_{SS}	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$	-2	-0.1		μA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	$V_{LOGIC} = 5\text{ V}; V_{IH} = 5\text{ V, or }V_{IL} = \text{GND}$		1	10	μA
Power Dissipation ⁷	P_{DISS}	$V_{IH} = 5\text{ V, or }V_{IL} = \text{GND}$		8	110	μW
Power Supply Rejection Ratio ⁴	PSSR	$\Delta V_{DD}/\Delta V_{SS} = \pm 15\text{ V} \pm 10\%$		0.025	0.08	%/%

AD5293

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DYNAMIC CHARACTERISTICS^{4, 8}						
Bandwidth	BW	-3 dB		520		kHz
Total Harmonic Distortion	THD _w	V _A = 1 V rms, V _B = 0 V, f = 1 kHz,		-93		dB
V _w Settling Time	t _s	V _A = 30 V, V _B = 0 V, ±0.5 LSB error band, initial code = zero scale				
		Code = full scale, normal mode		750		ns
		Code = full scale, R-Perf mode		2.5		µs
		Code = half scale, normal mode		2.5		µs
		Code = half scale, R-Perf mode		5		µs
Resistor Noise Density	e _{N, WB}	R _{WB} = 10 kΩ, T _A = 25°C, 0 kHz to 200 kHz		0.11		nV/√Hz

¹ Typical values represent average readings at 25°C; V_{DD} = +15 V, V_{SS} = -15 V, and V_{LOGIC} = 5 V.

² Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between the R_{WB} at Code 0x02 and the R_{WB} at Code 0xFF or between R_{WA} at Code 0xFD and R_{WA} at Code 0x00. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode with a wiper current of 1 mA for V_A < 12 V and 1.2 mA for V_A ≥ 12 V.

³ The terms resistor performance mode and R-Perf mode are used interchangeably.

⁴ Guaranteed by design; not subject to production test.

⁵ INL and DNL are measured at V_w with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

⁶ The A, B, and W resistor terminals have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.

⁷ P_{DISS} is calculated from (I_{DD} × V_{DD}) + (I_{SS} × V_{SS}) + (I_{LOGIC} × V_{LOGIC}).

⁸ All dynamic characteristics use V_{DD} = +15 V, V_{SS} = -15 V, and V_{LOGIC} = 5 V.

RESISTOR PERFORMANCE (R-PERF) MODE CODE RANGE

Table 2.

Resistor Tolerance per Code	V _{DD} - V _{SS} = 30 V to 33 V		V _{DD} - V _{SS} = 26 V to 30 V		V _{DD} - V _{SS} = 22 V to 26 V		V _{DD} - V _{SS} = 21 V to 22 V	
	R _{WB}	R _{WA}	R _{WB}	R _{WA}	R _{WB}	R _{WA}	R _{WB}	R _{WA}
1% R-Tolerance	From 0x15E to 0x3FF	From 0x00 to 0x2A1	From 0x1F4 to 0x3FF	From 0x00 to 0x20B	From 0x1F4 to 0x3FF	From 0x00 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x8C to 0x3FF	From 0x00 to 0x373	From 0xB4 to 0x3FF	From 0x00 to 0x34B	From 0xFA to 0x3FF	From 0x00 to 0x305	From 0xFA to 0x3FF	From 0x00 to 0x305
3% R-Tolerance	From 0x5A to 0x3FF	From 0x00 to 0x3A5	From 0x64 to 0x3FF	From 0x00 to 0x39B	From 0x78 to 0x3FF	From 0x00 to 0x387	From 0x78 to 0x3FF	From 0x00 to 0x387

INTERFACE TIMING SPECIFICATIONS

$V_{DD} = V_{SS} = \pm 15\text{ V}$, $V_{LOGIC} = 2.7\text{ V}$ to 5.5 V , and $-40^{\circ}\text{C} < T_A < +105^{\circ}\text{C}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

Parameter	Limit ¹	Unit	Test Conditions/Comments
t_1^2	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	10	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	1	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	400 ³	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	14	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK falling edge ignore
t_{10}^4	1	ns min	RDY rise to $\overline{\text{SYNC}}$ falling edge
t_{11}^4	40	ns max	$\overline{\text{SYNC}}$ rise to RDY fall time
t_{12}^4	2.4	μs max	RDY low time, RDAC register write command execute time (R-Perf mode)
	410	ns max	RDY low time, RDAC register write command execute time (normal mode)
	1.5	ms max	Software\hardware reset
t_{13}^4	450	ns max	RDY low time, RDAC register read command execute time
t_{14}^4	450	ns max	SCLK rising edge to SDO valid
t_{RESET}	20	ns min	Minimum $\overline{\text{RESET}}$ pulse width (asynchronous)
$t_{\text{POWER-UP}}^5$	2	ms max	Power-on time to half scale

¹ All input signals are specified with $t_r = t_f = 1\text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

² Maximum SCLK frequency = 50 MHz.

³ Refer to t_{12} and t_{13} for RDAC register command operations.

⁴ $R_{\text{PULL-UP}} = 2.2\text{ k}\Omega$ to V_{LOGIC} with a capacitance load of 168 pF.

⁵ Typical power supply voltage slew rate of 2 ms/V.

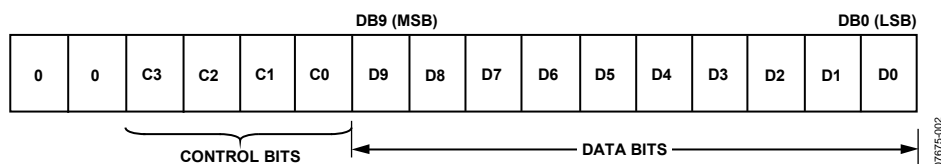
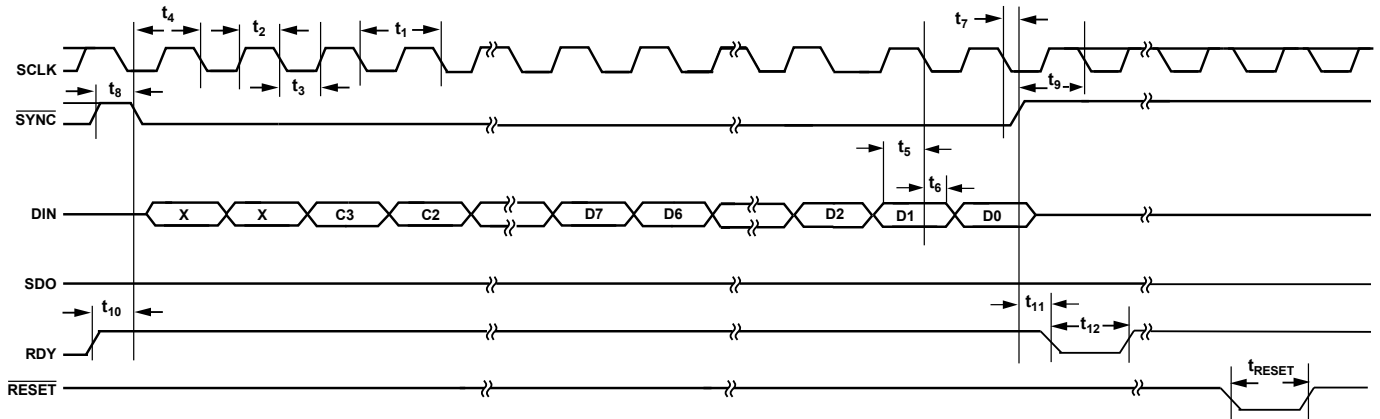
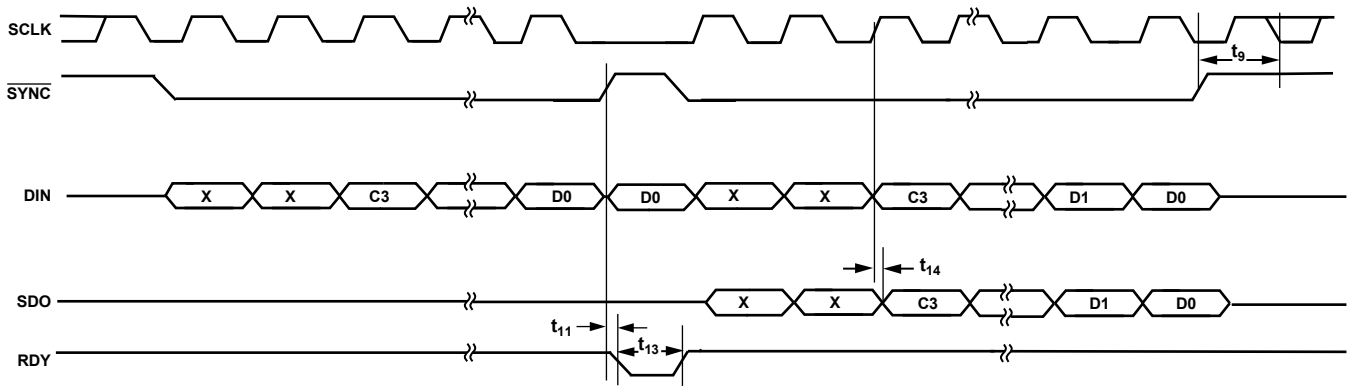


Figure 2. Shift Register Contents

TIMING DIAGRAMS



07675-003



07675-004

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4

Parameter	Rating
V_{DD} to GND	-0.3 V to +35 V
V_{SS} to GND	+0.3 V to -16.5 V
V_{LOGIC} to GND	-0.3 V to +7 V
V_{DD} to V_{SS}	35 V
V_A, V_B, V_W to GND	$V_{SS} - 0.3\text{ V}, V_{DD} + 0.3\text{ V}$
I_A, I_B, I_W	
Pulsed ¹	
Frequency >10 kHz	$\pm 3\text{ mA}/d^2$
Frequency $\leq 10\text{ kHz}$	$\pm 3\text{ mA}/\sqrt{d^2}$
Continuous	$\pm 3\text{ mA}$
Digital Input and Output Voltage to GND	-0.3 V to $V_{LOGIC} + 0.3\text{ V}$
EXT_CAP Voltage to GND	-0.3 V to +7 V
Operating Temperature Range	-40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	-65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$

¹ Maximum terminal current is bounded by the maximum current handling of the switches, the maximum power dissipation of the package, and the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

² d = pulse duty factor.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP	93 ¹	20	°C/W

¹ JEDEC 2s2p test board, still air (from 0 m/sec to 1 m/sec of airflow).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

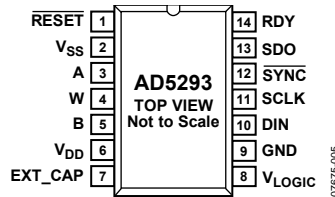


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RESET	Hardware Reset. Sets the RDAC register to midscale. $\overline{\text{RESET}}$ is activated at the logic high transition. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if not used.
2	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
3	A	Terminal A of RDAC. $V_{\text{SS}} \leq V_A \leq V_{\text{DD}}$.
4	W	Wiper Terminal W of RDAC. $V_{\text{SS}} \leq V_W \leq V_{\text{DD}}$.
5	B	Terminal B of RDAC. $V_{\text{SS}} \leq V_B \leq V_{\text{DD}}$.
6	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
7	EXT_CAP	Connect a 1 μF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥ 7 V.
8	V_{LOGIC}	Logic Power Supply, 2.7 V to 5.5 V. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
9	GND	Ground, Logic Ground Reference.
10	DIN	Serial Data Input. This part has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
12	$\overline{\text{SYNC}}$	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register, and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of SYNC, following the 16 th clock cycle. If SYNC is taken high before the 16 th clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the serial register in daisy-chain mode or in readback mode.
14	RDY	Ready. This active-high, open-drain output identifies the completion of a write or read operation to or from the RDAC register.

TYPICAL PERFORMANCE CHARACTERISTICS

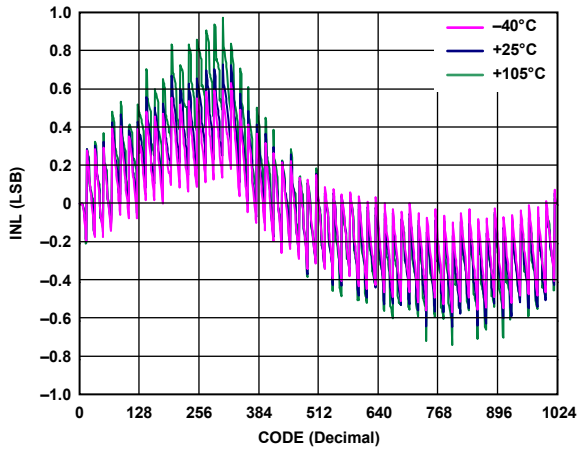


Figure 6. R-INL in R-Perf Mode vs. Code vs. Temperature

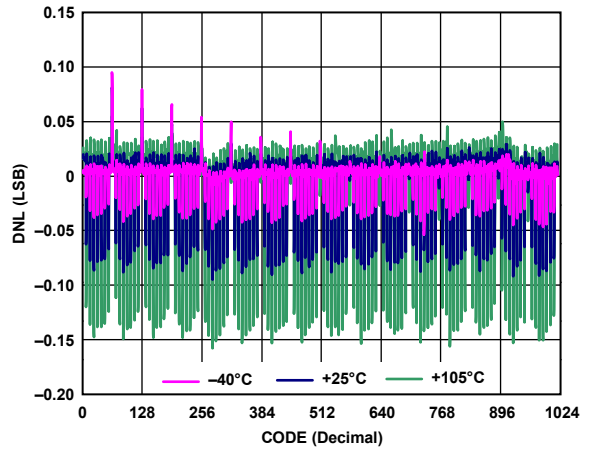


Figure 9. R-DNL in Normal Mode vs. Code vs. Temperature

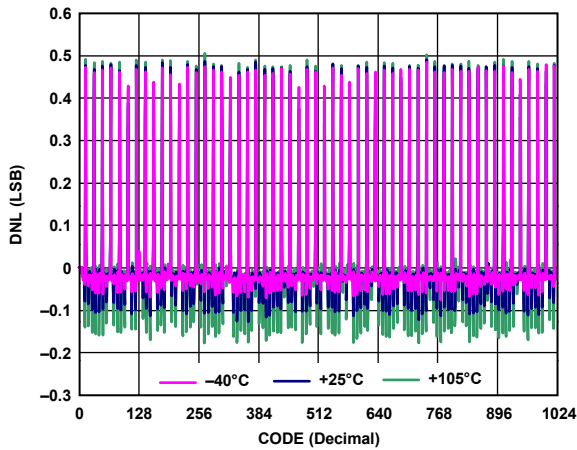


Figure 7. R-DNL in R-Perf Mode vs. Code vs. Temperature

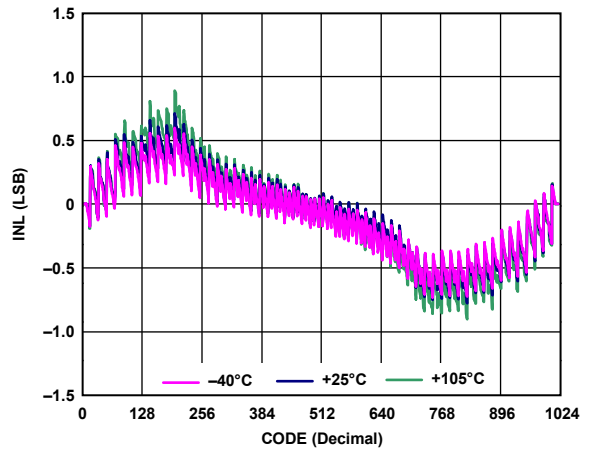


Figure 10. INL in R-Perf Mode vs. Code vs. Temperature

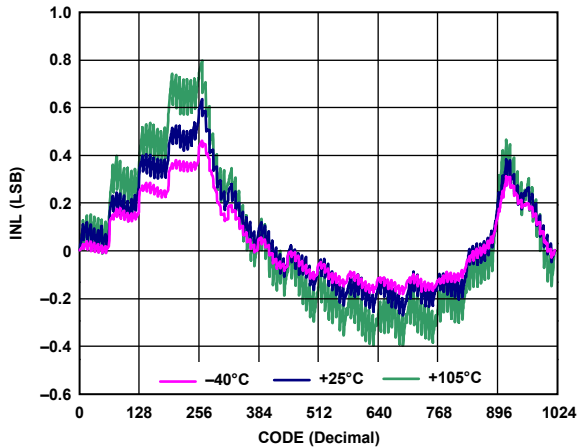


Figure 8. R-INL in Normal Mode vs. Code vs. Temperature

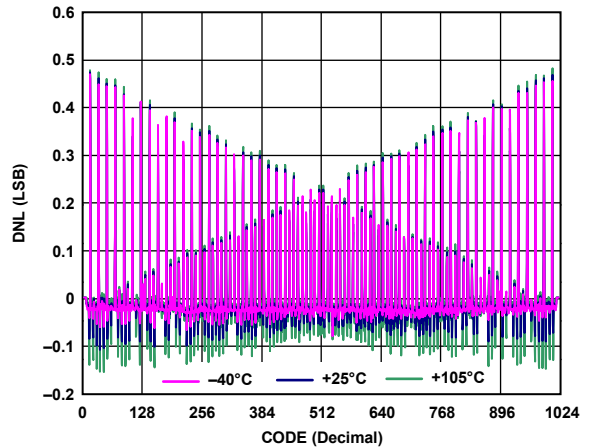


Figure 11. DNL in R-Perf Mode vs. Code vs. Temperature

07675-006

07675-011

07675-007

07675-014

07675-010

07675-015

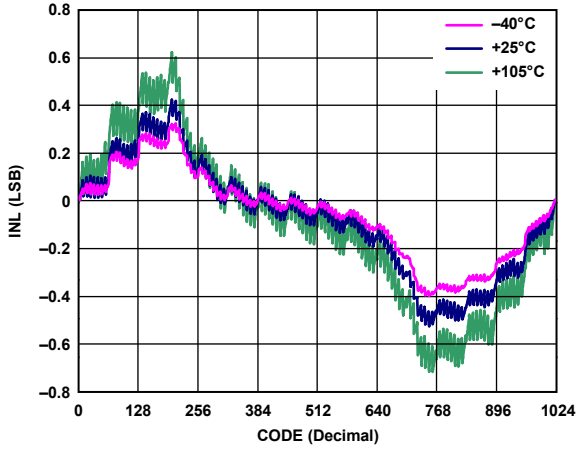


Figure 12. INL in Normal Mode vs. Code vs. Temperature

07675-018

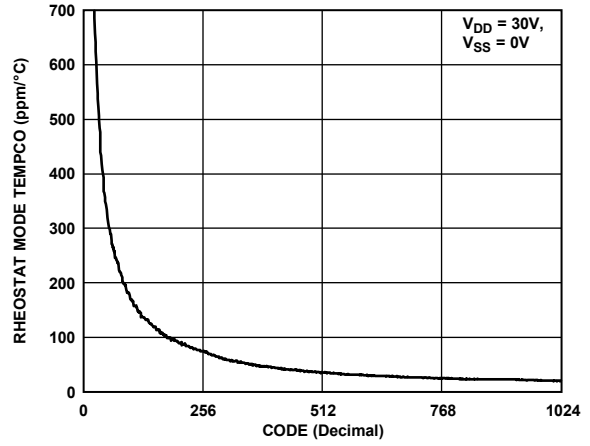


Figure 15. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

07675-024

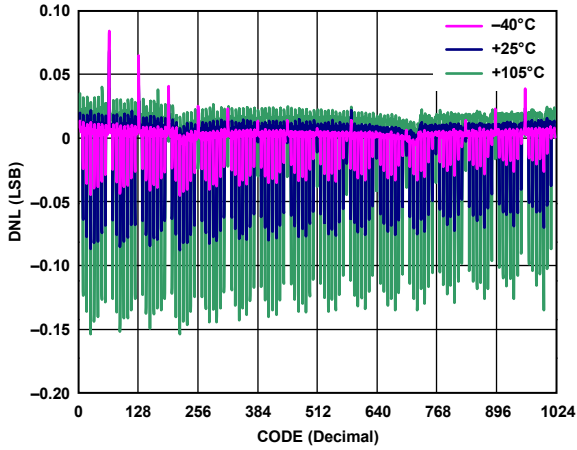


Figure 13. DNL in Normal Mode vs. Code vs. Temperature

07675-019

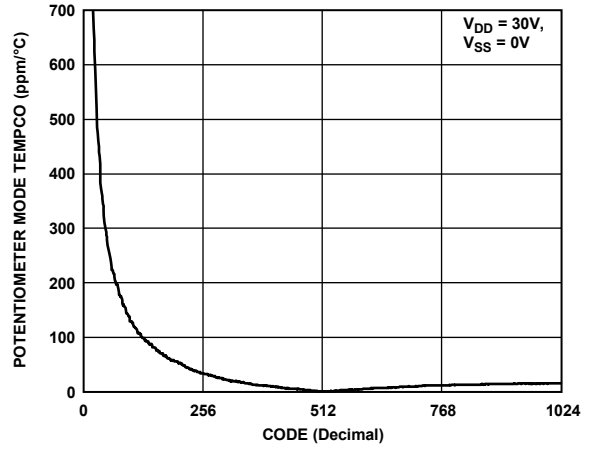


Figure 16. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

07675-023

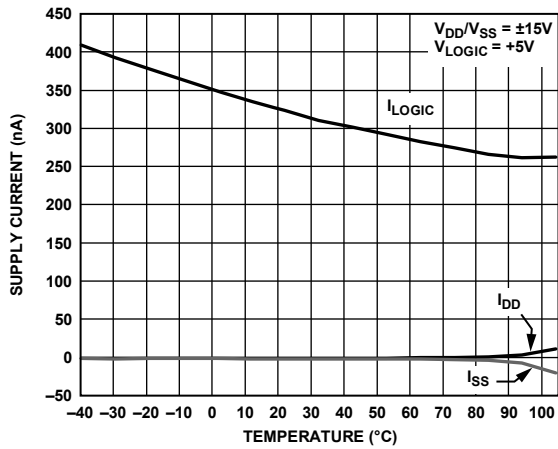


Figure 14. Supply Current vs. Temperature

07675-022

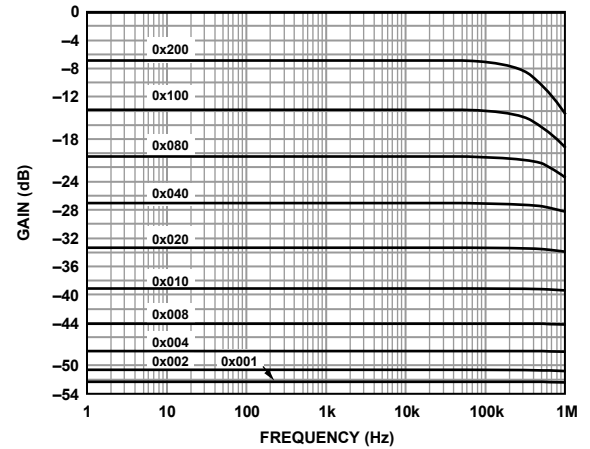


Figure 17. 20 k Ω Gain vs. Frequency vs. Code

07675-025

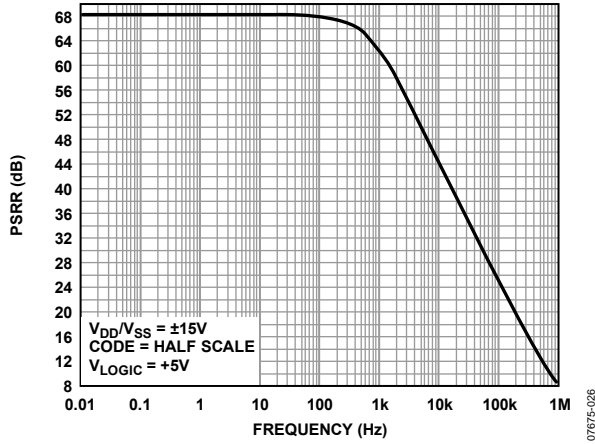


Figure 18. Power Supply Rejection Ratio vs. Frequency

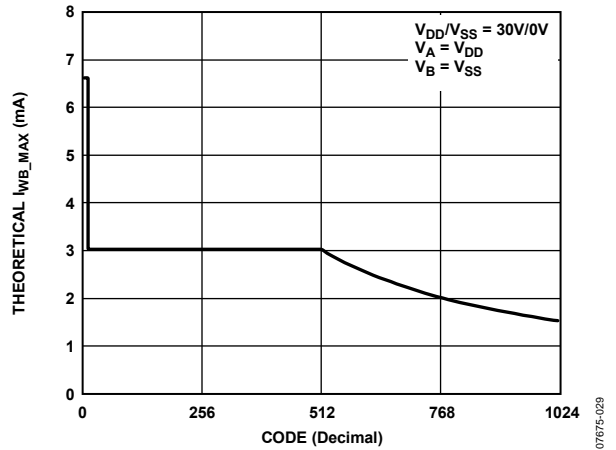


Figure 21. Theoretical Maximum Current vs. Code

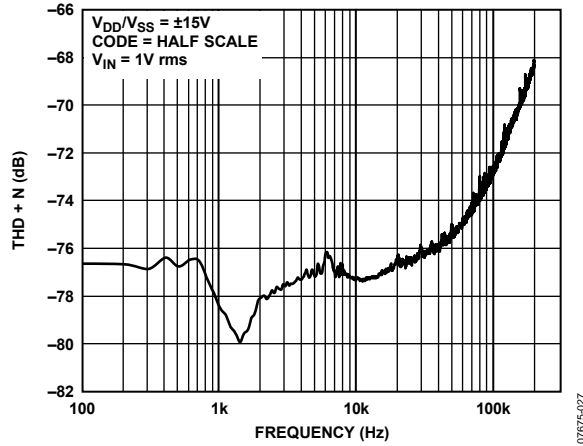


Figure 19. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

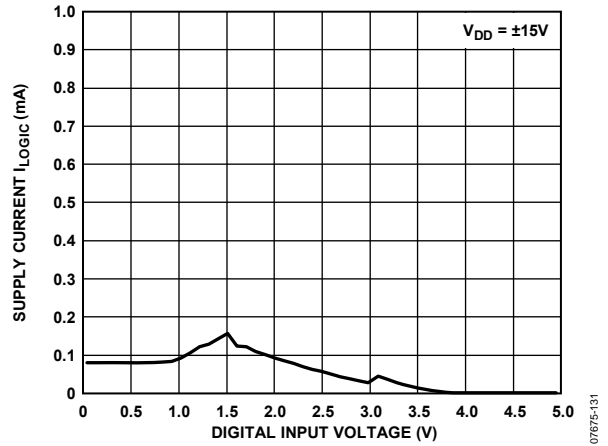


Figure 22. Supply Current, I_{LOGIC} vs. Digital Input Voltage

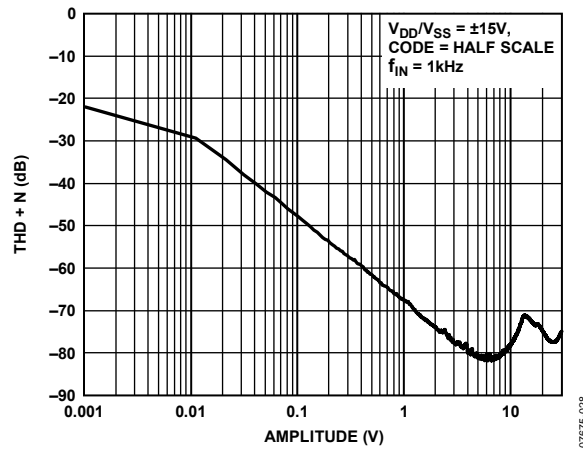


Figure 20. THD + Noise vs. Amplitude

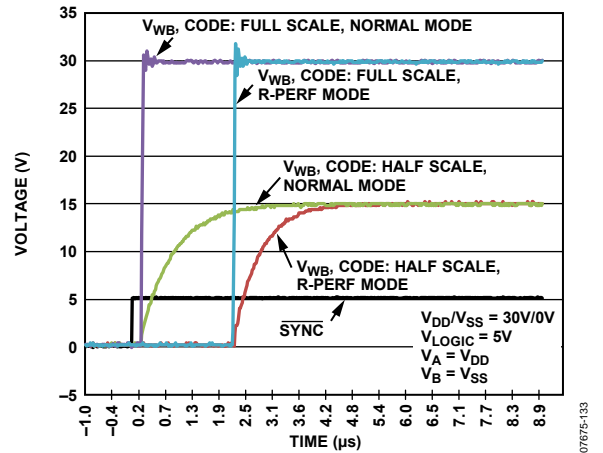


Figure 23. Large-Signal Settling Time, Code from Zero Scale to Full Scale

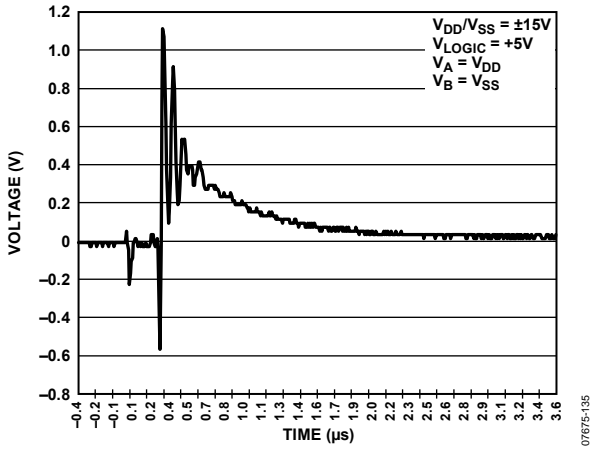


Figure 24. Maximum Transition Glitch

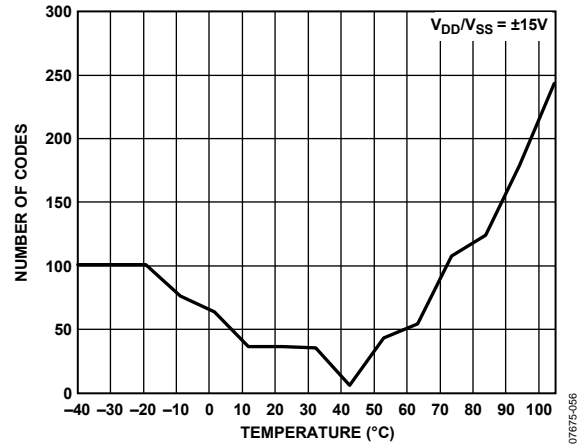


Figure 25. Code Range > 1% R-Tolerance Error vs. Temperature

TEST CIRCUITS

Figure 26 to Figure 31 define the test conditions used in the Specifications section.

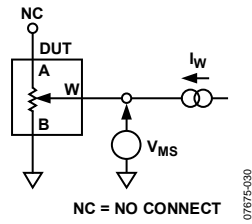


Figure 26. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

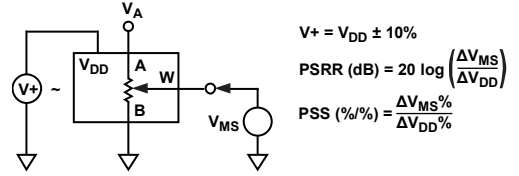


Figure 29. Power Supply Sensitivity (PSS, PSRR)

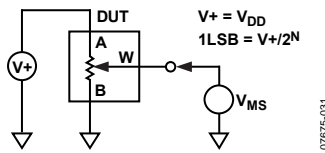


Figure 27. Potentiometer Divider Nonlinearity Error (INL, DNL)

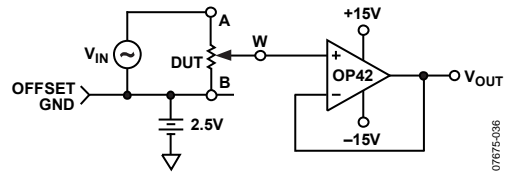


Figure 30. Gain vs. Frequency

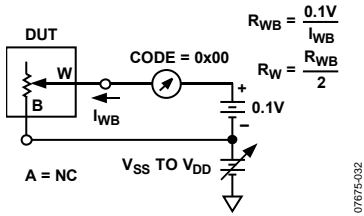


Figure 28. Wiper Resistance

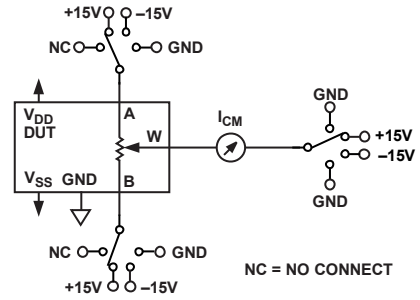


Figure 31. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5293 digital potentiometer is designed to operate as a true variable resistor for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The patented $\pm 1\%$ resistor tolerance feature helps to minimize the total RDAC resistance error, which reduces the overall system error by offering better absolute matching and improved open-loop performance. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The RDAC register can be programmed with any position setting via the standard serial peripheral interface (SPI) by loading the 16-bit data-word.

SERIAL DATA INTERFACE

The AD5293 contains a serial interface ($\overline{\text{SYNC}}$, SCLK, DIN, and SDO) that is compatible with SPI standards, as well as most DSPs. The device allows data to be written to every register via the SPI.

SHIFT REGISTER

The AD5293 shift register is 16 bits wide (see Figure 2). The 16-bit data-word consists of two unused bits, which are set to 0, followed by four control bits and 10 RDAC data bits. Data is loaded MSB first (Bit DB15). The four control bits determine the function of the software command (see Table 8). Figure 3 shows a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word is loaded from the DIN pin. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the instructions in Table 8. The command bits (Cx) control the operation of the digital potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The AD5293 has an internal counter that counts a multiple of 16 bits (per frame) for proper operation. For example, the AD5293 works with a 32-bit word, but it cannot work properly with a 31- or 33-bit word. The AD5293 does not require a continuous SCLK, when $\overline{\text{SYNC}}$ is high, and all interface pins should be operated close to the supply rails to minimize power consumption in the digital input buffers.

RDAC REGISTER

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with all 0s, the wiper is connected to Terminal B of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed. The RDY pin can be used to monitor the completion of a write to or read from the RDAC register. The AD5293 presets to mid-scale on power-up.

WRITE PROTECTION

On power-up, the serial data input register write command for the RDAC register is disabled. The RDAC write protect bit, C1 of the control register (see Table 9 and Table 10), is set to 0 by default. This disables any change of the RDAC register content, regardless of the software commands, except that the RDAC register can be refreshed to midscale using the software reset command (Command 3, see Table 8) or through hardware, using the $\overline{\text{RESET}}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register), the write protect bit, C1 of the control register, must first be programmed. This is accomplished by loading the serial data input register with Command 4 (see Table 8).

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the serial data input register with Command 1 (see Table 8) and the desired wiper position data. The RDY pin can be used to monitor the completion of this RDAC register write command. Command 2 can be used to read back the contents of the RDAC register (see Table 8). After issuing the readback command, the RDY pin can be monitored to indicate when the data is available to be read out on SDO in the next SPI operation. Instead of monitoring the RDY pin, a minimum delay can be implemented when executing a write or read command (see Table 3). Table 7 provides an example listing of a sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format for an RDAC write and read.

Table 7. RDAC Register Write and Read Example

DIN	SDO	Action
0x1802	0xFFFF ¹	Enable update of wiper position.
0x0500	0x1802	Write 0x100 to the RDAC register. Wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepare data read from RDAC register.
0x0000	0x0100	NOP (Instruction 0) sends a 16-bit word out of SDO, where the last 10 bits contain the contents of the RDAC register.

¹ X = unknown.

SHUTDOWN MODE

The AD5293 can be placed in shutdown mode by executing the software shutdown command (see Command 6 in Table 8) and then setting the LSB to 1. This feature places the RDAC in a special state in which Terminal A is open-circuited and Wiper W is connected to Terminal B. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 8 are supported while in shutdown mode.

RESET

A low-to-high transition of the hardware $\overline{\text{RESET}}$ pin loads the RDAC register with midscale. The AD5293 can also be reset through software by executing Command 3 (see Table 8). The control register is restored with default settings (see Table 10).

RESISTOR PERFORMANCE MODE

This mode activates a new, patented 1% end-to-end resistor tolerance that ensures a $\pm 1\%$ resistor tolerance on each code, that is, code = half scale, $R_{WB} = 10 \text{ k}\Omega \pm 100 \Omega$. See Table 2 to verify which codes achieve $\pm 1\%$ resistor tolerance. The resistor performance mode is activated by programming Bit C2 of the control register (see Table 9 and Table 10). The typical settling time is shown in Figure 23.

DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes. It can be used to read the contents of the wiper setting, using Command 2 (see Table 8), or it can be used for daisy-chaining multiple devices. The remaining instructions are valid for daisy-chaining multiple devices in simultaneous operations. Daisy chaining minimizes the number of port pins required from the controlling IC.

The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor, if this function is used. As shown in Figure 32, the SDO pin of one package must be tied to the DIN pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO/DIN interface may require an additional time delay between subsequent devices.

When two AD5293 devices are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1. The SYNC pin should be held low until all 32 bits are clocked into their respective serial registers. The SYNC pin is then pulled high to complete the operation.

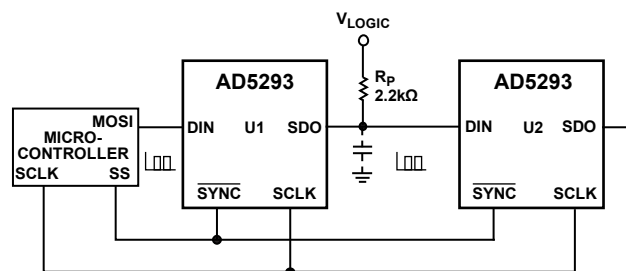


Figure 32. Daisy-Chain Configuration Using SDO

Table 8. Command Operation Truth Table

Command	Command Bits[B13:B10]				Data Bits[B9:B0] ¹										Operation
	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP command. Do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read RDAC wiper setting from SDO output in the next frame.
3	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Reset. Refresh RDAC with midscale code.
4	0	1	1	0	X	X	X	X	X	X	X	D2	D1	X	Write contents of serial register data to control register.
5	0	1	1	1	X	X	X	X	X	X	X	X	X	X	Read control register from SDO output in the next frame.
6	1	0	0	0	X	X	X	X	X	X	X	X	X	D0	Software power-down. D0 = 0 (normal mode). D0 = 1 (device placed in shutdown mode).

¹ X = don't care.

Table 9. Control Register Bit Map

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X ¹	X ¹	X ¹	X ¹	X ¹	X ¹	X ¹	C2	C1	X ¹

¹ X = don't care.

Table 10. Control Register Bit Descriptions

Register Name	Bit Name	Description
Control	C2	Calibration enable. 0 = Resistor Performance Mode (default). 1 = Normal Mode.
	C1	RDAC register write protect. 0 = locks the wiper position through the digital interface (default). 1 = allows update of wiper position through digital interface.

RDAC ARCHITECTURE

To achieve optimum cost performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5293 employs a three-stage segmentation approach, as shown in Figure 33. The AD5293 wiper switch is designed with transmission gate CMOS topology and with the gate voltage derived from V_{DD} .

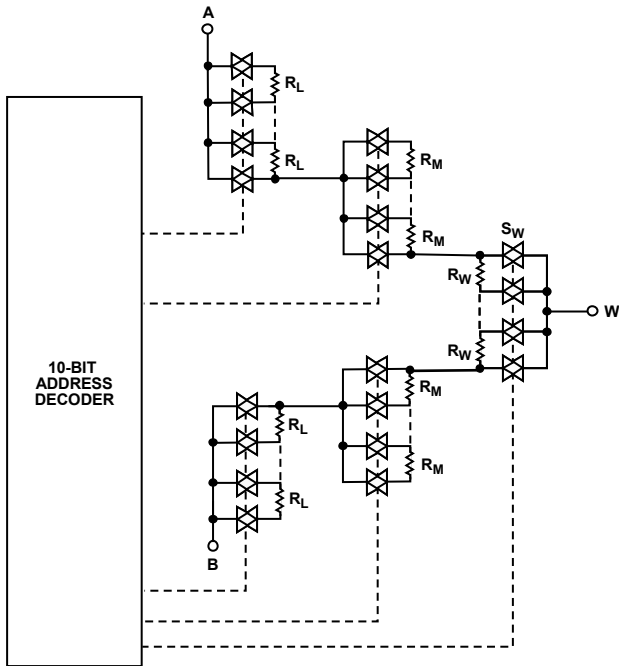


Figure 33. Simplified RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—1% Resistor Tolerance

The AD5293 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be left floating or can be tied to the W terminal as shown in Figure 34.

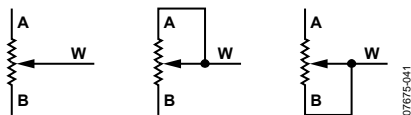


Figure 34. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB} , is available in 20 k Ω and has 1024 tap points that are accessed by the wiper terminal. The 10-bit data in the RDAC latch is decoded to select one of the 1024 possible wiper settings. The AD5293 contains an internal $\pm 1\%$ resistor tolerance calibration feature that can be enabled or disabled (enabled by default) by programming Bit C2 of the control register (see Table 9 and Table 10).

The digitally programmed output resistance between the W terminal and the A terminal, R_{WA} , and the W terminal and B terminal, R_{WB} , is calibrated to give a maximum of $\pm 1\%$ absolute resistance error over both the full supply and temperature ranges. As a result, the general equation for determining the digitally programmed output resistance between the W terminal and B terminal is

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB} \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.

R_{AB} is the end-to-end resistance.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA} . R_{WA} is also calibrated to give a maximum of 1% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equation for this operation is

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} \quad (2)$$

where:

D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.

R_{AB} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of the setting in which the part is operating, care should be taken to limit the current between the A terminal and B terminal, the W terminal and A terminal, and the W terminal and B terminal to the maximum continuous current of ± 3 mA or to the pulse current specified in Table 4. Otherwise, degradation, or possible destruction of the internal switch contact, can occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at the wiper-to-B terminal and the wiper-to-A terminal that is proportional to the input voltage at A to B, as shown in Figure 35. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

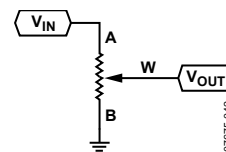


Figure 35. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for simplicity, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B that ranges from 0 V to 30 V – 1 LSB. Each LSB of voltage is equal to the voltage applied across the A terminal and B terminal, divided by the 1024 positions of the potentiometer divider. The general equation defining the output voltage at V_W , with respect to ground for any valid input voltage applied to Terminal A and Terminal B, is

$$V_W(D) = \frac{D}{1024} \times V_A + \frac{1024-D}{1024} \times V_B \quad (3)$$

To optimize the wiper position update rate when in voltage divider mode, it is recommended that the internal $\pm 1\%$ resistor tolerance calibration feature be disabled by programming Bit C2 of the control register (see Table 9 and Table 10).

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike when the part is in the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB} , not on the absolute values. Therefore, the temperature drift reduces to 5 ppm/ $^{\circ}\text{C}$.

EXT_CAP CAPACITOR

A 1 μF capacitor to GND must be connected to the EXT_CAP pin (see Figure 36) on power-up and throughout the operation of the AD5293. This capacitor must have a voltage rating of ≥ 7 V.

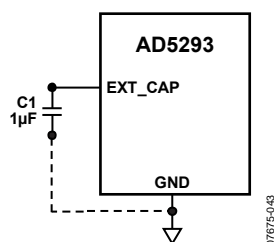


Figure 36. Hardware Setup for the EXT_CAP Pin

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the AD5293 define the boundary conditions for proper 3-terminal, digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 37).

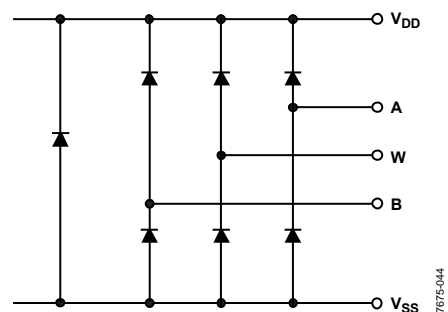


Figure 37. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5293 is primarily used as a digital ground reference. To minimize the digital ground bounce, the AD5293 ground pin should be joined remotely to common ground. The digital input control signals to the AD5293 must be referenced to the device ground pin (GND) to satisfy the logic level defined in the Specifications section.

Power-Up Sequence

Because there are diodes to limit the voltage compliance at the A, B, and W terminals (see Figure 37), it is important to power V_{DD} and V_{SS} first, before applying any voltage to the A, B, and W terminals. Otherwise, the diode is forward-biased such that V_{DD} and V_{SS} are powered up unintentionally. The ideal power-up sequence is GND, V_{SS} , V_{LOGIC} , V_{DD} , the digital inputs, and then V_A , V_B , and V_W . The order of powering up V_A , V_B , V_W , and the digital inputs is not important, as long as they are powered after V_{DD} , V_{SS} , and V_{LOGIC} .

Regardless of the power-up sequence and the ramp rates of the power supplies, the power-on preset activates after V_{LOGIC} is powered, restoring midscale to the RDAC register.

APPLICATIONS INFORMATION

HIGH VOLTAGE DAC

The AD5293 can be configured as a high voltage DAC, with output voltage as high as 33 V. The circuit is shown in Figure 38. The output is

$$V_{OUT}(D) = \frac{D}{1024} \times \left[1.2 \text{ V} \times \left(1 + \frac{R_2}{R_1} \right) \right] \quad (4)$$

where D is the decimal code from 0 to 1023.

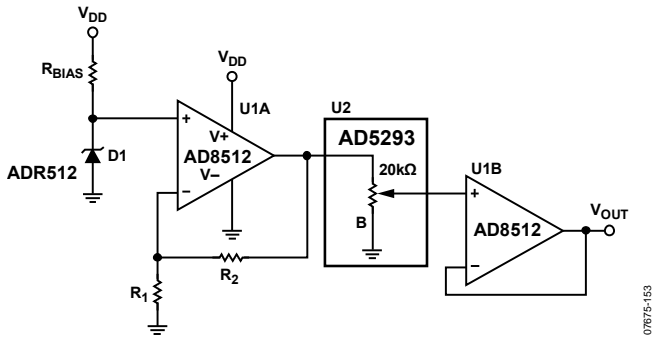


Figure 38. High Voltage DAC

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustments, such as a laser diode or tunable laser, a boosted voltage source can be considered (see Figure 39).

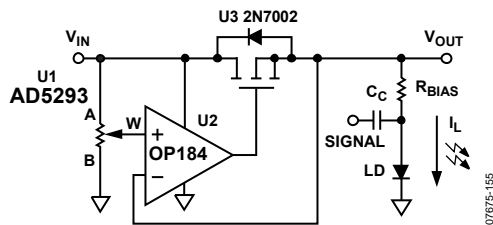


Figure 39. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET (U3). The N-channel FET power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 33 V supply.

HIGH ACCURACY DAC

It is possible to configure the AD5293 as a high accuracy DAC by optimizing the resolution of the device over a specific reduced voltage range. This is achieved by placing external resistors on either side of the RDAC, as shown in Figure 40. The improved $\pm 1\%$ resistor tolerance specification greatly reduces errors that are associated with matching to discrete resistors.

$$V_{OUT}(D) = \frac{R_3 + (D/1024 \times R_{AB}) \times V_{DD}}{R_1 + ((1024-D)/1024) \times R_{AB} + R_3} \quad (5)$$

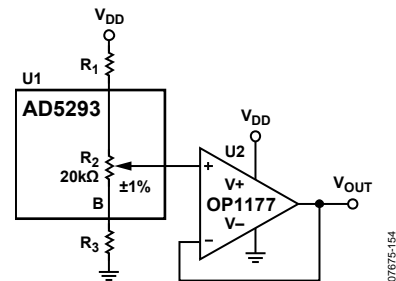


Figure 40. Optimizing Resolution

VARIABLE GAIN INSTRUMENTATION AMPLIFIER

The AD8221 in conjunction with the AD5293 and the ADG1207, as shown in Figure 41, make an excellent instrumentation amplifier for use in data acquisition systems. The data acquisition system is low distortion and low noise enable it to condition signals in front of a variety of ADCs.

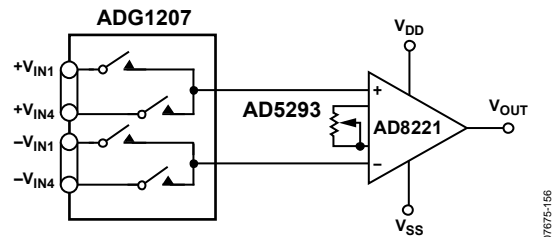


Figure 41. Data Acquisition System

The gain can be calculated by using Equation 6, as follows:

$$G(D) = 1 + \frac{49.4 \text{ k}\Omega}{(D/1024) \times R_{AB}} \quad (6)$$

AUDIO VOLUME CONTROL

The excellent THD performance and high voltage capability of the AD5293 make it ideal for digital volume control. The AD5293 is used as an audio attenuator; it can be connected directly to a gain amplifier. A large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal, causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the SYNC line to delay the device update until the audio signal crosses the window. Because the input signal can operate on top of any dc level, rather than absolute 0 V level, zero crossing in this case means the signal is ac-coupled, and the dc offset level is the signal zero reference point.

The configuration to reduce zipper noise is shown in Figure 42, and the results of using this configuration are shown in Figure 43.

The input is ac-coupled by C1 and attenuated down before feeding into the window comparator formed by U2, U3, and U4B. U6 is used to establish the signal as zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or a 0.005 V window) in this example. This output is AND'd with the chip select signal such that the AD5293 updates whenever the signal crosses the window. To avoid a constant update of the device, the chip select signal should be programmed as two pulses, rather than as one.

In Figure 43, the lower trace shows that the volume level changes from a quarter-scale to full-scale when a signal change occurs near the zero-crossing window.

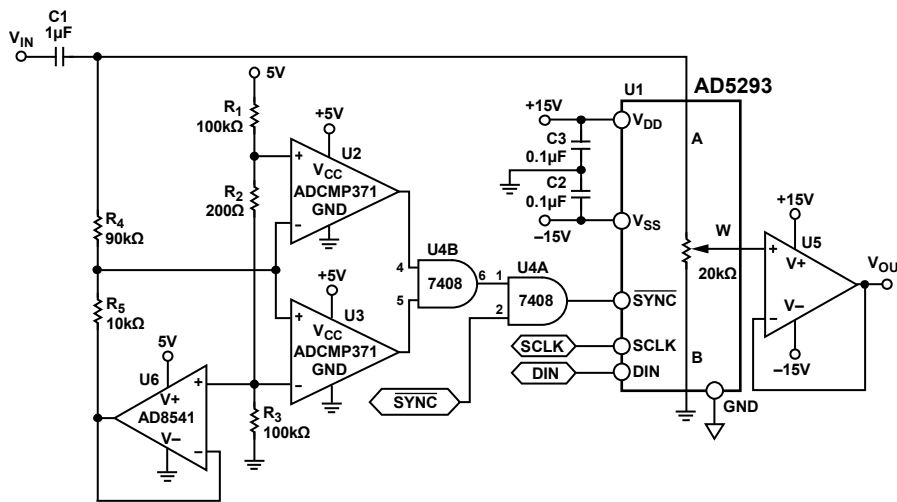


Figure 42. Audio Volume Control with Zipper Noise Reduction

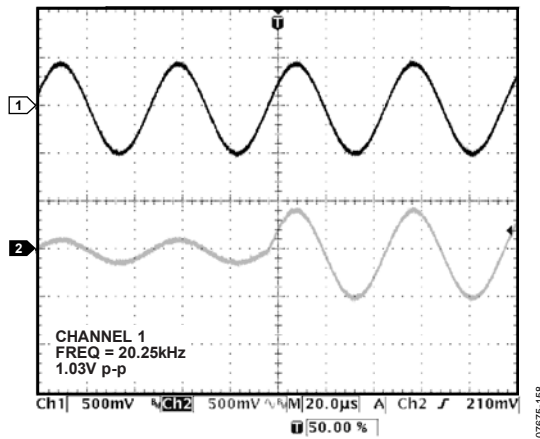
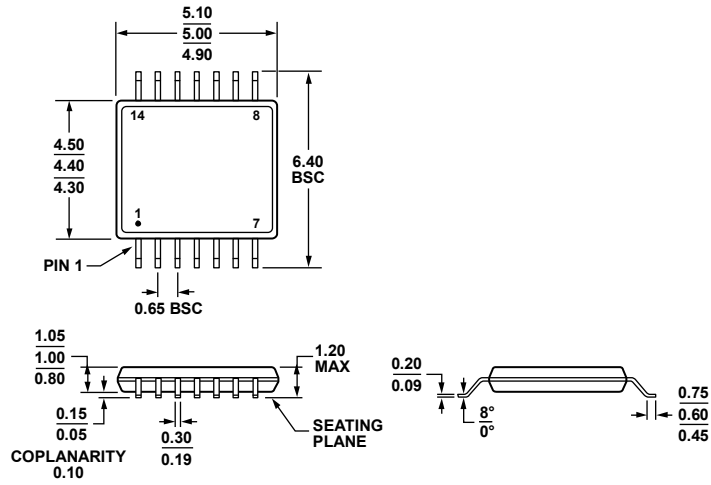


Figure 43. Zipper Noise Detector

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1
 Figure 44. 14-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-14)
 Dimensions shown in millimeters

061906-A

ORDERING GUIDE

Model	R _{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option
AD5293BRUZ-20 ¹	20	1,024	-40°C to +105°C	14-Lead TSSOP	RU-14
AD5293BRUZ-20-RL7 ¹	20	1,024	-40°C to +105°C	14-Lead TSSOP	RU-14

¹ Z = RoHS Compliant Part.