DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 320240B CCH-PW-N
(3,8” COLOR-STN)

Product Specification ***Version: 1***

03.12.2007

GENERAL SPECIFICATION

MODULE NO. :

DEM 320240B CCH-PW-N

CUSTOMER

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	20.03.2007
1	CHANGED MODULE AND BACKLIGHT, LCD DRAWING	30.03.2007

PREPARED BY: ZXD DATE: 03.12.2007

APPROVED BY: MH DATE: 03.12.2007

CONTENTS

1. FUNCTIONS &FEATURES

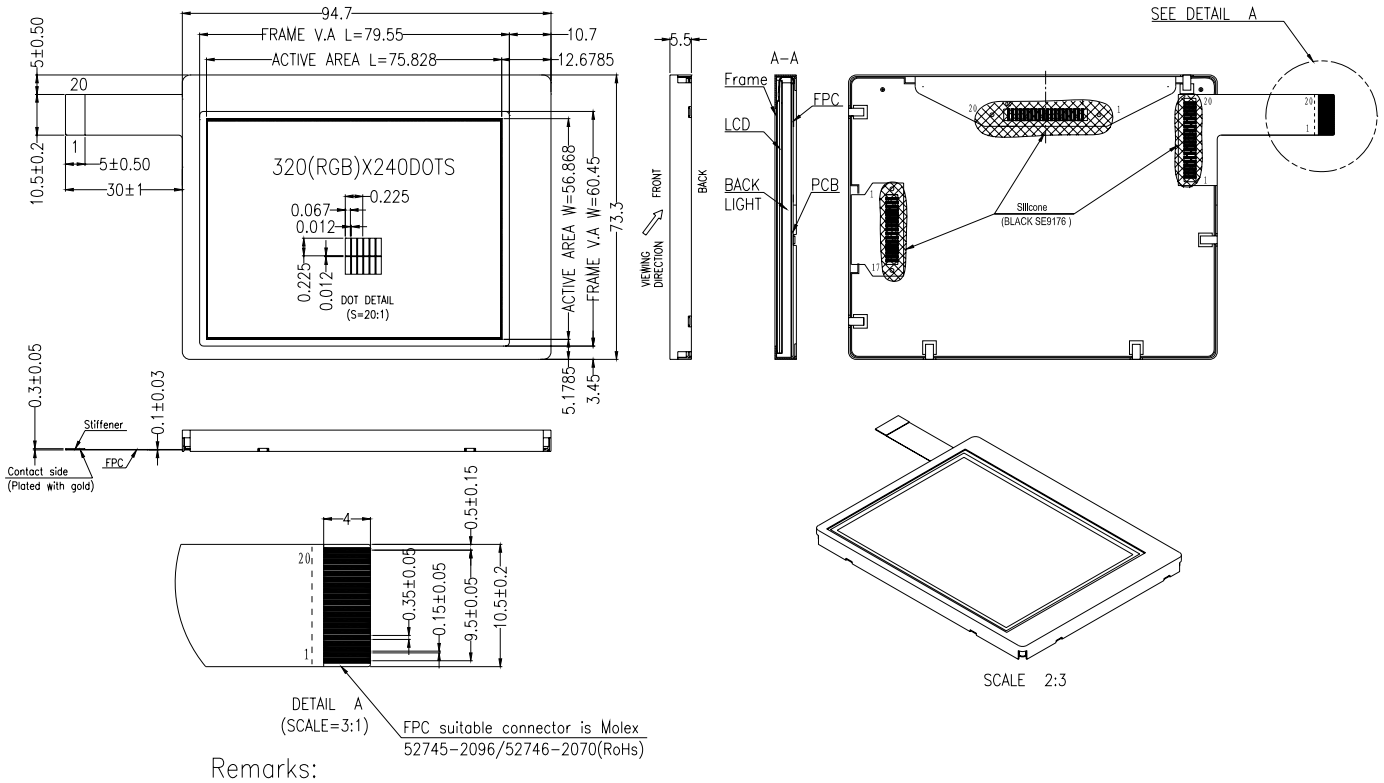
MODULE NAME	LCD TYPE
DEM 320240B CCH-PW-N	Color-STN Transmissive Negative Mode

- Display Format : 320xRGBx240 Dots
- Display Colour : 65k Colors
- Viewing Direction : 6 o'clock
- Driving Scheme : 1/240 Duty, 1/13Bias
- Power Supply voltage : 3.0 Volt (typ.)
- Lcd Voltage : 23.0 Volt (typ.)
- Operating Temperature : -20ºC ~ 70ºC
- Storage Temperature : -30ºC ~ 80ºC
- Driver IC : SSD1706Z (2x) + SSD1702Z (Solomon Systech)
- Interface : 8-Bit-Parallel
- Backlight : White LED

2. MODULE ARTWORK

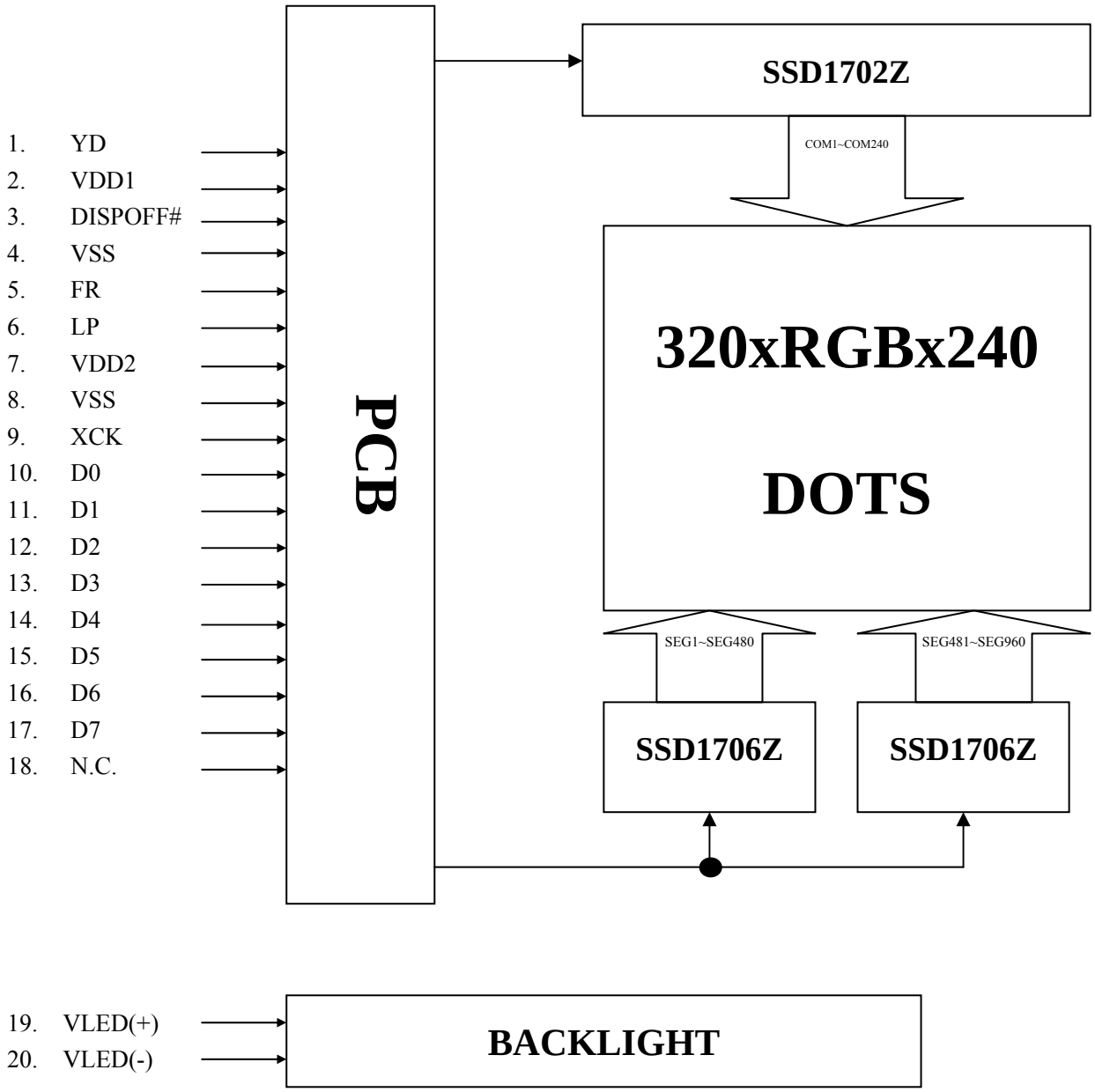
- Module size : 124.70 x 73.30 x 5.50 mm
- LCD Viewing Area : 79.228 x 60.268 mm

3. EXTERNAL DIMENSIONS



Remarks:
1,Unmarked tolerance is ±0.30;
2,All material comply with RoHs.

4. BLOCK DIAGRAM



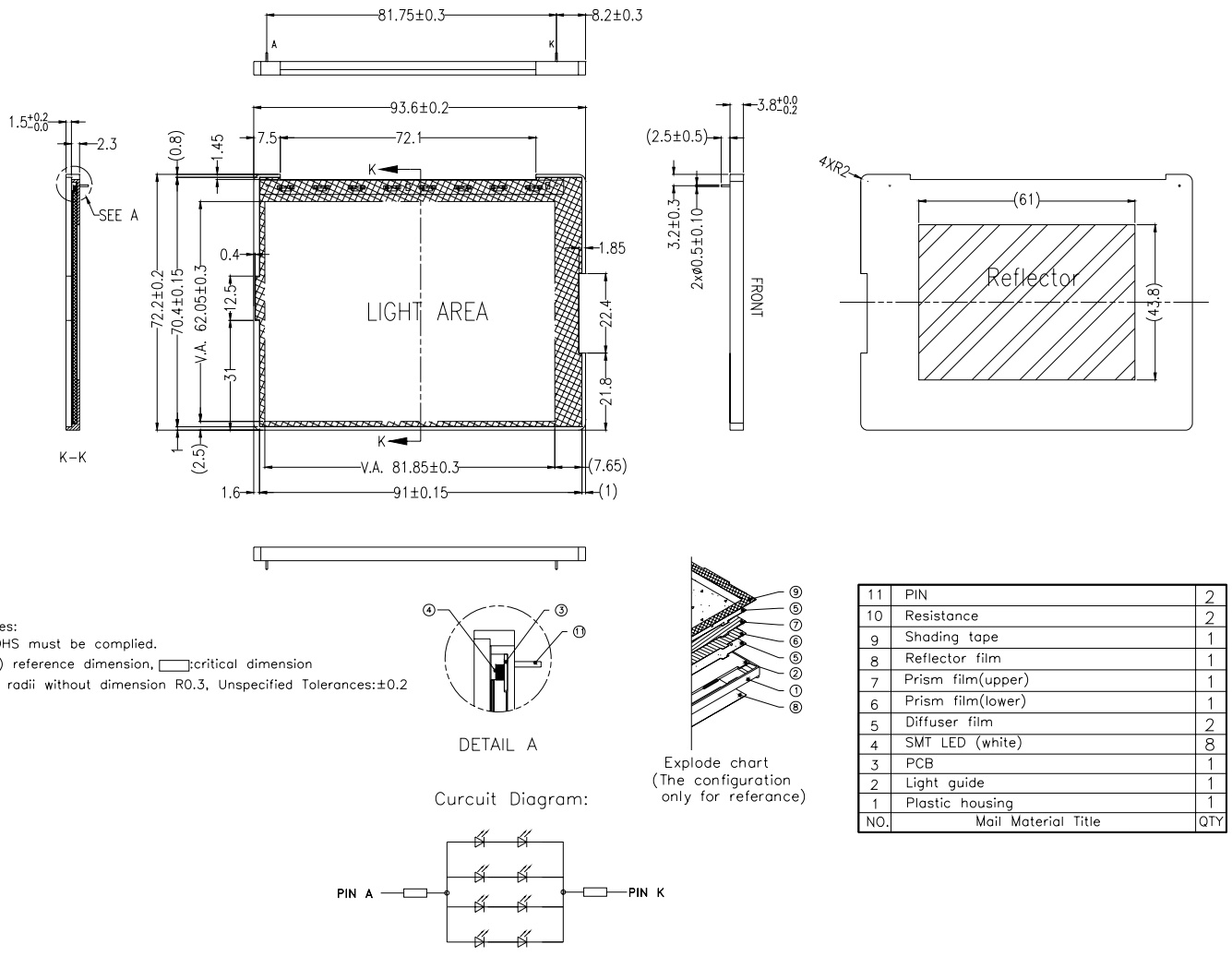
5. PIN ASSIGNMENT

Pin NO.	Symbol	Function
1	YD	Scan start pulse
2	VDD1	Power supply for logic (+3.3 Volt typ.)
3	DISPOFF#	This is the display off control pin.
4	VSS	Ground pin.
5	FR	FR is the AC signal input for LC driving waveform.
6	LP	This is the latch pulse input pin.
7	VDD2	Power supply for booster circuit (+5.0 Volt typ.)
8	VSS	Ground pin.
9	XCK	This is the shift clock input pin. Data is read at the falling edge of the clock pulse.
10	D0	These are display data input pins.
11	D1	
12	D2	
13	D3	
14	D4	
15	D5	
16	D6	
17	D7	
18	N.C.	
19	VLED(+)	Power supply for LED backlight
20	VLED(-)	Power supply for LED backlight

6. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS

Electrical–Optical Characteristics(Ta=25°C):

Item		Symbol	min.	typ.	max.	Unit	Condition
Main screen	Luminance	Lv	2500	3000		cd/m²	If=20*4mA Measure tolerance: Luminance: ± 5% Colour coordinate: ± 0.008 Voltage: ± 0.1V
	Uniformity	Avg	75			%	
	Colour Coordinate	X	0.283		0.330		
		Y	0.276		0.339		
Sub screen	Luminance	Lv	----			cd/m²	
	Uniformity	Avg	--			%	
	Colour Coordinate	X	---		---		
		Y	---		---		
Forward Voltage		Vf		6.4		V	
Reverse Current		Ir			--	μA	Vr= -- V
● Operating Temperature: -30~+70°C ● Storage Temperature: -40~+80°C							



Notes:
1.ROHS must be complied.
2.( ) reference dimension, ▭:critical dimension
3.All radii without dimension R0.3, Unspecified Tolerances:±0.2

NO.	Mail Material Title	QTY
11	PIN	2
10	Resistance	2
9	Shading tape	1
8	Reflector film	1
7	Prism film(upper)	1
6	Prism film(lower)	1
5	Diffuser film	2
4	SMT LED (white)	8
3	PCB	1
2	Light guide	1
1	Plastic housing	1

7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VDD	Logic supply voltage	-0.3 to +4.0	V
V0	LC driving voltage supply	-0.3 to +32.0	V
V12		-0.3 to + V0+0.3	V
V43		-0.3 to + V0+0.3	V
V5		-0.3 to + V0+0.3	V
VI	Input voltage	-0.3 to VDD+0.3	V
TA	Operating Temperature	-20 to +70	°C
TSTG	Storage Temperature	-30 to +80	°C

***** Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that VIN and VOUT be constrained to the range VSS ≤ (VIN or VOUT) ≤ VDD. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either VSS or VDD). Unused outputs must be left open. All dummy and NC pins should be left open and unconnected. Do not group dummy or NC pins together. This device may be light sensitive. Caution should be taken to avoid exposed of this device to any light source during normal operation. This device is not radiation protected.

8. DC CHARACTERISTICS

8.1 SSD1702Z DC CHARACTERISTICS

(Unless otherwise specified, voltage referenced to V_{SS}, V_{DD} = 2.4 to 3.6 Volt, V_0=+15.0 to +30.0 Volt, T_A = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	V_{DD} operation voltage	-	2.4	-	3.6	V
V_0	V_0 operation voltage	-	15.0	-	30.0	V
V_{IH}	Input voltage at D0-D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF#		0.8xV_{DD}	-	-	V
V_{IL}			-	-	0.2xV_{DD}	V
V_{OH}	Output voltage at EIO1, EIO2	I_{OH} = -0.4mA	0.9xV_{DD}	-	-	V
V_{OL}		I_{OL} = +0.4mA	-	-	0.1xV_{DD}	V
R_{ON}	Output resistance at Y1-Y240	ΔV_{ON} = 0.5Volt, V_0 = +30Volt	-	1.1	1.5	kΩ
		ΔV_{ON} = 0.5Volt, V_0 = +20Volt	-	1.1	2.0	kΩ

8.2 SSD1706Z DC CHARACTERISTICS

(Unless otherwise specified, voltage referenced to V_{SS}, V_{DD} = 2.4 to 3.6Volt, V_0=+15.0 to +30.0 Volt, T_A = -20 to 70°C)

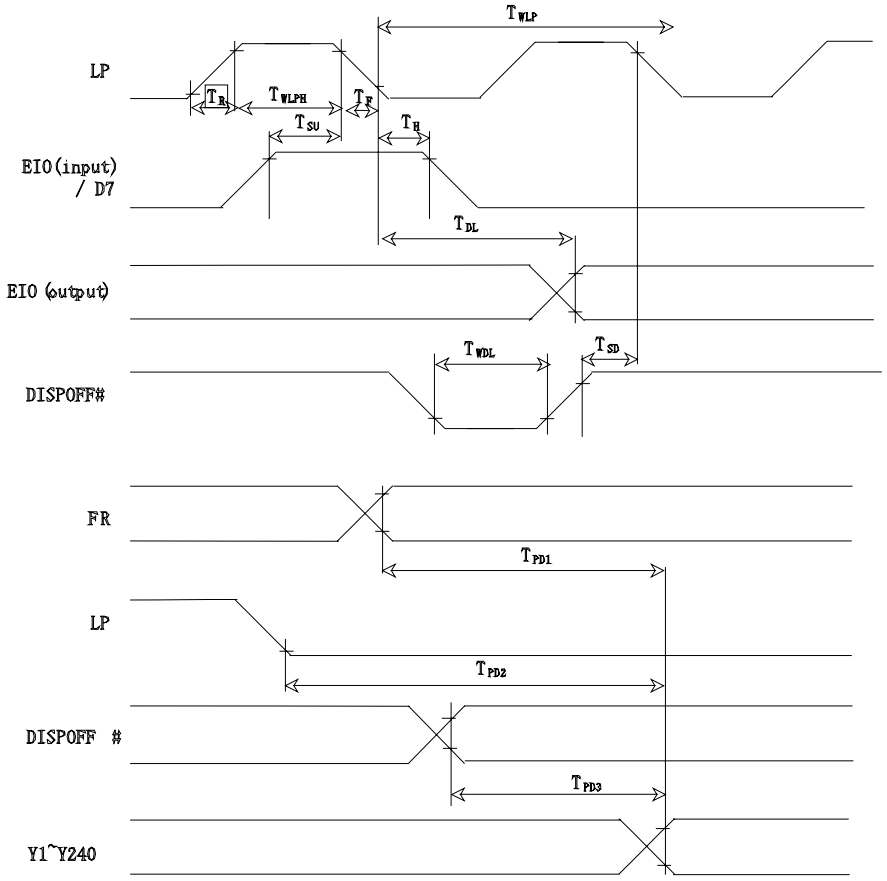
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	V_{DD} operating voltage		2.4	-	3.6	V
V_0	V_0 operating voltage		15.0	-	30.0	V
V_{IH}	Input voltage at D0-D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF#	-	0.8xV_{DD}	-	-	V
V_{IL}			-	-	0.2xV_{DD}	V
V_{OH}	Output voltage at EIO1, EIO2	I_{OH} = -0.4mA	0.9xV_{DD}	-	-	V
V_{OL}		I_{OL} = +0.4mA	-	-	0.1xV_{DD}	V
R_{ON}	Output resistance	V_O=30Volt, ΔV_{ON} = 0.5Volt, Vout = +30Volt	-	1.1	-	kΩ

9. AC CHARACTERISTICS

9.1 SSD1702Z INTERFACE TIMING CHARACTERISTICS

(V_{DD}-V_{SS} = 2.4 to 3.6 Volt, V_0=+15.0 to +30.0 Volt, T_A = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_{WLP}	Shift clock period	T_R, $T_F \leq$ 20ns	250	-	-	ns
T_{WLPH}	Shift clock H pulse width	V_{DD} = +3.0 to 3.6 Volt	15	-	-	ns
		V_{DD} = +2.4 to 3.0 Volt	30	-	-	ns
T_{SU}	Data setup time	-	30	-	-	ns
T_H	Data hold time	-	50	-	-	ns
T_R	Input signal rise time	-	-	-	50	ns
T_F	Input signal fall time	-	-	-	50	ns
T_{SD}	DISPOFF# removal time	-	100	-	-	ns
T_{WDL}	DISPOFF# L pulse width	-	1.2	-	-	µs
T_{DL}	Output delay time (1)	C_L=15 pF	-	-	200	ns
T_{PD1},T_{PD2}	Output delay time (2)	C_L=15 pF	-	-	1.2	µs
T_{PD3}	Output delay time (3)	C_L=15 pF	-	-	1.2	µs



9.2 SSD1706Z AC CHARACTERISTICS

(Unless otherwise specified, voltage referenced to V_{SS}, V_{DD} = 3.0 to 3.6 Volt, V_0=+15.0 to +30.0 Volt, T_A = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_{WCK}	Shift clock period (1)	T_R, $T_F \leq$ 10ns	50	-	-	ns
T_{WCKH}	Shift clock H pulse width	-	15	-	-	ns
T_{WCKL}	Shift clock L pulse width	-	15	-	-	ns
T_{DS}	Data setup time	-	10	-	-	ns
T_{DH}	Data hold time	-	12	-	-	ns
T_{WLPH}	Latch pulse H pulse width	-	15	-	-	ns
T_{LD}	Shift clock rise to Latch pulse rise time	-	0	-	-	ns
T_{SL}	Shift clock fall to Latch pulse fall time	-	25	-	-	ns
T_{LS}	Latch pulse rise to Shift clock rise time	-	25	-	-	ns
T_{LH}	Latch pulse fall to Shift pulse fall time	-	25	-	-	ns
T_R	Input signal rise time (2)	-	-	-	50	ns
T_F	Input signal fall time (2)	-	-	-	50	ns
T_S	Enable setup time	-	10	-	-	ns
T_{SD}	DISPOFF# removal time	-	100	-	-	ns
T_{WDL}	DISPOFF# L pulse width	-	1.2	-	-	µs
T_D	XCK to EIO Output delay time	C_L = 15pF	-	-	30	ns
T_{PD1}	FR to YOUT delay time	C_L = 15pF	-	-	1.2	µs
T_{PD2}	LP to YOUT delay time	C_L = 15pF	-	-	1.2	µs
T_{PD3}	DISPOFF# to YOUT delay time	C_L = 15pF	-	-	1.2	µs

Note:

(1) Take the cascade connection into consideration

(2) (T_{CK}-T_{WCKH}-T_{WCKL})/2 is maximum in the case of high speed operation.

9.3 SSD1706Z INTERFACE TIMING CHARACTERISTICS

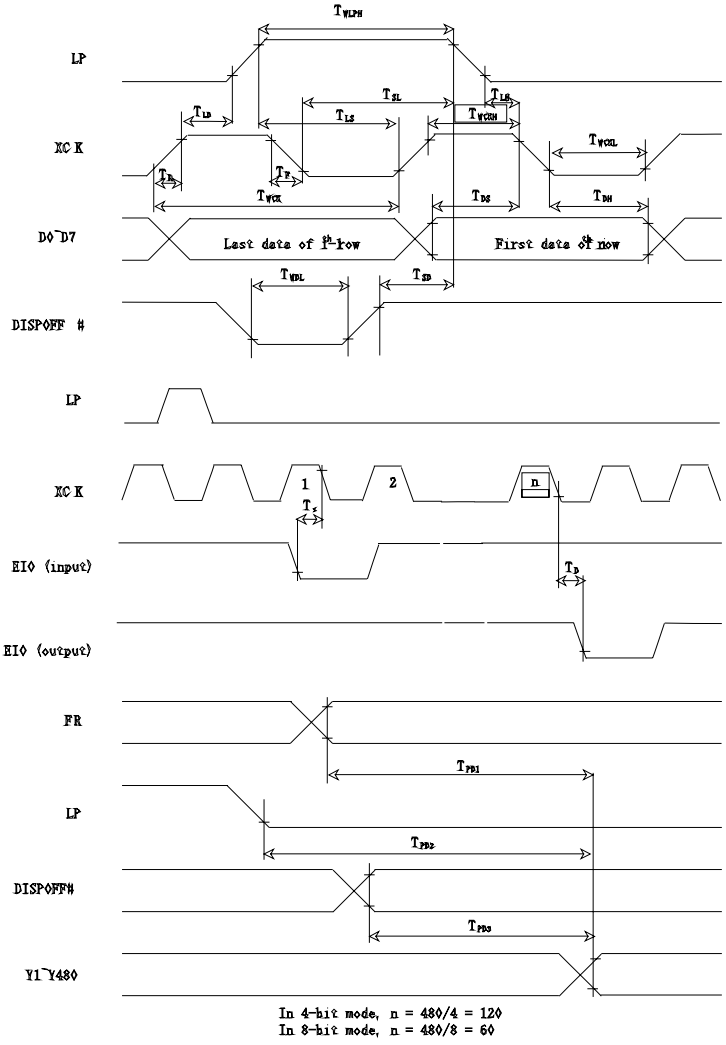
(V_{DD}-V_{SS} = +2.4 to +3.0 Volt, V_0=+15.0 to +30.0 Volt, T_A = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_{WCK}	Shift clock period (1)	T_R, $T_F \leq$ 10ns	66	-	-	ns
T_{WCKH}	Shift clock H pulse width	-	23	-	-	ns
T_{WCKL}	Shift clock L pulse width	-	23	-	-	ns
T_{DS}	Data setup time	-	15	-	-	ns
T_{DH}	Data hold time	-	23	-	-	ns
T_{WLPH}	Latch pulse H pulse width	-	30	-	-	ns
T_{LD}	Shift clock rise to Latch pulse rise time	-	0	-	-	ns
T_{SL}	Shift clock fall to Latch pulse fall time	-	50	-	-	ns
T_{LS}	Latch pulse rise to Shift clock rise time	-	30	-	-	ns
T_{LH}	Latch pulse fall to Shift pulse fall time	-	30	-	-	ns
T_R	Input signal rise time (2)	-	-	-	50	ns
T_F	Input signal fall time (2)	-	-	-	50	ns
T_S	Enable setup time	-	15	-	-	ns
T_{SD}	DISPOFF# removal time	-	100	-	-	ns
T_{WDL}	DISPOFF# L pulse width	-	1.2	-	-	µs
T_D	XCK to EIO Output delay time	C_L = 15pF	-	-	41	ns
T_{PD1}	FR to YOUT delay time	C_L = 15pF	-	-	1.2	µs
T_{PD2}	LP to YOUT delay time	C_L = 15pF	-	-	1.2	µs
T_{PD3}	DISPOFF# to YOUT delay time	C_L = 15pF	-	-	1.2	µs

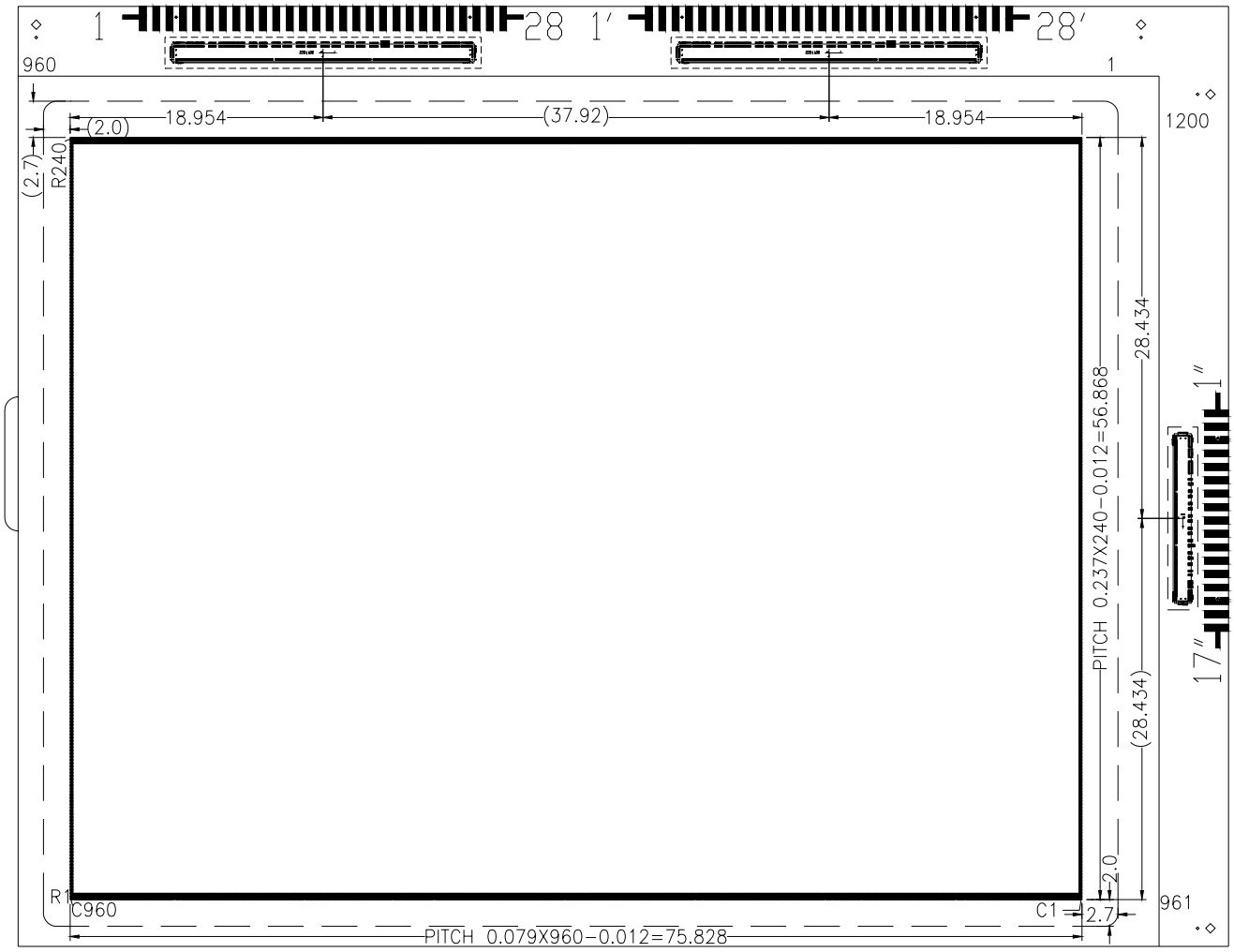
Note:

(1) Take the cascade connection into consideration

(2) (T_{CK}-T_{WCKH}-T_{WCKL})/2 is maximum in the case of high speed operation.

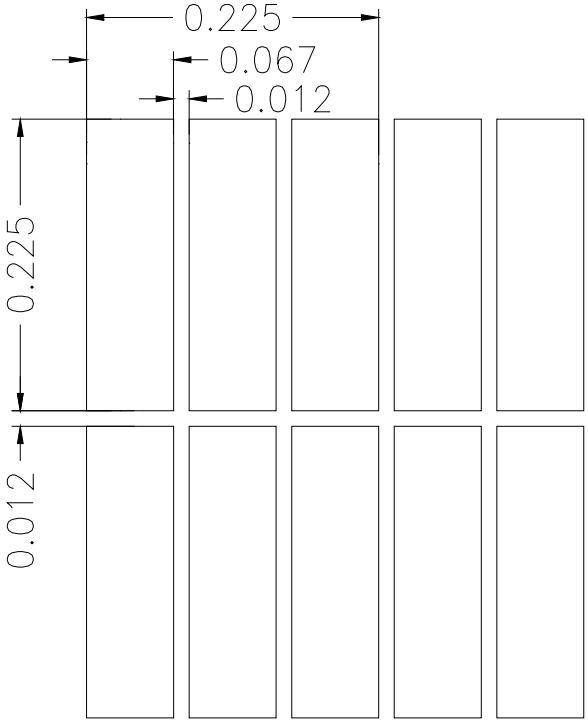


10. LABELLING



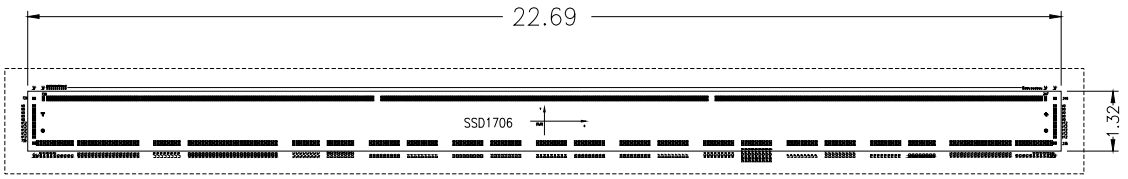
11. PAD CONFIGURATION GRAPHIC DIMENSION

PAD NO.	PAD CONFIGURATION
1	Y1[C1(R1-R240)]
2	Y2[C2(R1-R240)]
|	|
479	Y479[C479(R1-R240)]
480	Y480[C480(R1-R240)]
481	Y1[C481(R1-R240)]
482	Y2[C482(R1-R240)]
|	|
959	Y479[C959(R1-R240)]
960	Y480[C960(R1-R240)]
961	Y1[R1(C1-C960)]
962	Y2[R2(C1-C960)]
|	|
1999	Y239[R239(C1-C960)]
1200	Y240[R240(C1-C960)]



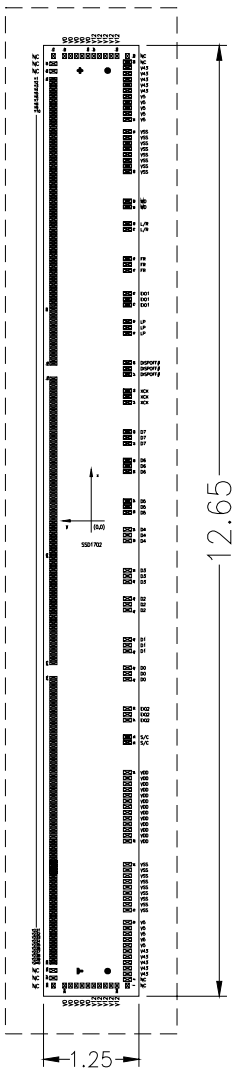
12. IC PIN NO. CONFIGURATION

12.1 SSD1706Z



PAD NO.	IC NO. CONFIGURATION	PAD NO.	IC NO. CONFIGURATION
1'	V0	16'	D6
2'	V12	17'	D7
3'	V43	18'	XCK
4'	V5	19'	DISPOFF#
5'	VSS	20'	LP
6'	L/R	21'	EIO1
7'	VDD	22'	FR
8'	S/C	23'	MD
9'	EIO2	24'	VSS
10'	D0	25'	V5
11'	D1	26'	V43
12'	D2	27'	V12
13'	D3	28'	V0
14'	D4		
15'	D5		

12.2 SSD1702Z



PAD NO.	IC NO. CONFIGURATION
1"	V0
2"	V12
3"	V43
4"	V5
5"	VSS,S/C,D0~D7,XCK,MD
6"	VDD
7"	EIO2
8"	DISPOFF#
9"	LP
10"	EIO1
11"	FR
12"	L/R
13"	VSS,S/C,D0~D7,XCK,MD
14"	V5
15"	V43
16"	V12
17"	V0

13. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

14. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections.