EFM32®

... the world's most energy friendly microcontrollers

EFM32G280 DATASHEET

EFM32G280F128/EFM32G280F64/EFM32G280F32

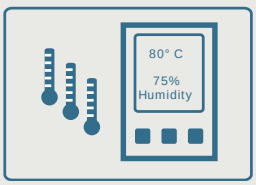
Preliminary

- **ARM Cortex-M3 CPU platform**
  - High Performance 32-bit processor @ up to 32 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including Real Time Clock with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 µA/MHz @ 3 V Sleep Mode
  - 180 µA/MHz @ 3 V Run Mode, with code executed from flash
- **128/64/32 KB Flash**
- **16/16/8 KB RAM**
- **85 General Purpose I/O pins**
  - Configurable Push-pull, Open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 64 MB of external memory mapped space**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
  - 3× 16-bit Timer/Counter
    - 3×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 24-bit Real-Time Counter
  - 3× 8-bit Pulse Counter
    - Asynchronous pulse counting/quadrature decoding
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Communication interfaces**
  - 3× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA
    - Triple buffered full/half-duplex operation
    - 4-16 data bits
  - Universal Asynchronous Receiver/Transmitter
    - Triple buffered full/half-duplex operation
    - 8-9 data bits
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single ended channels/4 differential channels
    - On-chip temperature sensor
    - Conversion tailgating for predictable latency
  - 12-bit 500 ksamples/s Digital to Analog Converter
    - 2 single ended channels/1 differential channel
  - 2× Analog Comparator
    - Programmable speed/current
    - Capacitive sensing with up to 8 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
  - 1-pin Serial Wire Viewer
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.8 to 3.8 V**
- **LQFP100 package**

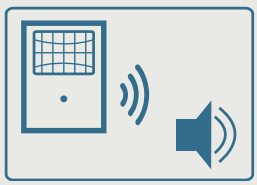
EFM32G280 microcontrollers are suited for all battery operated applications

Energy Metering

Industrial/ Home Automation



Wireless Alarm/ Security



Medical Systems

ENERGY® micro

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32G280 devices.

Table 1.1. Ordering Information

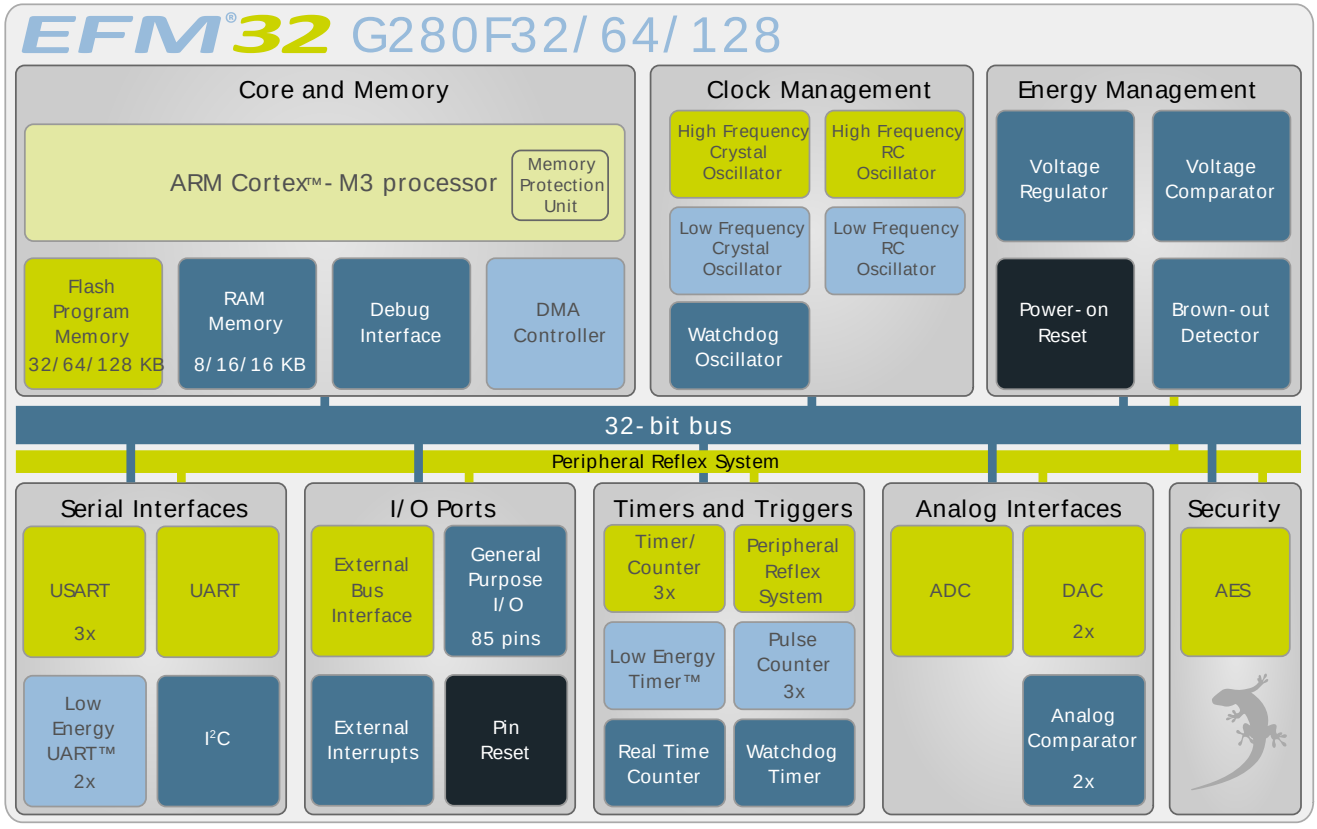
Ordering Code	Flash (KB)	RAM (KB)	Max Speed (MHz)	Supply Voltage	Temperature	Package
EFM32G280F32-QFP100	32	8	32	1.8 to 3.8V	-40 to 85 ºC	LQFP100
EFM32G280F64-QFP100	64	16	32	1.8 to 3.8V	-40 to 85 ºC	LQFP100
EFM32G280F128-QFP100	128	16	32	1.8 to 3.8V	-40 to 85 ºC	LQFP100

Visit **www.energymicro.com** for information on global distributors and representatives or contact **sales@energymicro.com** for additional information.

1.1 Block Diagram

A block diagram of the EFM32G280 is shown in Figure 1.1 (p. 2) .

Figure 1.1. Block Diagram



2 System Summary

2.1 System Introduction

The EFM32G family of MCUs is the world's most energy friendly microcontroller. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also and shows a summary of the configuration for the EFM32G280 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32G Reference Manual*.

2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32G Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to the DAC. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all

peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

2.1.11 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and IrDA devices.

2.1.13 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.17 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.18 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.19 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.20 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.21 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.22 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.23 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK

cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.24 General Purpose Input/Output (GPIO)

In the EFM32G280, there are 85 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advances configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32G280 is a subset of the feature set described in the EFM32G Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

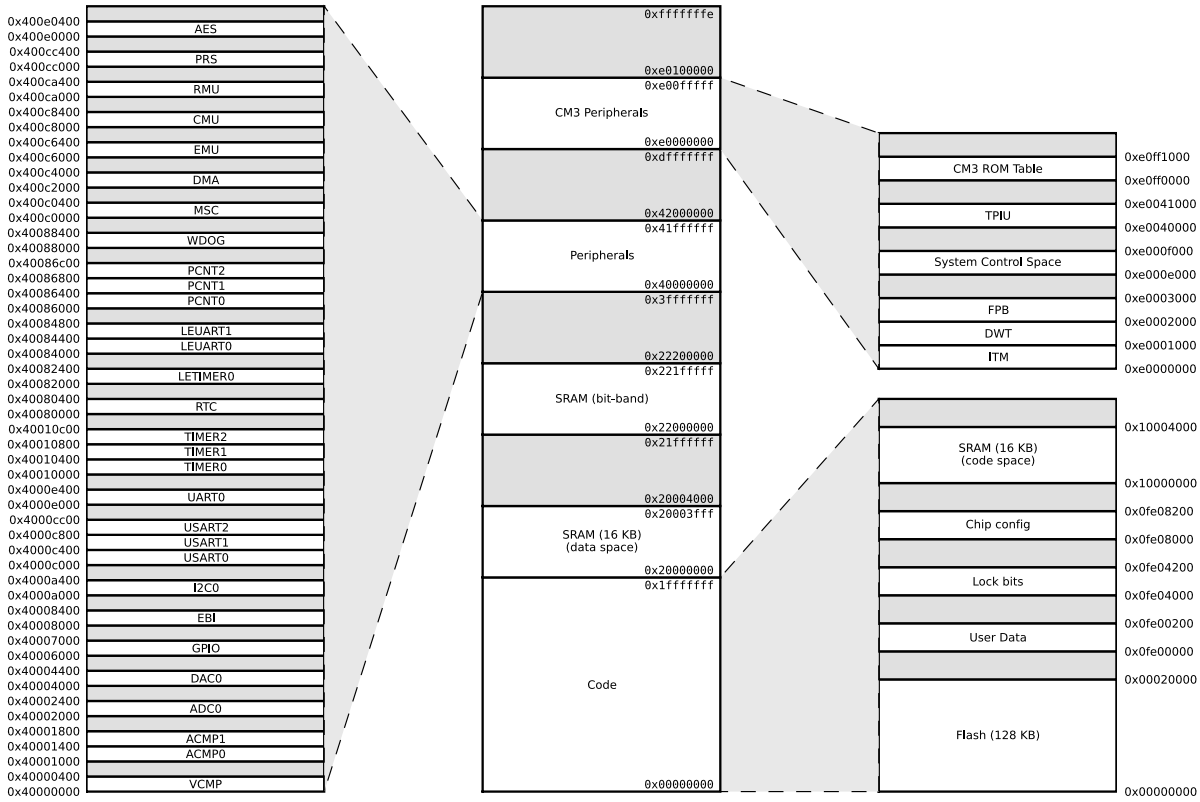
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWV
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	No IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	No IrDA	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	No DTI	TIM1_CC[2:0]
TIMER2	No DTI	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	8-bit count register	PCNT0_S[1:0]

Module	Configuration	Pin Connections
PCNT1	8-bit count register	PCNT1_S[1:0]
PCNT2	8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0], ADC0_VCM
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	85 pins	Available pins are shown in Table 4.2 (p. 34)

2.3 Memory Map

The *EFM32G280* memory map is shown in Figure 2.1 (p. 7), with RAM and Flash sizes for the largest memory configuration.

Figure 2.1. EFM32G280 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Introduction

Unless otherwise specified data in this chapter is preliminary and subject to change without further notice.

3.1.2 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.1.3 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		85	°C
T_J	Maximum junction temperature	JEDEC J-STD-020D			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40	25	85	°C
V_{DDOP}	Operating supply voltage	1.8	3.0	3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2	kV
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			500	V
MSL	Moisture sensitivity level	JEDEC J-STD-20D. Level 3			168	hrs
LU	Latchup sensitivity	JESD78 Latchup test procedure. Class II level A.			85	°C

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running code from Flash.	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		180		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		190	240	µA/MHz
		32 MHz HFXO, all peripheral clocks enabled, V_{DD}= 3.0 V		TBD		µA/MHz
		14 MHz HFRCO. all peripheral clocks enabled.		TBD		µA/MHz
		1 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		220		µA/MHz
I_{EM1}	EM1 current	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		45		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		48	55	µA/MHz
		1 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V		103		µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC at 1 Hz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.9		µA
		EM2 current with RTC at 1 Hz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		1.7	3.6	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.59		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		1.27	2.7	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.12	0.5	µA

Figure 3.1. EM0 Current consumption vs supply voltage, executing code from flash with HFRCO running at 28MHz

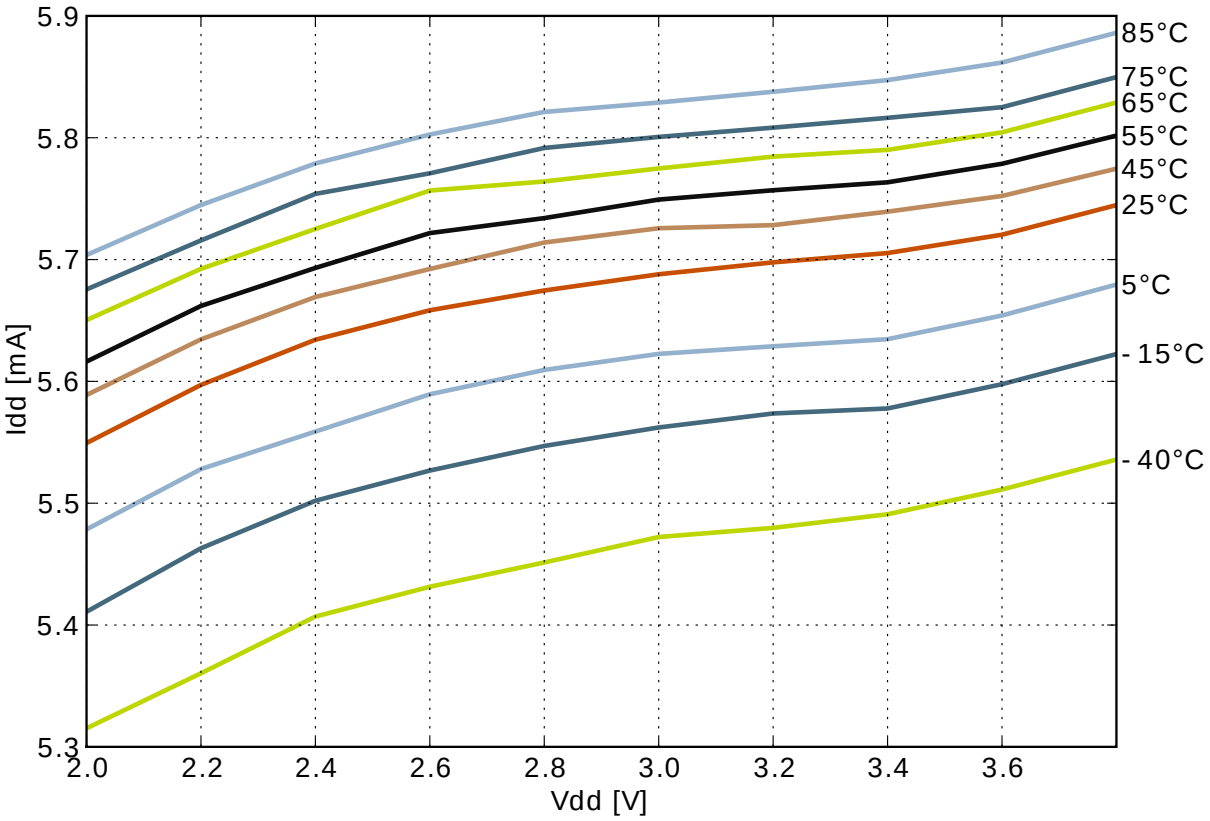


Figure 3.2. EM0 Current consumption vs temperature, executing code from flash with HFRCO running at 28MHz

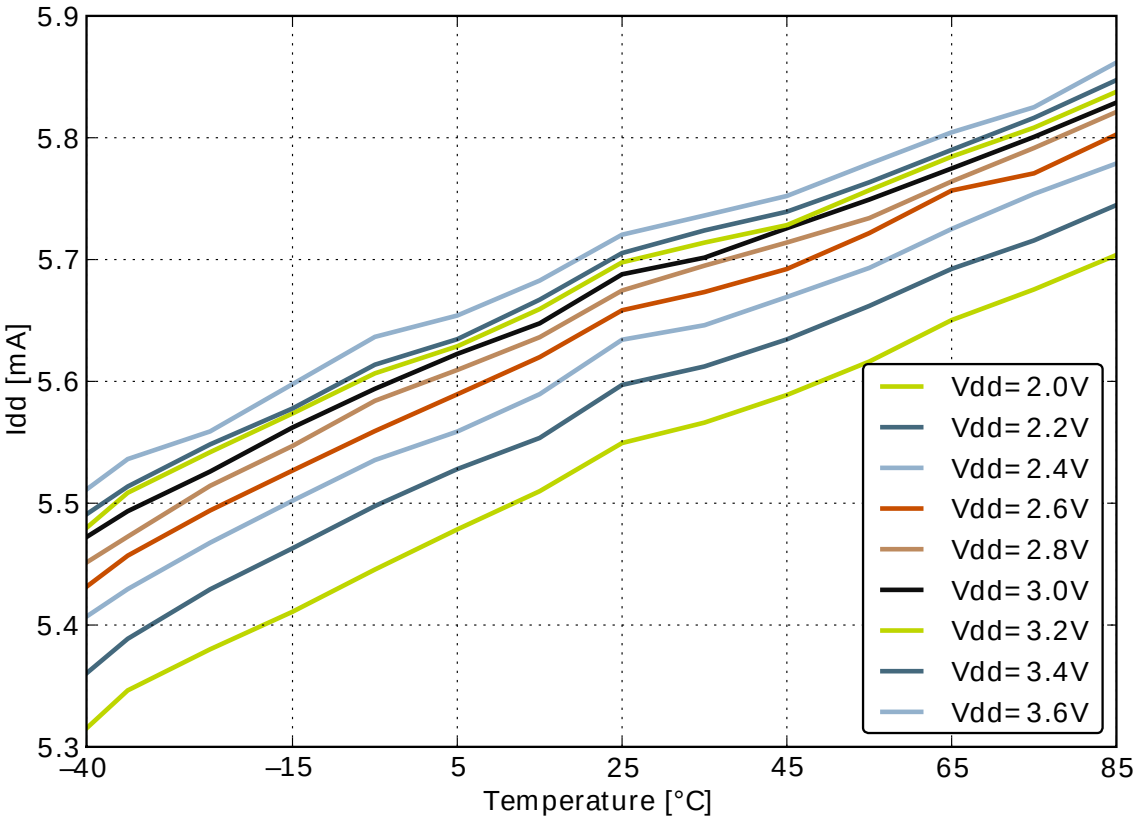


Figure 3.3. EM1 Current consumption vs supply voltage, all peripheral clocks disabled, HFRCO running at 28MHz

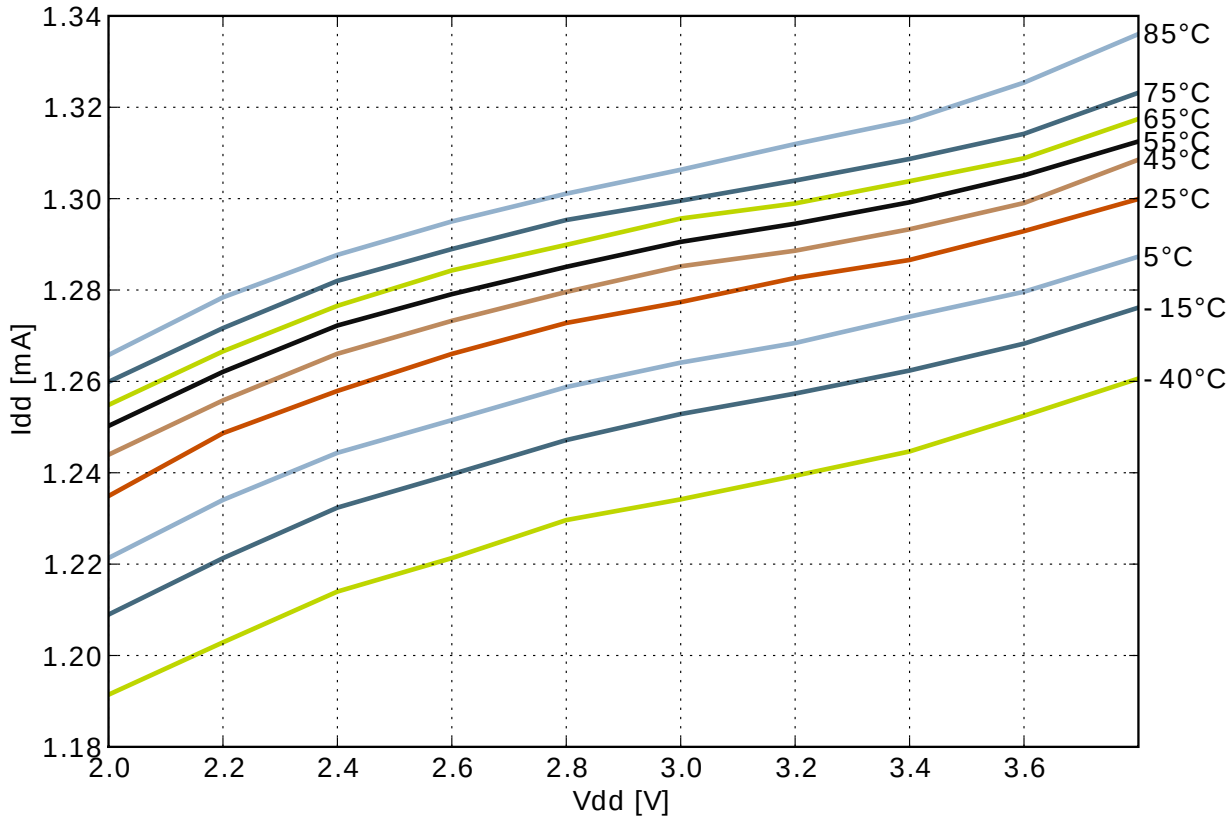


Figure 3.4. EM1 Current consumption vs temperature, all peripheral clocks disabled, HFRCO running at 28MHz

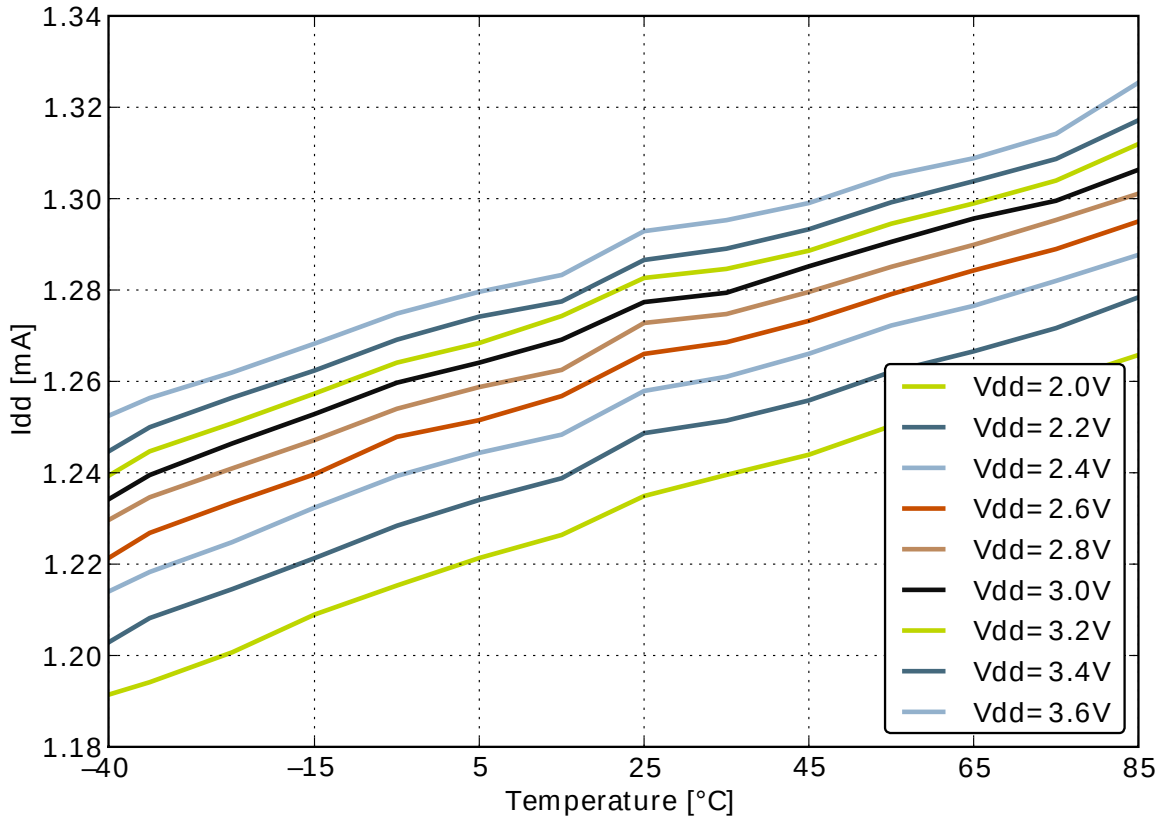


Figure 3.5. EM2 Current consumption vs supply voltage

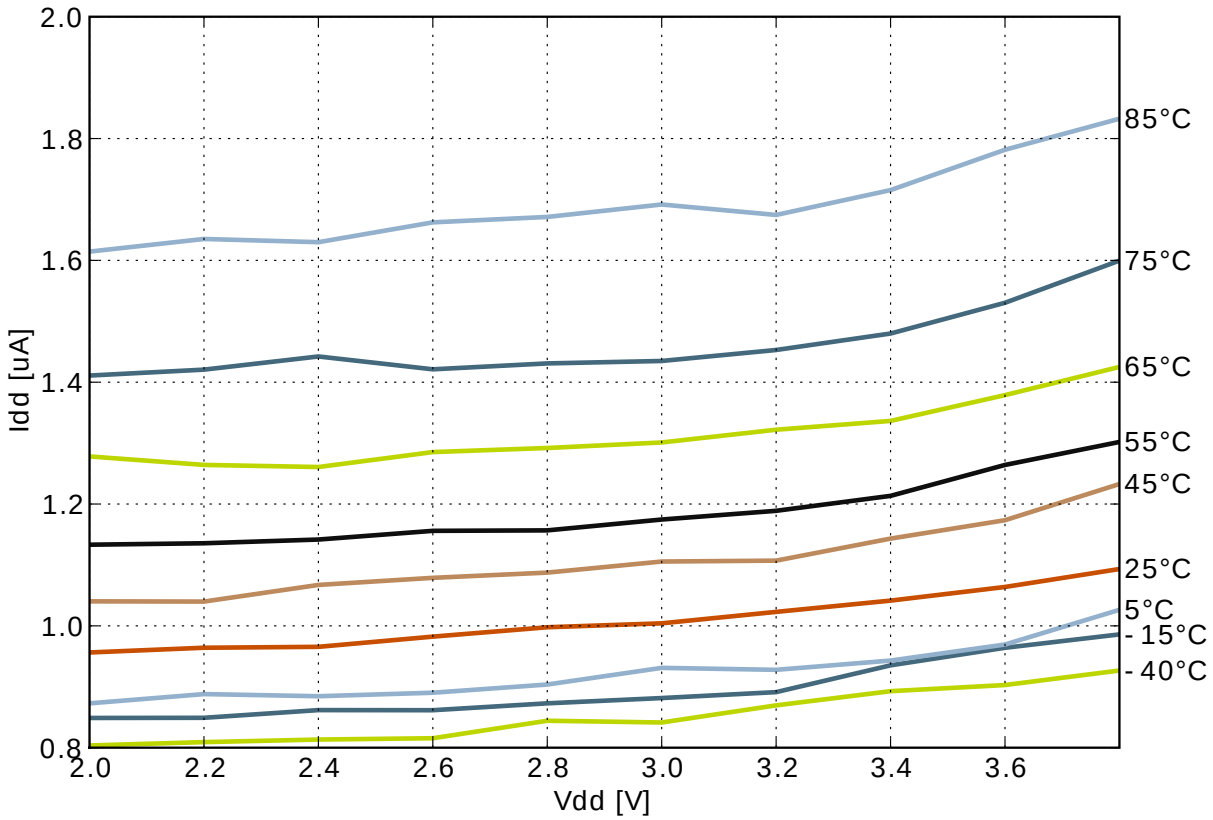


Figure 3.6. EM2 Current consumption vs temperature

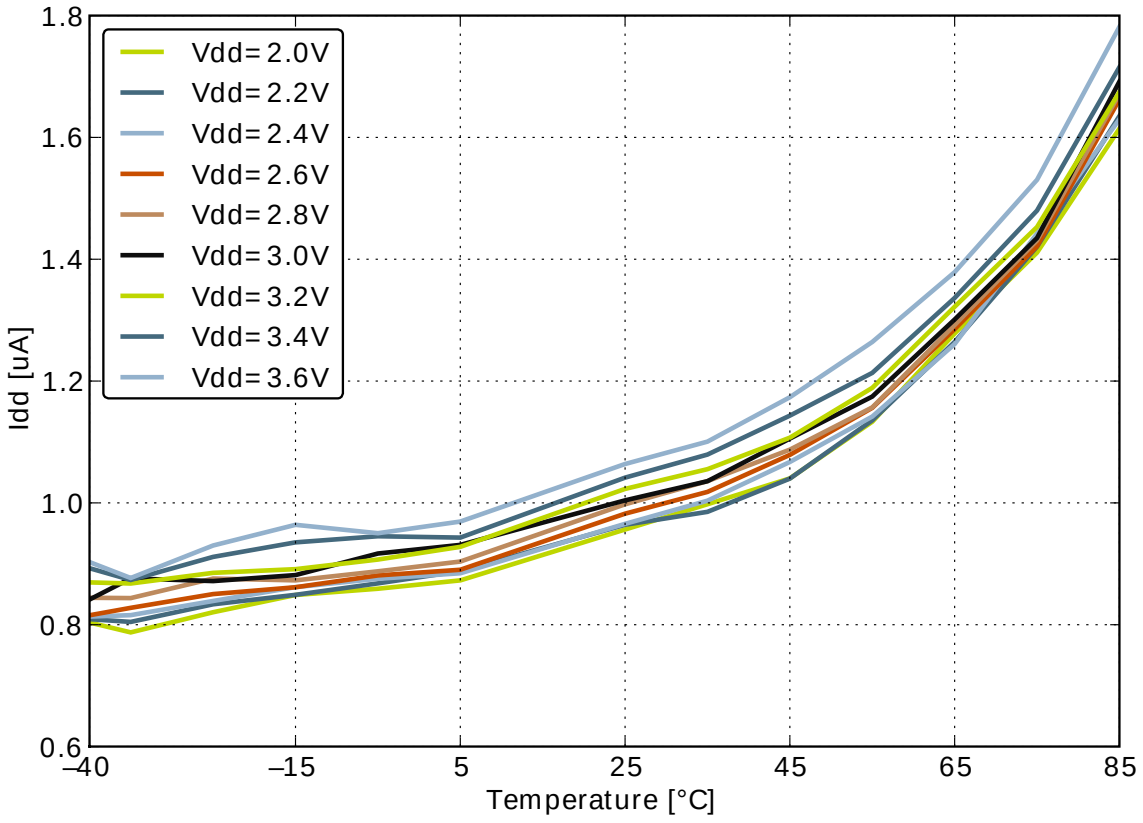


Figure 3.7. EM3 Current consumption vs supply voltage

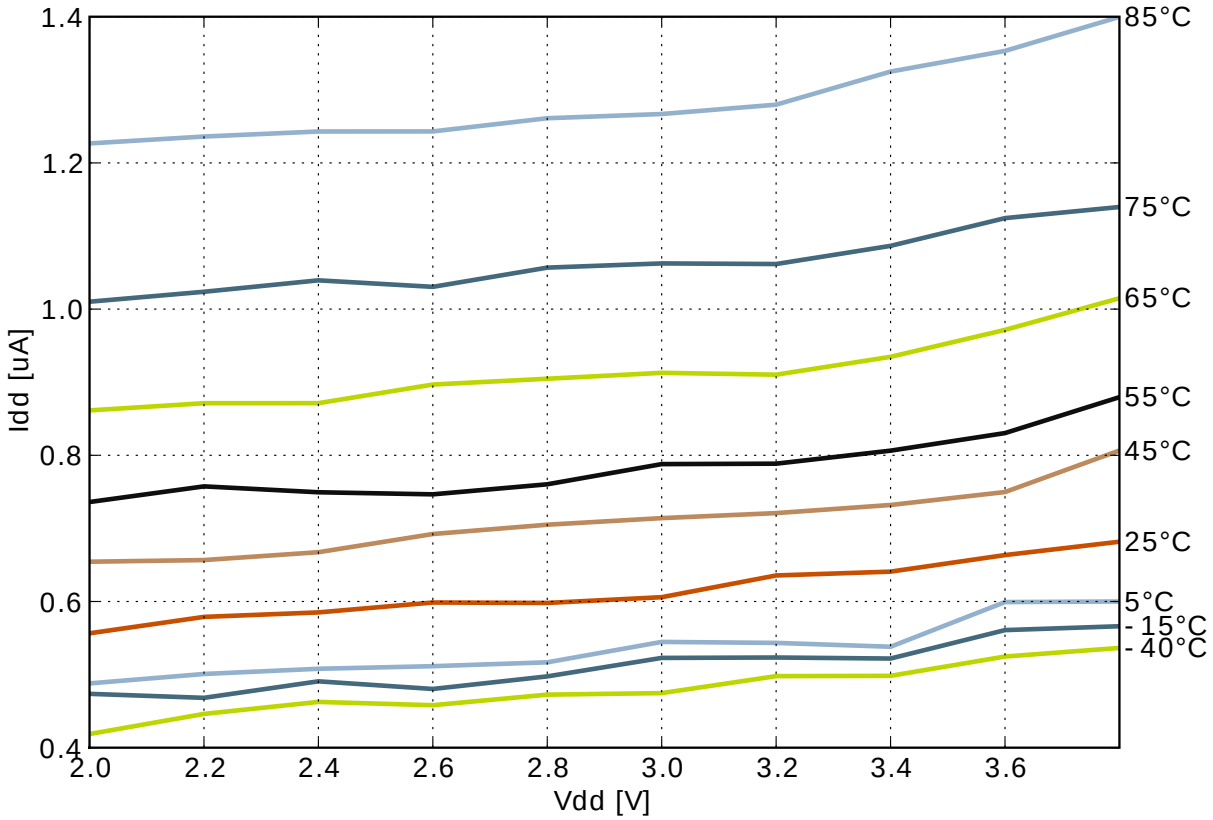


Figure 3.8. EM3 Current consumption vs temperature

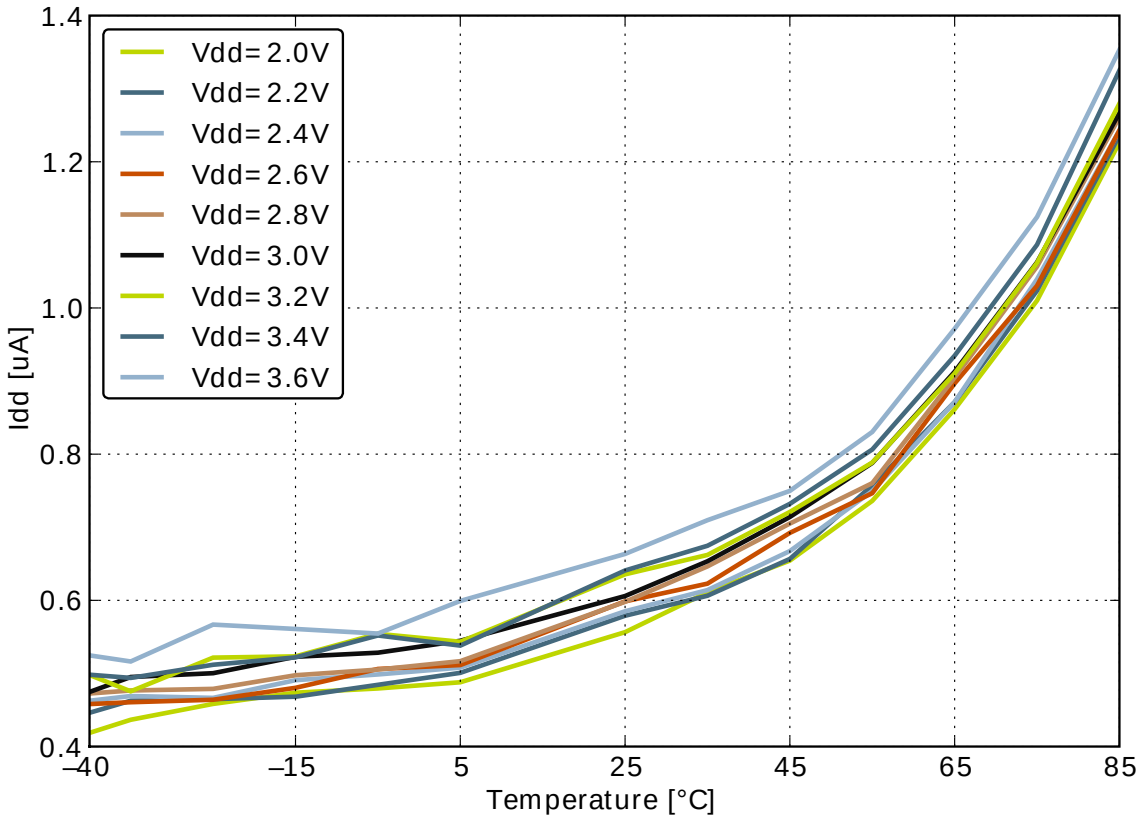


Figure 3.9. EM4 Current consumption vs supply voltage

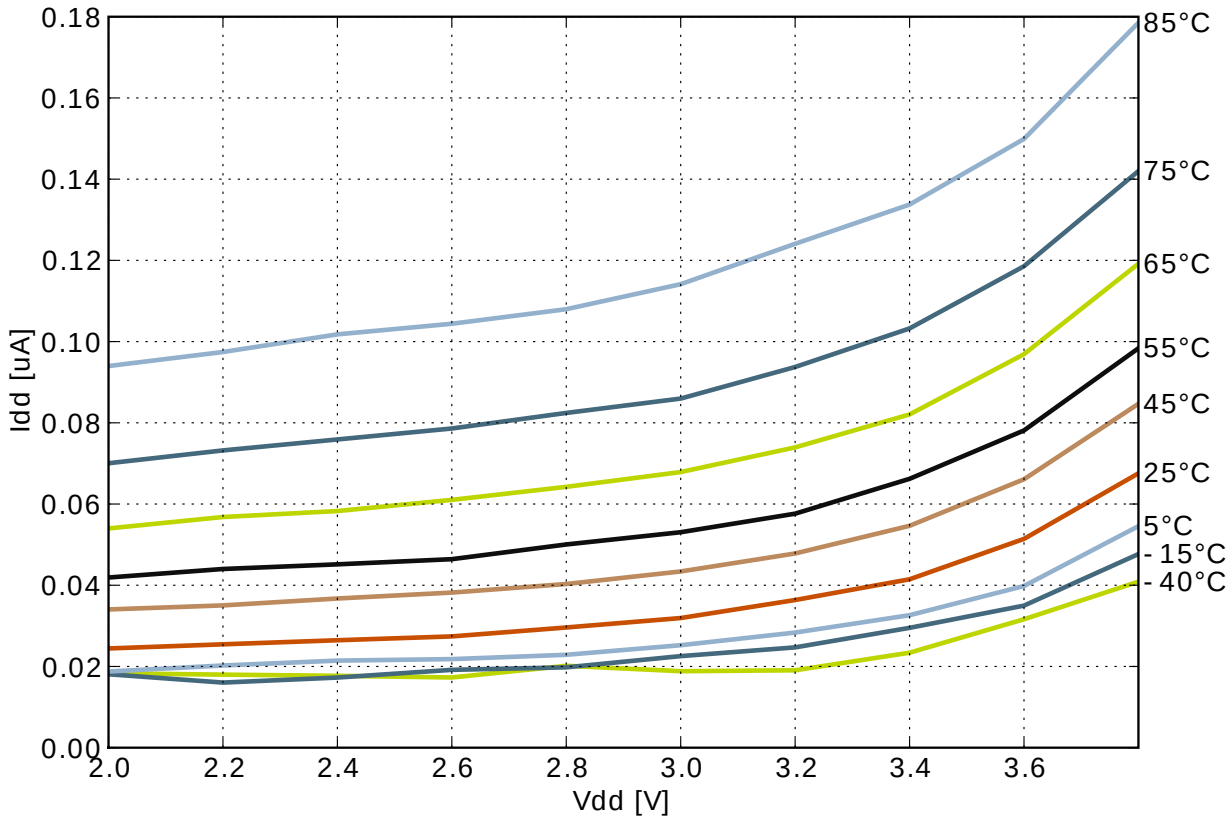
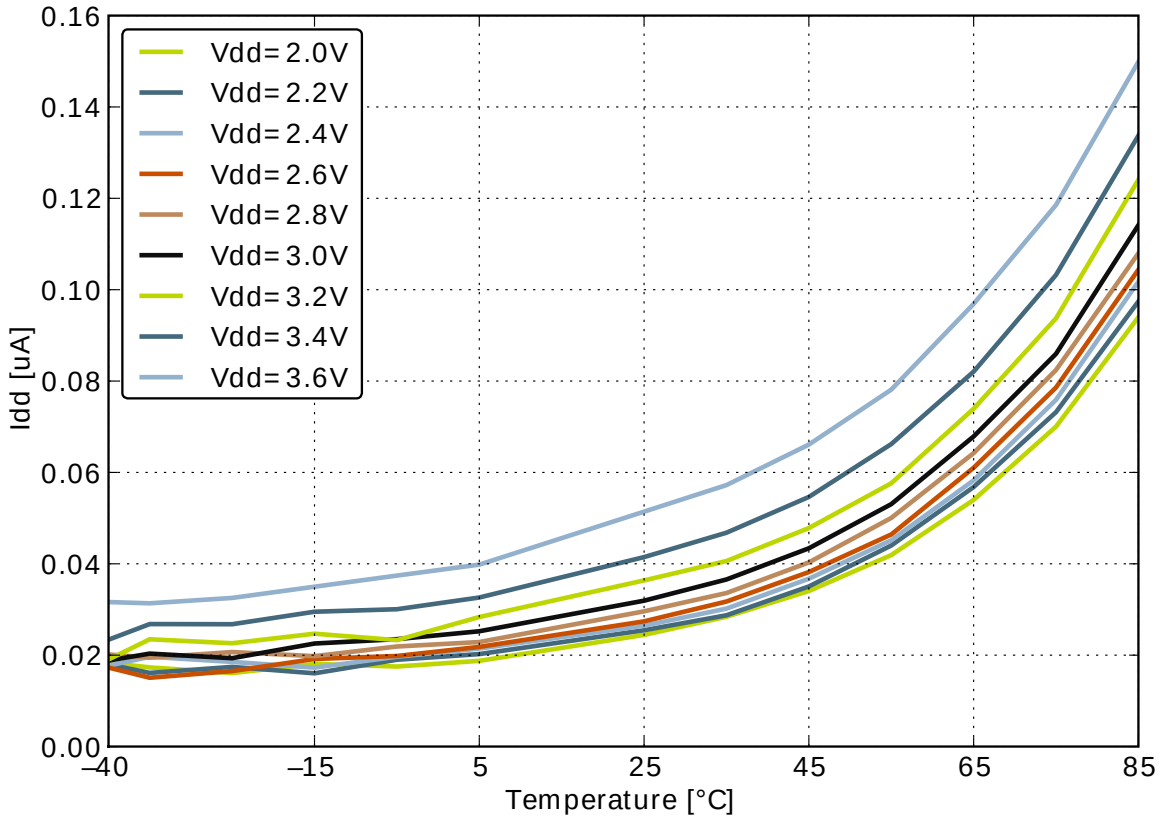


Figure 3.10. EM4 Current consumption vs temperature



3.5 Transition between Energy Modes

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0			0[1]		HF core CLK cycles
t_{EM20}	Transition time from EM2 to EM0			2		µs
t_{EM30}	Transition time from EM3 to EM0			2		µs
t_{EM40}	Transition time from EM4 to EM0			163		µs

[1]Core wakeup time only.

3.6 Power Management

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.77		1.80	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.62		1.65	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage	Uncalibrated		1.82		V
$V_{BODexthyst}$	BOD hysteresis on external supply voltage			150		mV
TC_{BGR}	Temperature coefficient of band-gap reference (BGR)	Relative voltage variation in EM0 based on the difference in V_{ref} between -40°C and 85°C.			0.55	%
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<85°C	10			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{P_ERASE}	Page erase time		20	20.4	20.8	ms
t_{D_ERASE}	Device erase time		40	40.8	41.6	ms

3.8 General Purpose Input Output

Table 3.8. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				$0.3V_{DD}$	V
V_{IOIH}	Input high voltage		$0.7V_{DD}$			V
V_{IOOH}	Output high voltage relative to V_{DD}	Sourcing 6 mA, V_{DD}=1.8V	75			%
		Sourcing 6 mA, V_{DD}=3.0V	95			%
		Sourcing 20 mA, V_{DD}=1.8V	70			%
		Sourcing 20 mA, V_{DD}=3.0V	90			%
V_{IOOL}	Output low voltage relative to V_{DD}	Sinking 6 mA, V_{DD}=1.8V			25	%
		Sinking 6 mA, V_{DD}=3.0V			5	%
		Sinking 20 mA, V_{DD}=1.8V			30	%
		Sinking 20 mA, V_{DD}=3.0V			10	%
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	0.5 mA drive strength and load capacitance C_L=12.5-25pF.	$20+0.1C_L$		250	ns
		2mA drive strength and load capacitance C_L=350-600pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.8 - 3.8 V	$0.1V_{DD}$			V

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after start-up.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

3.9.2 HFXO

Table 3.10. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.9.3 LFRCO

Table 3.11. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			190		nA

3.9.4 HFRCO

Table 3.12. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency	28 MHz frequency band		28		MHz
		21 MHz frequency band		21		MHz
		14 MHz frequency band		14		MHz
		11 MHz frequency band		11		MHz
		7 MHz frequency band		7		MHz
		1 MHz frequency band		1		MHz
t_{HFRCO}	Start-up time not including software calibration	f_{HFRCO} = 14 MHz		0.6		µs
I_{HFRCO}	Current consumption	f_{HFRCO} = 28 MHz		106		µA
		f_{HFRCO} = 21 MHz		93		µA
		f_{HFRCO} = 14 MHz		77		µA
		f_{HFRCO} = 11 MHz		72		µA
		f_{HFRCO} = 7 MHz		63		µA
DC_{HFRCO}	Duty cycle	f_{HFRCO} = 14 MHz	48.5	50	51	%

3.10 Analog Digital Converter (ADC)

Table 3.13. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCCM}	Analog input common mode voltage range		0		V_{DD}	V
V_{ADCIN}	Input voltage range of external reference voltage, single ended and differential		1.25		V_{DD}	V
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		220		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00		9		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01		6		µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		74		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		290		µA
		6 bit 10 kSamples/s, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		4		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		70		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$V_{ADCCMOUT}$	Common mode output voltage range			1.65		V
f_{ADCCLK}	Frequency of ADC clock, max and min			13		MHz
$t_{ADCCONV}$	Conversion time			1		µs
t_{ADCACQ}	Acquisition time	Programmable		0.5		µs
$t_{ADCACQVDD3}$	Required sample time for VDD/3 reference			2		µs
$t_{ADCSTART}$	Startup time of reference generator in NORMAL mode and startup time ADC			5		µs
	Startup time of reference generator in KEEPADCWARM mode and startup time ADC			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		69		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		72		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		70		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		1 MSamples/s, 12 bit, differential, 5V reference		73		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		69		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		72		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		70		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		100 kSamples/s, 12 bit, differential, 5V reference		73		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		37		dB
$SNDR_{ADC}$	Signal to Noise-puls-Distortion Ratio (SNDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		68		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		69		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		1 MSamples/s, 12 bit, differential, 5V reference		72		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		68		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		69		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		100 kSamples/s, 12 bit, differential, 5V reference		72		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		37		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		75		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, 5V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, 5V reference		75		dB
		1.86 MSamples/s, 6 bit, single ended, internal 1.25V reference		57		dB
$V_{ADCOFFSET}$	Offset voltage	Before calibration, single ended		10		mV
		After calibration, single ended		0.3		mV
		Before calibration, differential		10		mV
		After calibration, differential		0.3		mV
DNL_{ADC}	Differential non-linearity (DNL)	Internal 1.25V reference		1		LSB
		Internal 2.5V reference		1		LSB
		Internal 5V reference		1		LSB
INL_{ADC}	Integral non-linearity (INL), End point method	Internal 1.25V reference		2		LSB
		Internal 2.5V reference		2		LSB
		Internal 5V reference		2		LSB
MC_{ADC}	No missing codes	12 bit, internal 1.25V reference, single ended		0		
		12 bit, internal 1.25V reference, differential		0		
		12 bit, internal 2.5V reference, single ended		0		
		12 bit, internal 2.5V reference, differential		0		
		12 bit, internal 5V reference, differential		0		

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.11 (p. 24) and Figure 3.12 (p. 24) , respectively.

Figure 3.11. Integral Non-Linearity (INL)

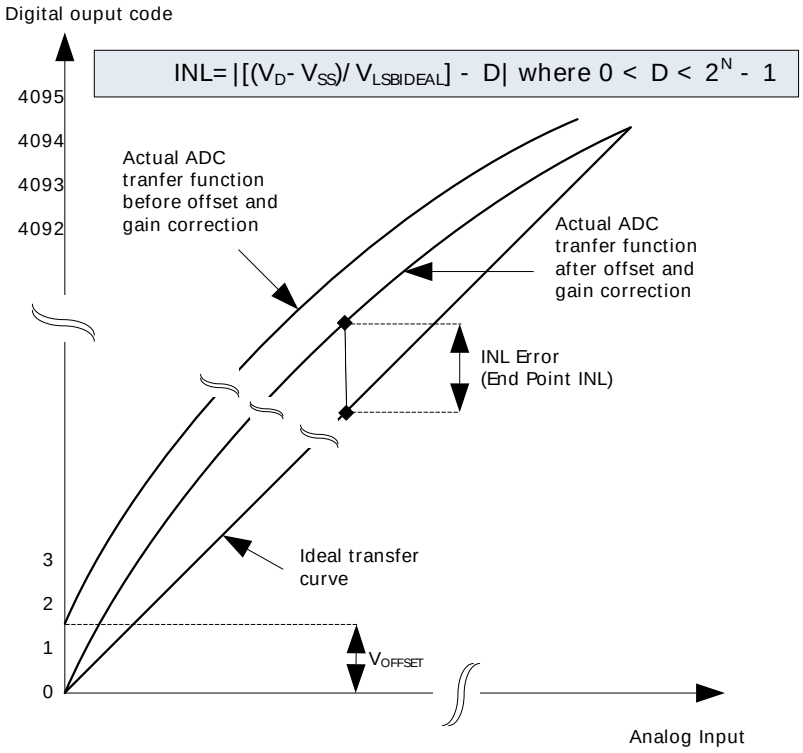
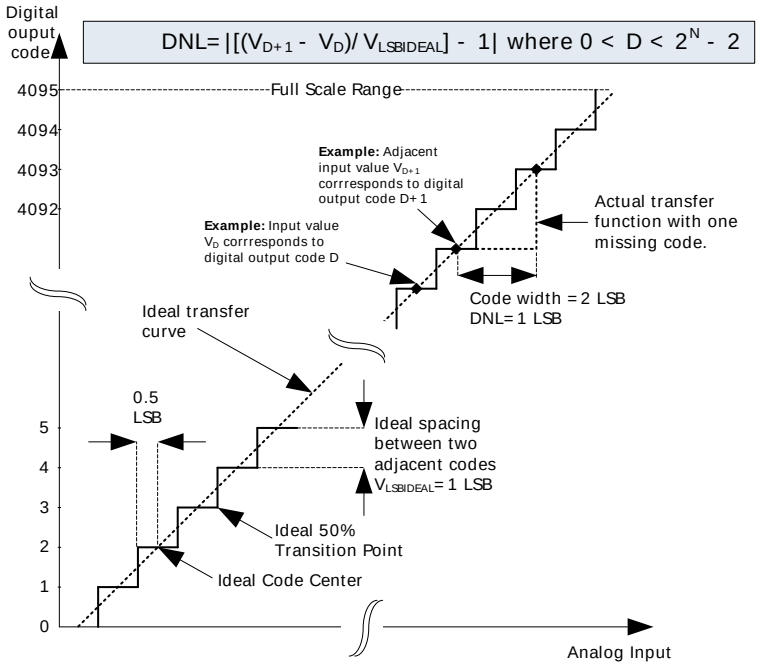


Figure 3.12. Differential Non-Linearity (DNL)



3.11 Digital Analog Converter (DAC)

Table 3.14. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	External voltage reference, single ended	0		V_{DD}	V
		External voltage reference, differential	0		V_{DD}	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12bit		400		µA
		100 kSamples/s, 12 bit		200		µA
		1 kSamples/s 12 bit NORMAL		38		µA
f_{DAC}	DAC clock frequency			0.5		MHz
$t_{DACCONV}$	DAC conversion time			2		µs
$t_{DACSETTLE}$	DAC settling time			5		µs
SNR_{DAC}	DAC Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		71		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		70		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		73		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		500 kSamples/s, 12 bit, differential, 5V reference		72		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		72		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		71		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		73		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		73		dB
		100 kSamples/s, 12 bit, differential, 5V reference		73		dB
$SNDR_{DAC}$	DAC Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		70		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		69		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		72		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		71		dB
		500 kSamples/s, 12 bit, differential, 5V reference		71		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		71		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		70		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		72		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		72		dB
		100 kSamples/s, 12 bit, differential, 5V reference		72		dB
$SFDR_{DAC}$	DAC Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		500 kSamples/s, 12 bit, differential, 5V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 1.25V reference		75		dB
		100 kSamples/s, 12 bit, differential, internal 2.5V reference		75		dB
		100 kSamples/s, 12 bit, differential, 5V reference		75		dB
$V_{DACOFFSET}$	Offset voltage	Before calibration, single ended		10		mV
		Before calibration, differential		10		mV
		After calibration, single ended		0.5		mV
		After calibration, differential		0.5		mV
DNL_{DAC}	Differential non-linearity	Internal 1.25V reference		1		LSB
		Internal 2.5V reference		1		LSB
		5V reference		1		LSB
INL_{DAC}	Integral non-linearity	Internal 1.25V reference		2		LSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Internal 2.5V reference		2		LSB
		5V reference		2		LSB
MC_{DAC}	No missing codes	12 bit, internal 1.25V reference, single ended		0		
		12 bit, internal 1.25V reference, differential		0		
		12 bit, internal 2.5V reference, single ended		0		
		12 bit, internal 2.5V reference, differential		0		
		12 bit, internal 5V reference, differential		0		

3.12 Analog Comparator (ACMP)

Table 3.15. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1		µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87		µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195		µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 28) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

3.13 Voltage Comparator (VCMP)

Table 3.16. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1		µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register		2.7		µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level} = 1.667V + 0.034 \times TRIGLEVEL \quad (3.2)$$

3.14 Digital Peripherals

Table 3.17. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		TBD		µA/MHz
		USART transmit current		TBD		µA/MHz
I_{UART}	UART current	UART idle current, clock enabled		TBD		µA/MHz
		UART transmit current		TBD		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		TBD		µA
		LEUART transmit current		TBD		µA
I_{I2C}	I2C current	I2C idle current, clock enabled		TBD		µA/MHz
		I2C transmit current		TBD		µA/MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		TBD		µA/ MHz
		TIMER_n (n>0) idle current, clock enabled		TBD		µA/ MHz
		TIMER counting current, counter enabled		TBD		µA/ MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		TBD		µA
		LETIMER counting current, counter enabled		TBD		µA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		TBD		µA
		PCNT Count Current, counter enabled		TBD		µA
I_{RTC}	RTC current	RTC idle current, clock enabled		TBD		µA
		RTC counting current, counter enabled		TBD		µA
I_{WDOG}	WDOG current	WDOG idle current, clock enabled		TBD		µA
		WDOG counting current, counter enabled		TBD		µA
I_{AES}	AES current	AES idle current, clock enabled		TBD		µA/ MHz
		AES-128 encryption/decryption current		TBD		µA/ MHz
		AES-256 encryption/decryption current		TBD		µA/ MHz
I_{EBI}	EBI current	EBI idle current, clock enabled		TBD		µA/ MHz
I_{PRS}	PRS current	PRS idle current		TBD		µA/ MHz
I_{DMA}	DMA current	Clock enable		TBD		µA/ MHz

4 Pinout and Package

4.1 Pinout

The *EFM32G280* pinout is shown in Table 4.1 (p. 30). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Table 4.1. Device Pinout

LQFP100 Pin# and Name		Pin Functionality								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
1	PA0	-	-	EBI_AD09 #0	TIM0_CC0 #0/1	-	-	I2C0_SDA #0	-	-
2	PA1	-	-	EBI_AD10 #0	TIM0_CC1 #0/1	-	-	I2C0_SCL #0	-	CMU_OUT1 #0
3	PA2	-	-	EBI_AD11 #0	TIM0_CC2 #0/1	-	-	-	-	CMU_OUT0 #0
4	PA3	-	-	EBI_AD12 #0	TIM0_CDTI0 #0	-	-	U0_TX #2	-	-
5	PA4	-	-	EBI_AD13 #0	TIM0_CDTI1 #0	-	-	U0_RX #2	-	-
6	PA5	-	-	EBI_AD14 #0	TIM0_CDTI2 #0	-	-	LEU1_TX #1	-	-
7	PA6	-	-	EBI_AD15 #0	-	-	-	LEU1_RX #1	-	-
8	IOVDD_0	-	-	-	-	-	-	-	-	-
9	PB0	-	-	-	TIM1_CC0 #2	-	-	-	-	-
10	PB1	-	-	-	TIM1_CC1 #2	-	-	-	-	-
11	PB2	-	-	-	TIM1_CC2 #2	-	-	-	-	-
12	PB3	-	-	-	PCNT1_S0IN #1	-	-	US2_TX #1	-	-
13	PB4	-	-	-	PCNT1_S1IN #1	-	-	US2_RX #1	-	-
14	PB5	-	-	-	-	-	-	US2_CLK #1	-	-
15	PB6	-	-	-	-	-	-	US2_CS #1	-	-
16	VSS	-	-	-	-	-	-	-	-	-
17	IOVDD_1	-	-	-	-	-	-	-	-	-
18	PC0	ACMP0_CH0	-	-	PCNT0_S0IN #2	-	-	US1_TX #0	-	-
19	PC1	ACMP0_CH1	-	-	PCNT0_S1IN #2	-	-	US1_RX #0	-	-
20	PC2	ACMP0_CH2	-	-	-	-	-	US2_TX #0	-	-
21	PC3	ACMP0_CH3	-	-	-	-	-	US2_RX #0	-	-
22	PC4	ACMP0_CH4	-	-	LETIM0_OUT0 #3	PCNT1_S0IN #0	-	US2_CLK #0	-	-

LQFP100 Pin# and Name		Pin Functionality								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
23	PC5	ACMP0_CH5	-	-	LETIM0_OUT1 #3	PCNT1_S1IN #0	-	US2_CS #0	-	-
24	PB7	LFXTAL_P	-	-	-	-	-	US1_CLK #0	-	-
25	PB8	LFXTAL_N	-	-	-	-	-	US1_CS #0	-	-
26	PA7	-	-	-	-	-	-	-	-	-
27	PA8	-	-	-	TIM2_CC0 #0	-	-	-	-	-
28	PA9	-	-	-	TIM2_CC1 #0	-	-	-	-	-
29	PA10	-	-	-	TIM2_CC2 #0	-	-	-	-	-
30	PA11	-	-	-	-	-	-	-	-	-
31	IOVDD_2	-	-	-	-	-	-	-	-	-
32	VSS	-	-	-	-	-	-	-	-	-
33	PA12	-	-	-	TIM2_CC0 #1	-	-	-	-	-
34	PA13	-	-	-	TIM2_CC1 #1	-	-	-	-	-
35	PA14	-	-	-	TIM2_CC2 #1	-	-	-	-	-
36	RESETn	-	-	-	-	-	-	-	-	-
37	PB9	-	-	-	-	-	-	-	-	-
38	PB10	-	-	-	-	-	-	-	-	-
39	PB11	DAC0_OUT0	-	-	LETIM0_OUT0 #1	-	-	-	-	-
40	PB12	DAC0_OUT1	-	-	LETIM0_OUT1 #1	-	-	-	-	-
41	AVDD_1	-	-	-	-	-	-	-	-	-
42	PB13	HFXTAL_P	-	-	-	-	-	LEU0_TX #1	-	-
43	PB14	HFXTAL_N	-	-	-	-	-	LEU0_RX #1	-	-
44	IOVDD_3	-	-	-	-	-	-	-	-	-
45	AVDD_0	-	-	-	-	-	-	-	-	-
46	PD0	ADC0_CH0	-	-	PCNT2_S0IN #0	-	-	US1_TX #1	-	-
47	PD1	ADC0_CH1	-	-	TIM0_CC0 #3	PCNT2_S1IN #0	-	US1_RX #1	-	-
48	PD2	ADC0_CH2	-	-	TIM0_CC1 #3	-	-	US1_CLK #1	-	-
49	PD3	ADC0_CH3	-	-	TIM0_CC2 #3	-	-	US1_CS #1	-	-
50	PD4	ADC0_CH4	-	-	-	-	-	LEU0_TX #0	-	-
51	PD5	ADC0_CH5	-	-	-	-	-	LEU0_RX #0	-	-

LQFP100 Pin# and Name		Pin Functionality								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
52	PD6	ADC0_CH6	-	-	LETIM0_OUT0 #0	-	-	I2C0_SDA #1	-	-
53	PD7	ADC0_CH7	-	-	LETIM0_OUT1 #0	-	-	I2C0_SCL #1	-	-
54	PD8	ADC0_VCM	-	-	-	-	-	-	-	CMU_OUT1 #1
55	PC6	ACMP0_CH6	-	-	-	-	-	LEU1_TX #0	I2C0_SDA #2	-
56	PC7	ACMP0_CH7	-	-	-	-	-	LEU1_RX #0	I2C0_SCL #2	-
57	VDD_DREG	-	-	-	-	-	-	-	-	-
58	VSS	-	-	-	-	-	-	-	-	-
59	DECOUPLE	-	-	-	-	-	-	-	-	-
60	PE0	-	-	-	PCNT0_S0IN #1	-	-	U0_TX #1	-	-
61	PE1	-	-	-	PCNT0_S1IN #1	-	-	U0_RX #1	-	-
62	PE2	-	-	-	-	-	-	-	-	ACMP0_O #1
63	PE3	-	-	-	-	-	-	-	-	ACMP1_O #1
64	PE4	-	-	-	-	-	-	US0_CS #1	-	-
65	PE5	-	-	-	-	-	-	US0_CLK #1	-	-
66	PE6	-	-	-	-	-	-	US0_RX #1	-	-
67	PE7	-	-	-	-	-	-	US0_TX #1	-	-
68	PC8	ACMP1_CH0	-	-	TIM2_CC0 #2	-	-	US0_CS #2	-	-
69	PC9	ACMP1_CH1	-	-	TIM2_CC1 #2	-	-	US0_CLK #2	-	-
70	PC10	ACMP1_CH2	-	-	TIM2_CC2 #2	-	-	US0_RX #2	-	-
71	PC11	ACMP1_CH3	-	-	-	-	-	US0_TX #2	-	-
72	PC12	ACMP1_CH4	-	-	-	-	-	-	-	CMU_OUT0 #1
73	PC13	ACMP1_CH5	-	-	TIM0_CDTI0 #1/3	TIM1_CC0 #0	PCNT0_S0IN #0	-	-	-
74	PC14	ACMP1_CH6	-	-	TIM0_CDTI1 #1/3	TIM1_CC1 #0	PCNT0_S1IN #0	U0_TX #3	-	-
75	PC15	ACMP1_CH7	DBG_SWV #1	-	TIM0_CDTI2 #1/3	TIM1_CC2 #0	-	U0_RX #3	-	-
76	PF0	-	DBG_SWCLK #0/1	-	LETIM0_OUT0 #2	-	-	-	-	-
77	PF1	-	DBG_SWDIO #0/1	-	LETIM0_OUT1 #2	-	-	-	-	-
78	PF2	-	DBG_SWV #0	EBI_ARDY #0	-	-	-	-	-	ACMP1_O #0
79	PF3	-	-	EBI_ALE #0	TIM0_CDTI0 #2	-	-	-	-	-

LQFP100 Pin# and Name		Pin Functionality								
Pin #	Pin Name	Analog	Debug	EBI	Timers			Communication		Other
80	PF4	-	-	EBI_WEn #0	TIM0_CDTI1 #2	-	-	-	-	-
81	PF5	-	-	EBI_REn #0	TIM0_CDTI2 #2	-	-	-	-	-
82	IOVDD_5	-	-	-	-	-	-	-	-	-
83	VSS	-	-	-	-	-	-	-	-	-
84	PF6	-	-	-	TIM0_CC0 #2	-	-	U0_TX #0	-	-
85	PF7	-	-	-	TIM0_CC1 #2	-	-	U0_RX #0	-	-
86	PF8	-	-	-	TIM0_CC2 #2	-	-	-	-	-
87	PF9	-	-	-	-	-	-	-	-	-
88	PD9	-	-	EBI_CS0 #0	-	-	-	-	-	-
89	PD10	-	-	EBI_CS1 #0	-	-	-	-	-	-
90	PD11	-	-	EBI_CS2 #0	-	-	-	-	-	-
91	PD12	-	-	EBI_CS3 #0	-	-	-	-	-	-
92	PE8	-	-	EBI_AD00 #0	PCNT2_S0IN #1	-	-	-	-	-
93	PE9	-	-	EBI_AD01 #0	PCNT2_S1IN #1	-	-	-	-	-
94	PE10	-	-	EBI_AD02 #0	TIM1_CC0 #1	-	-	US0_TX #0	-	-
95	PE11	-	-	EBI_AD03 #0	TIM1_CC1 #1	-	-	US0_RX #0	-	-
96	PE12	-	-	EBI_AD04 #0	TIM1_CC2 #1	-	-	US0_CLK #0	-	-
97	PE13	-	-	EBI_AD05 #0	-	-	-	US0_CS #0	-	ACMP0_O #0
98	PE14	-	-	EBI_AD06 #0	-	-	-	LEU0_TX #2	-	-
99	PE15	-	-	EBI_AD07 #0	-	-	-	LEU0_RX #2	-	-
100	PA15	-	-	EBI_AD08 #0	-	-	-	-	-	-

4.2 GPIO pinout overview

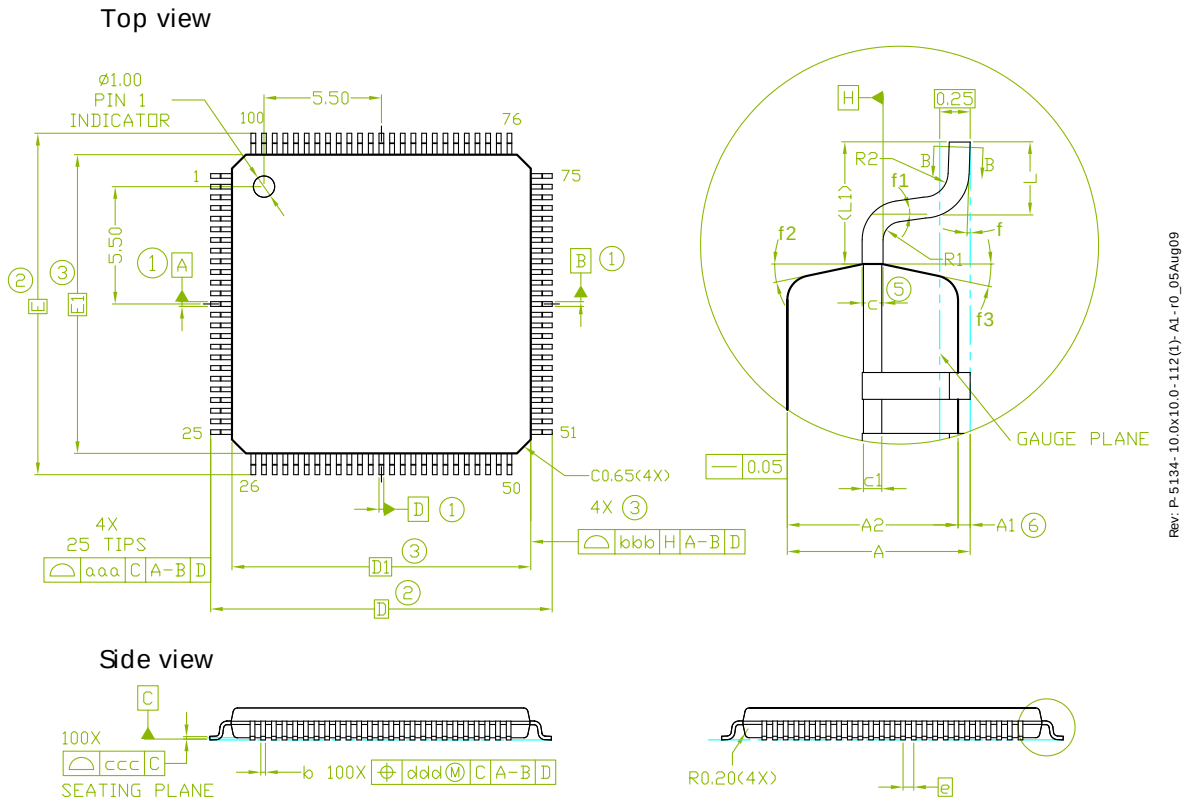
The specific GPIO pins available in *EFM32G280* is shown in Table 4.2 (p. 34). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 4.2. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.3 LQFP100 Package

Figure 4.1. LQFP100



1. Datum 'A', 'B' and 'D' to determine at datum plane 'H'.
2. To be determined at seating datum plan 'C'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 mm per side. 'S1' and 'E1' are maximum plastic body size dimension including mold mismatch.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch package.
5. These dimensions apply to the flat section between 0.10 mm and 0.25 mm from the lead tip.
6. 'A1' is defined as the distance from the seating plan to the lowest point on the package body.
7. Package dimensions conform to JEDEC MS-026 rev. D.

Table 4.3. LQFP100 (Dimensions in mm)

Symbol	A	A1	A2	b	b1	D	D1	e	E	E1	f	f1
Min	-	0.05	1.35	0.17	0.17						0°	0°
Nom	-	-	1.40	0.22	0.20	16.00	14.00	0.50	16.00	14.00	3.5°	-
Max	1.60	0.15	1.45	0.27	0.23						7°	-
Symbol	**f2**	**f3**	**c**	**c1**	**L**	**L1**	**R1**	**R2**	**aaa**	**bbb**	**ccc**	**ddd**
Min	11°	11°	0.09	0.09	0.45		0.08	0.08				
Nom	12°	12°	-	-	0.60	1.00	-	-	0.20	0.20	0.10	0.08
Max	13°	13°	0.20	0.16	0.75		-	0.20				

5 Errata

5.1 Introduction

This chapter describes the identified errata of the device including fixes and workaraounds for these.

5.2 Device revision A

5.2.1 BOD threshold too high

Problem

The Brown-Out Detector (BOD) threshold voltage is calibrated to a too high value.

Effect

The high BOD threshold voltage may create sporadic BOD resets while the EFM32 is running in Energy Mode 2. Also, the BOD may cause a reset at higher voltages than specified as the threshold voltage in the Electrical Characterisitics.

Fix/Workaround

Download Development Kit Board Support Library and Example Code (rev 1.1.1 or later) and include `chip.h` in your project. In the start of the application code, call `void_CHIP_init(void);`. This procedure will re-program the device to a safe BOD threshold.

This erratum will be fixed in the next device revision.

5.2.2 Unpredictable Behaviour After WDOG Reset From EM2/EM3

Problem

When the watchdog (WDOG) triggers a reset while the EFM32 is in EM2 or EM3, the resulting behaviour is undefined.

Effect

After a watchdog reset from EM2/EM3, the EFM32 may go directly to hard fault or may not start at all.

Fix/Workaround

Don not use the watchdog in EM2/EM3. This is controlled by the EM2RUN and EM3RUN bits in WDOG_CTRL. The default setting is that the Watchdog is not running in EM2/EM3.

This erratum will be fixed in the next device revision.

5.2.3 Wrong RCO Frequency

Problem

The HFRCO, AUCHFRCO and LFRCO oscillators has wrong frequency when running with default settings.

Effect

The oscillator frequency has not been programmed with correct calibration values, and the frequencies are not within the expected frequency ranges.

Fix/Workaround

The oscillator frequency can be calibrated in the Clock Management Unit, which is described in the CMU chapter of the EFM32G Reference Manual.

This erratum will be fixed in the next device revision.

5.2.4 No calibration values for HFRCO band 1, 7, 11 and 21 MHz band

Problem

The Device Information page does not contain calibration values for the 1 MHz, 7 MHz, 11 MHz and 21 MHz frequency band.

Effect

The HFRCO frequency will be outside the expected frequency range when applying the calibration value from the device information page.

Fix/Workaround

The oscillator frequency can be calibrated in the Clock Management Unit, which is described in the CMU chapter of the EFM32G Reference Manual.

This erratum will be fixed in the next device revision.

5.2.5 LFRCO/HFRCO Frequency Change during EM2/3

Problem

RCO oscillator frequency can become unstable on transitions between EM2/3 and EM0.

Effect

When switching between EM0 and EM2/3, the following events can happen occasionally:

- The frequency of LFRCO becomes off by up to 14%
- The frequency of HFRCO becomes off by up to 6%

The frequency will be off for a shorter or longer period.

Fix/Workaround

Make this line of code part of your startup code, typically in the start of main():

```
*(volatile unsigned int*) 0x400C600CUL = 0x00020100;
```

As a result of this workaround, the current consumption in EM2/3 will go up by 450 nA.

This erratum will be fixed in the next device revision.

5.2.6 AUXHFRCO Not Automatically Disabled When Entering EM2/EM3

Problem

AUXHFRCO is not disabled automatically when entering EM2/EM3.

Effect

If AUXHFRCO is running while in EM2/EM3, and the EMVREG bit in EMU_CTRL is cleared. This may result in an unstable system.

Fix/Workaround

Disable AUXHFRCO by writing a 1 to AUXHFRCODIS in CMU_OSCENCMD, before going to EM2/EM3.

5.2.7 Peripheral clocks not gated in EM2/EM3 with debug session active

Problem

When a debug session has been active since the last reset, the EFM32 is not allowed to go to EM2 or EM3. When attempting to go to either EM2 or EM3, the system goes to EM1, and the peripheral clocks, which should have been turned off in EM2/EM3 keep going. This is only an issue when debugging a system.

Effect

The device cannot enter EM2/3 if a debug session has been entered since the last reset.

Fix/Workaround

If the debugger is running, clear HFPERCLKEN in CMU_HFPERCLKDIV before going to EM2/EM3 and set it when going back to EM0.

5.2.8 I^2C RX Buffer Silent Overflow

Problem

If reception of a byte by the RX shift register is completed while there is still a byte in the RX buffer, the byte in the shift register is silently discarded.

Effect

If a received byte is acknowledged before it is read out of the RXDATA, all new bytes received before the read operation are discarded. A new byte is not discarded if the read operation is performed before the new byte is fully received.

Fix/Workaround

Make sure to read the RX buffer before the reception of the next byte completes. One way to ensure this is to always read a received byte before acknowledging it.

This erratum will be fixed in the next device revision.

5.2.9 U(S)ART Double Buffer Transmission Control

Problem

Transmission control not working with double buffering.

Effect

When a frame is loaded into the transmission shift register, transmission control bits are always taken from buffer TX buffer element 1. If only one frame is in the U(S)ART buffer, the content of the buffer elements is equivalent, and transmission control bits work as specified. If two frames are in the buffer however, the control bits for the frame in buffer element 1 are used for transmitting the frame in buffer element 0. This is not a problem for frames consisting of more than 9 bits.

Fix/Workaround

If using transmission control bits make sure there are not more than frame in the U(S)ART buffer at a time. When TXBIL in U(S)ARTn_CTRL is cleared, the TXBL status and interrupt flags in U(S)ARTn_STATUS

and U(S)ARTn_IF respectively tell when the buffer is empty. When using transmission control bits a single frame can then be loaded into the USART for transmission.

5.2.10 LEUART + DMA awake for last byte transmitted:

Problem/Effect

When using the LEUART with DMA in EM2, TXDMAWU in LEUARTn_CTRL must be cleared when the DMA has no more data to transmit. Otherwise the LEUART will keep the system awake waiting for data from the DMA. The way to do this is to clear TXDMAWU in the DMA DONE interrupt for the channel feeding the LEUART with data. In this device revision, the DMA DONE interrupt will not trigger a wakeup from EM2. The DMA DONE interrupt is not executed before another interrupt wakes the system up from EM2.

Fix/Workaround

Use the TX complete interrupt (TXC) in the leuart to clear TXDMAWU, or clear TXDMAWU in the DMA DONE interrupt and make sure the TXC interrupt is triggered. The system will then be awake with a higher power consumption while the last byte is transmitted by the LEUART, but will be allowed to go back to EM2 once TXDMAWU has been cleared.

5.2.11 DMA Clock Disable Prevents EM2/EM3

Problem

When the DMA clock is disabled, the EFM32 is not able to go to Energy Modes 2 or 3.

Effect

The DMA will prevent the system to go to EM2/EM3 as long as the DMA clock is disabled.

Fix/Workaround

Make sure the DMA clock is enabled when going to EM2/EM3. The DMA clock is enabled by default, and can also be enabled in the CMU.

This erratum will be fixed in the next device revision.

5.2.12 ADC Temperature Sensor Not Working

Problem

The temperature sensor in the ADC does not work.

Effect

The temperature values read when sampling the temperature sensor in the ADC are not correct.

Fix/Workaround

Do not use the ADC temperature sensor.

This erratum will be fixed in the next device revision.

5.2.13 ADC SCANGAIN Affects Single Conversions

Problem

SCANGAIN in ADCn_CAL affects the gain setting for single conversions.

Effect

When SCANGAIN and SINGLEGAIN in ADCn_CAL have different values, single conversions will be affected by the SCANGAIN value.

Fix/Workaround

Configure SCANGAIN and SINGLEGAIN in ADCn_CAL to the same value. This requires the same reference to be used for both single and scan conversions.

This erratum will be fixed in the next device revision.

5.2.14 ADC at 1 Msample/s does not work at default bias settings

Problem

The ADC does not meet its 1 Msample/s performance target for the default ADC bias settings.

Effect

At default ADC bias settings the ADC conversion results are wrong when running the ADC_CLK at 13 MHz, which is required to reach the 1 Msample/s performance. Under typical conditions wrong conversions have been observed for ADC_CLK speeds of 8 MHz and higher.

Fix/Workaround

Increase the ADC performance by programming increasing the ADC bias, for example by using value 0xF0F for register ADCn_BIASPROG.

This erratum will be fixed in the next device revision.

5.2.15 Large spikes in ADC output when ADC output at mid code

Problem

The ADC does not always sample a voltage at (or close to) the middle of its range correctly (e.g. when sampling 1.25V when using the 2.5V internal reference).

Effect

When the ADC is sampling voltages at (or close to) the middle of its range, the ADC output code can be off by a large value (e.g. returning value 1023 or 3072 instead of the expected value of 2048). This effect happens for all ADC reference selections.

Fix/Workaround

Perform multiple (e.g. 3) ADC measurements for each ADC sample required and use the median value. Do not average the ADC results, throw away the 1023 or 3072 sample instead.

This erratum will be fixed in the next device revision.

5.2.16 DAC output voltage not correctly held in sample/hold mode

Problem

When the DAC is in sample/hold mode, the DAC output is not correctly held, but drifts faster than specified.

Effect

The DAC output starts drifting in the order of 10 mV/us after two DAC clock cycles.

Fix/Workaround

Put the DAC into continuous mode by setting the CONVMODE field in the DACn_CTRL register to CONTINUOUS. The DAC channels will then drive their outputs continuously with the data in the DACn_CHxDATA registers. This mode will maintain the output voltage and refresh is therefore not needed. As the DAC cores are not turned off between samples in continuous mode, the power consumption is increased compared to sample/hold mode.

5.2.17 DAC conversions closely after DAC channel enable are incorrect

Problem

DAC conversions done closely after enabling the DAC channel are incorrect.

Effect

The DAC output takes about 600 us (under typical conditions) to settle after a DAC channel has been enabled via setting field CH0EN in DACn_CH0CTRL (or CH1EN in DACn_CH1CTRL for channel 1). The effect is most visible for the 1.25V and 2.5V internal references.

Fix/Workaround

After enabling a DAC channel, wait 600 us before programming the channel data (via DACn_CH0DATA, DACn_CH1DATA, or DACn_COMBDATA).

This erratum will be fixed in the next device revision.

6 Revision History

6.1 Revision 0.83

January 25th, 2010

Updated errata in Chapter 5 (p. 36)

Specified flash word width in Section 3.7 (p. 18)

Added Capacitive Sense Internal Resistor values in Section 3.12 (p. 27) .

6.2 Revision 0.82

December 9th, 2009

Incorrect pin 0 removed from Table 4.1 (p. 30) .

Updated conctact information.

ADC current consumption numbers updated in Section 3.10 (p. 20)

6.3 Revision 0.81

November 20th, 2009

Section 3.1 (p. 8) updated.

Storage temperature in Section 3.2 (p. 8) updated.

Temperature coefficient of band-gap reference in Section 3.6 (p. 17) added.

Erase times in Section 3.7 (p. 18) updated.

Definitions of DNL and INL added in Figure 3.11 (p. 24) and Figure 3.12 (p. 24) .

Current consumption of digital peripherals added in Section 3.14 (p. 28) .

Package information in Section 4.3 (p. 34) corrected.

Updated erratas in Chapter 5 (p. 36)

6.4 Revision 0.80

Initial preliminary revision, October 19th, 2009

A Disclaimer and Trademarks

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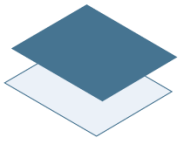
Table of Contents

List of Figures

List of Tables

List of Equations



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