LINEAR TECHNOLOGY

8-/16-Channel 16-Bit No Latency $\Delta\Sigma^{TM}$ ADC

FEATURES

- **16-Channel Single-Ended or 8-Channel Differential Inputs**
- **Low Supply Current (200μA, 4μA in Autosleep)**
- **Rail-to-Rail Differential Input/Reference**
- **16-Bit No Missing Codes**
- **1μV RMS Noise, 16-ENOBS Independent of V_{REF}**
- **Very Low Transition Noise: Less Than 0.02LSB**
- **Operates with a Reference as Low as 100mV with 1.5μV LSB Step Size**
- **Guaranteed Modulator Stability and Lock-Up Immunity for Any Input and Reference Conditions**
- Single Supply 2.7V to 5.5V Operation
- Internal Oscillator—No External Components Required
- 87dB Min, 50Hz and 60Hz Simultaneous Notch Filter
- Pin Compatible with the 24-Bit LTC2418
- 28-Lead SSOP Package

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control

DESCRIPTION

The LTC®2439-1 is a 16-channel (8-differential) micropower 16-bit $\Delta\Sigma$ analog-to-digital converter. It operates from 2.7V to 5.5V and includes an integrated oscillator, 0.12LSB INL and 1μV RMS noise. It uses delta-sigma technology and provides single cycle settling time for multiplexed applications. Through a single pin, the LTC2439-1 can be configured for better than 87dB differential mode rejection at 50Hz and 60Hz ±2%, or it can be driven by an external oscillator for a user-defined rejection frequency. The internal oscillator requires no external frequency setting components.

The LTC2439-1 accepts any external differential reference voltage from 0.1V to V_{CC} for flexible ratiometric and remote sensing measurement applications. It can be configured to take 8 differential channels or 16 single-ended channels. The full-scale bipolar input range is from $-0.5V_{REF}$ to $0.5V_{REF}$. The reference common mode voltage, V_{REFCM}, and the input common mode voltage, V_{INCM}, may be independently set between GND and V_{CC}. The DC common mode input rejection is better than 140dB.
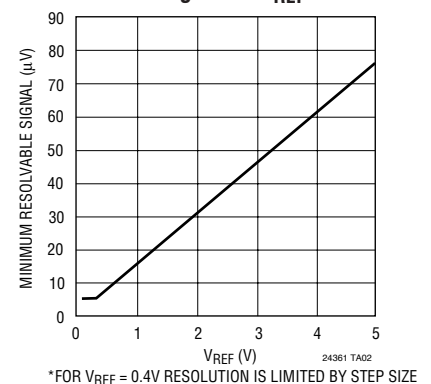
The LTC2439-1 communicates through a flexible 4-wire digital interface that is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION
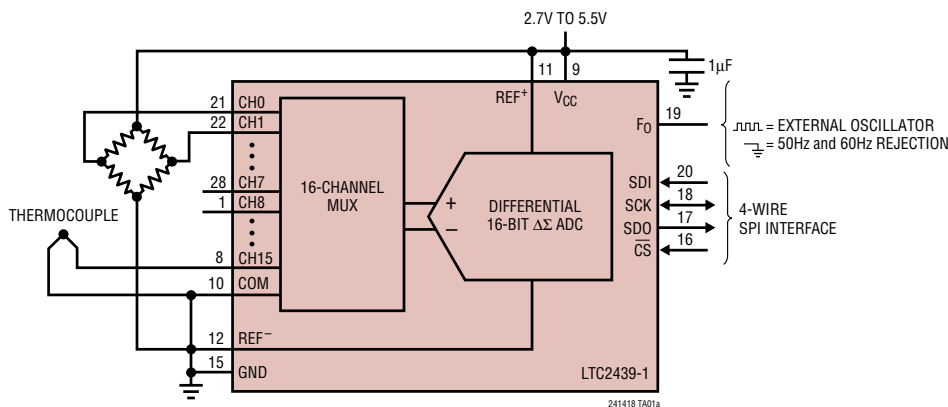
Minimum Resolvable Signal vs V_{REF}

*FOR V_{REF} = 0.4V RESOLUTION IS LIMITED BY STEP SIZE

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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND .... −0.3V to 7V
Analog Input Voltage to GND .... −0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. −0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND .... −0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... −0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
  LTC2439-1C .... 0°C to 70°C
  LTC2439-1I .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

CH8	1		28	CH7
CH9	2		27	CH6
CH10	3		26	CH5
CH11	4		25	CH4
CH12	5		24	CH3
CH13	6		23	CH2
CH14	7		22	CH1
CH15	8		21	CH0
V_{CC}	9		20	SDI
COM	10		19	F_O
REF⁺	11		18	SCK
REF⁻	12		17	SDO
NC	13		16	$\overline{CS}$
NC	14		15	GND

GN PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER	PART MARKING
LTC2439-1CGN
LTC2439-1IGN	

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS   The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, −0.5 • V_{REF} ≤ V_{IN} ≤ 0.5 • V_{REF}, (Note 5)	●	16			Bits
Integral Nonlinearity	4.5V ≤ V_{CC} ≤ 5.5V, REF⁺ = 2.5V, REF⁻ = GND, V_{INCM} = 1.25V, (Note 6)
5V ≤ V_{CC} ≤ 5.5V, REF⁺ = 5V, REF⁻ = GND, V_{INCM} = 2.5V, (Note 6)
REF⁺ = 2.5V, REF⁻ = GND, V_{INCM} = 1.25V, (Notes 6, 15)	●		0.06
0.12
0.30	1.25	LSB
LSB
LSB
Offset Error	2.5V ≤ REF⁺ ≤ V_{CC}, REF⁻ = GND,
GND ≤ IN⁺ = IN⁻ ≤ V_{CC}, (Notes 12,15)	●		5	20	μV
Offset Error Drift	2.5V ≤ REF⁺ ≤ V_{CC}, REF⁻ = GND,
GND ≤ IN⁺ = IN⁻ ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ REF⁺ ≤ V_{CC}, REF⁻ = GND,
IN⁺ = 0.75REF⁺, IN⁻ = 0.25 • REF⁺ (Note 15)	●		0.16	1.25	LSB
Positive Full-Scale Error Drift	2.5V ≤ REF⁺ ≤ V_{CC}, REF⁻ = GND,
IN⁺ = 0.75REF⁺, IN⁻ = 0.25 • REF⁺			0.03		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ REF⁺ ≤ V_{CC}, REF⁻ = GND,
IN⁺ = 0.25 • REF⁺, IN⁻ = 0.75 • REF⁺ (Note 15)	●		0.16	1.25	LSB
Negative Full-Scale Error Drift	2.5V ≤ REF⁺ ≤ V_{CC}, REF⁻ = GND,
IN⁺ = 0.25 • REF⁺, IN⁻ = 0.75 • REF⁺			0.03		ppm of V_{REF}/°C

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CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Total Unadjusted Error	$5V \leq V_{CC} \leq 5.5V$, REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V			0.20		LSB
	$5V \leq V_{CC} \leq 5.5V$, REF^+ = 5V, REF^- = GND, V_{INCM} = 2.5V			0.20		LSB
	REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V, (Note 6)					
Output Noise	$5V \leq V_{CC} \leq 5.5V$, REF^+ = 5V, $V_{REF}-$ = GND, $GND \leq IN^- = IN^+ \leq 5V$ (Note 12)			1		μV_{RMS}
Input Common Mode Rejection DC	$2.5V \leq REF^+ \leq V_{CC}$, REF^- = GND, $GND \leq IN^- = IN^+ \leq V_{CC}$ (Note 5)	●	130	140		dB
Input Common Mode Rejection 49Hz to 61.2Hz	$2.5V \leq REF^+ \leq V_{CC}$, REF^- = GND, $GND \leq IN^- = IN^+ \leq V_{CC}$, (Note 5)	●	140			dB
Input Normal Mode Rejection 49Hz to 61.2Hz	(Note 5)	●	87			dB
Reference Common Mode Rejection DC	$2.5V \leq REF^+ \leq V_{CC}$, $GND \leq REF^- \leq 2.5V$, V_{REF} = 2.5V, $IN^- = IN^+$ = GND (Note 5)	●	130	140		dB
Power Supply Rejection, DC	REF^+ = 2.5V, REF^- = GND, $IN^- = IN^+$ = GND			120		dB
Power Supply Rejection, Simultaneous 50Hz/60Hz ±2%	REF^+ = 2.5V, REF^- = GND, $IN^- = IN^+$ = GND			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage		●	GND − 0.3		V_{CC} + 0.3	V
IN^-	Absolute/Common Mode IN^- Voltage		●	GND − 0.3		V_{CC} + 0.3	V
V_{IN}	Input Differential Voltage Range ($IN^+ - IN^-$)		●	$-V_{REF}/2$		$V_{REF}/2$	V
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		V_{CC} − 0.1	V
V_{REF}	Reference Differential Voltage Range ($REF^+ - REF^-$)		●	0.1		V_{CC}	V
C_S (IN^+)	IN^+ Sampling Capacitance				18		pF
C_S (IN^-)	IN^- Sampling Capacitance				18		pF
C_S (REF^+)	REF^+ Sampling Capacitance				18		pF
C_S (REF^-)	REF^- Sampling Capacitance				18		pF
I_{DC_LEAK} (IN^+)	IN^+ DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, IN^+ = GND	●	−100	1	100	nA
I_{DC_LEAK} (IN^-)	IN^- DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, IN^- = 5V	●	−100	1	100	nA
I_{DC_LEAK} (REF^+)	REF^+ DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, REF^+ = 5V	●	−100	1	100	nA
I_{DC_LEAK} (REF^-)	REF^- DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, REF^- = GND	●	−100	1	100	nA
	Off Channel to On Channel Isolation (R_{IN} = 100Ω)	DC			140		dB
		1Hz			140		dB
		f_S = 15,3600Hz			140		dB
t_{OPEN}	MUX Break-Before-Make Interval	$2.7V \leq V_{CC} \leq 5.5V$			100		ns
$I_{S(OFF)}$	Channel Off Leakage Current	Channel at V_{CC} and GND	●	−100	1	100	nA

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DIGITAL INPUTS AND DIGITAL OUTPUTS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O, SDI	$2.7V \leq V_{CC} \leq 5.5V$ $2.7V \leq V_{CC} \leq 3.3V$	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O, SDI	$4.5V \leq V_{CC} \leq 5.5V$ $2.7V \leq V_{CC} \leq 5.5V$	●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	$2.7V \leq V_{CC} \leq 5.5V$ (Note 8) $2.7V \leq V_{CC} \leq 3.3V$ (Note 8)	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8) $2.7V \leq V_{CC} \leq 5.5V$ (Note 8)	●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O, SDI	$0V \leq V_{IN} \leq V_{CC}$	●	−10		10	μA
I_{IN}	Digital Input Current SCK	$0V \leq V_{IN} \leq V_{CC}$ (Note 8)	●	−10		10	μA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O, SDI				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 8)			10		pF
V_{OH}	High Level Output Voltage SDO	$I_O = -800μA$	●	$V_{CC} - 0.5$			V
V_{OL}	Low Level Output Voltage SDO	$I_O = 1.6mA$	●			0.4	V
V_{OH}	High Level Output Voltage SCK	$I_O = -800μA$ (Note 9)	●	$V_{CC} - 0.5$			V
V_{OL}	Low Level Output Voltage SCK	$I_O = 1.6mA$ (Note 9)	●			0.4	V
I_{OZ}	Hi-Z Output Leakage SDO		●	−10		10	μA

POWER REQUIREMENTS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode Sleep Mode	$\overline{CS} = 0V$ (Note 11) $\overline{CS} = V_{CC}$ (Note 11) $\overline{CS} = V_{CC}$, $2.7V \leq V_{CC} \leq 3.3V$ (Note 11, 14)	● ●		200 4 2	300 15	μA μA μA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		2000	kHz
t_{HEO}	External Oscillator High Period		●	0.25		390	μs
t_{LEO}	External Oscillator Low Period		●	0.25		390	μs
t_{CONV}	Conversion Time	$F_O = 0V$	●	143.8	146.7	149.6	ms
		External Oscillator (Note 10)	●		$20510/f_{EOSC}$ (in kHz)		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9)			17.5		kHz
		External Oscillator (Notes 9, 10)			$f_{EOSC}/8$		kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 8)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 19-Bit Data Output Time	Internal Oscillator (Notes 9, 11)	●	1.06	1.09	1.11	ms
		External Oscillator (Notes 9, 10)	●		$152/f_{EOSC}$ (in kHz)		ms
t_{DOUT_ESCK}	External SCK 19-Bit Data Output Time	(Note 7)	●		$19/f_{ESCK}$ (in kHz)		ms
t_1	$\overline{CS}$ ↓ to SDO Low		●	0		200	ns
$t2$	$\overline{CS}$ ↑ to SDO High Z		●	0		200	ns
$t3$	$\overline{CS}$ ↓ to SCK ↓	(Note 9)	●	0		200	ns
$t4$	$\overline{CS}$ ↓ to SCK ↑	(Note 8)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			220	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns
t_7	SDI Setup Before SCK ↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK ↑	(Note 5)	●	100			ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{CC} = 2.7V$ to 5.5V unless otherwise specified.
$V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$; $V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$, IN^+ and IN^- are defined as the selected positive and negative input respectively.

Note 4: F_O pin tied to GND or to V_{CC} or to external conversion clock source with $f_{EOSC} = 153600Hz$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size ($V_{REF}/2^{16}$) and the single shot measurement. Typical specifications are measured from the center of the quantization band.

Note 7: $F_O = GND$ (internal oscillator) or $f_{EOSC} = 139800Hz \pm 2\%$ (external oscillator).

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance $C_{LOAD} = 20pF$.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses the internal oscillator.
$F_O = 0V$ or $F_O = V_{CC}$.

Note 12: 1μV RMS noise is independent of V_{REF}. Since the noise performance is limited by the quantization, lowering V_{REF} improves the effective resolution.

Note 13: Guaranteed by design and test correlation.

Note 14: The low sleep mode current is valid only when $\overline{CS}$ is high.

Note 15: These parameters are guaranteed by design over the full supply and temperature range. Automated testing procedures are limited by the LSB Step Size ($V_{REF}/2^{16}$).

PIN FUNCTIONS

CH0 to CH15 (Pin 21 to Pin 28 and Pin 1 to Pin 8): Analog Inputs. May be programmed for single-ended or differential mode.

V_{CC} (Pin 9): Positive Supply Voltage. Bypass to GND (Pin 15) with a 10μF tantalum capacitor in parallel with 0.1μF ceramic capacitor as close to the part as possible.

COM (Pin 10): The common negative input (IN⁻) for all single-ended multiplexer configurations. The voltage on Channel 0 to 15 and COM input pins can have any value between GND – 0.3V and V_{CC} + 0.3V. Within these limits, the two selected inputs (IN⁺ and IN⁻) provide a bipolar input range (V_{IN} = IN⁺ – IN⁻) from $-0.5 \cdot V_{REF}$ to $0.5 \cdot V_{REF}$. Outside this input range, the converter produces unique overrange and underrange output codes.

REF⁺ (Pin 11), REF⁻ (Pin 12): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the positive reference input, REF⁺, is maintained more positive than the negative reference input, REF⁻, by at least 0.1V.

GND (Pin 15): Ground. Connect this pin to a ground plane through a low impedance connection.

$\overline{CS}$ (Pin 16): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 17): Three-State Digital Output. During the Data Output period, this pin is used as the serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS}$ = V_{CC}), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

SCK (Pin 18): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as the digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as the digital input for the external serial interface clock during the Data Output period. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock Operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of $\overline{CS}$.

F_O (Pin 19): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to GND (F_O = 0V), the converter uses its internal oscillator and rejects 50Hz and 60Hz simultaneously. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its system clock and the digital filter has 87dB minimum rejection in the range f_{EOSC}/2560 ±14% and 110dB minimum rejection at f_{EOSC}/2560 ±4%.

SDI (Pin 20): Serial Digital Data Input. During the Data Output period, this pin is used to shift in the multiplexer address started from the first rising SCK edge. During the Conversion and Sleep periods, this pin is in the DON'T CARE state. However, a HIGH or LOW logic level should be maintained on SDI in the DON'T CARE mode to avoid an excessive current in the SDI input buffers.

NC (Pins 13, 14): Not Internally Connected. Do not connect or connect to ground.
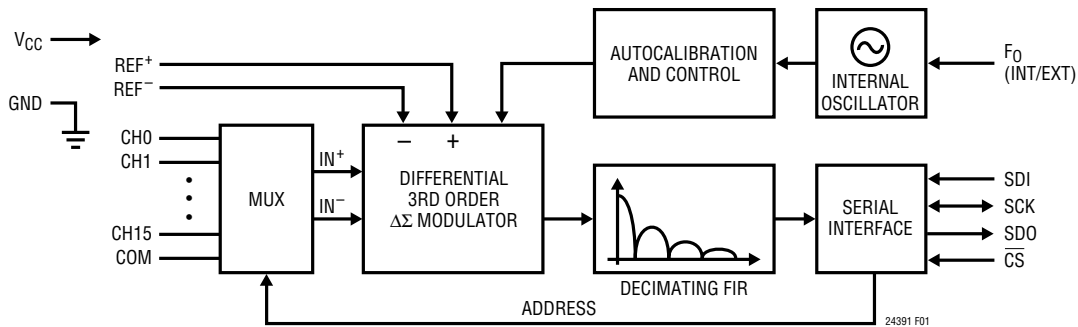
FUNCTIONAL BLOCK DIAGRAM

Figure 1

TEST CIRCUITS

Hi-Z TO V_{OH}
V_{OL} TO V_{OH}
V_{OH} TO Hi-Z

Hi-Z TO V_{OL}
V_{OH} TO V_{OL}
V_{OL} TO Hi-Z

APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2439-1 is a multichannel, low power, delta-sigma analog-to-digital converter with an easy-to-use 4-wire serial interface (see Figure 1). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data input/output (see Figure 2). The 4-wire interface consists of serial data input (SDI), serial data output (SDO), serial clock (SCK) and chip select ($\overline{CS}$).

Initially, the LTC2439-1 performs a conversion. Once the conversion is complete, the device enters the sleep state. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. While in the sleep state, power consumption is reduced by nearly two orders of magnitude. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.
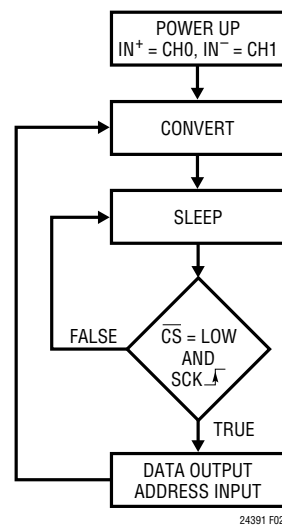
Figure 2. LTC2439-1 State Transition Diagram

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APPLICATIONS INFORMATION

Once $\overline{CS}$ is pulled LOW, the device exits the low power mode and enters the data output state. If $\overline{CS}$ is pulled HIGH before the first rising edge of SCK, the device returns to the low power sleep mode and the conversion result is still held in the internal static shift register. If $\overline{CS}$ remains LOW after the first rising edge of SCK, the device begins outputting the conversion result and inputting channel selection bits. Taking $\overline{CS}$ high at this point will terminate the data output state and start a new conversion. The channel selection control bits are shifted in through SDI from the first rising edge of SCK and depending on the control bits, the converter updates its channel selection immediately and is valid for the next conversion. The details of channel selection control bits are described in the Input Data Mode section. The output data is shifted out the SDO pin under the control of the serial clock (SCK). The output data is updated on the falling edge of SCK allowing

the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 19 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats. In order to maintain compatibility with 24-/32-bit data transfers, it is possible to clock the LTC2439-1 with additional serial clock pulses. This results in additional data bits which are always logic HIGH.

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2439-1 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.
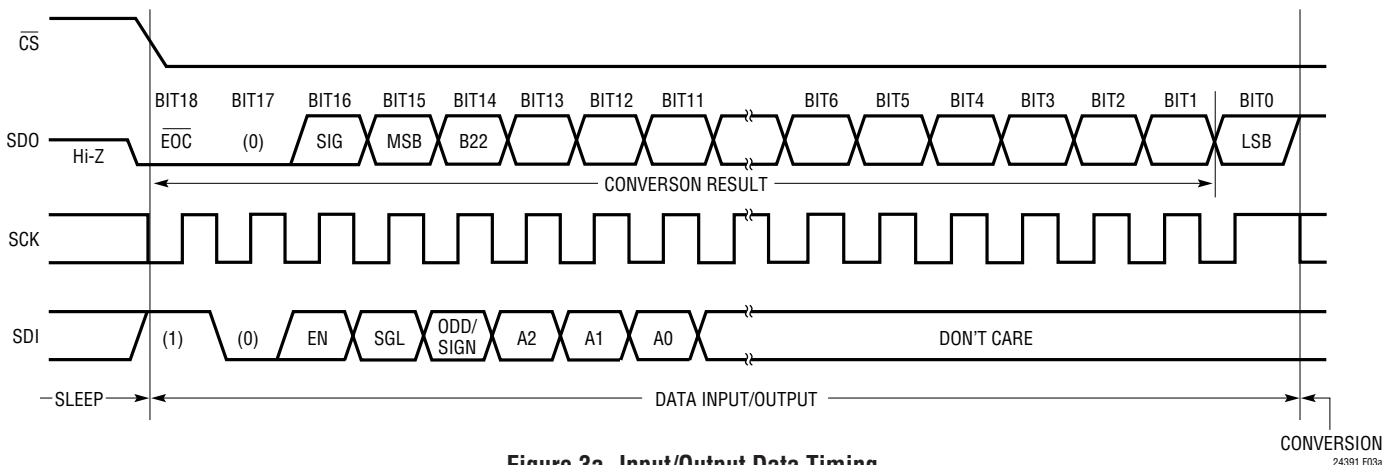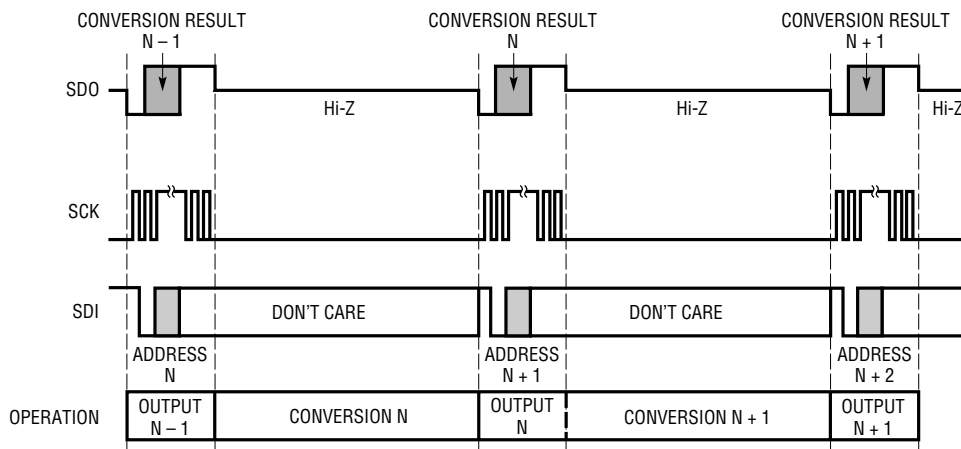
Figure 3a. Input/Output Data Timing

Figure 3b. Typical Operation Sequence

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APPLICATIONS INFORMATION

Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz and 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2439-1 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2436-1 achieves a minimum of 87dB rejection over the range 49Hz to 61.2Hz.

Ease of Use

The LTC2439-1 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2439-1 performs offset and full-scale calibrations in every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2439-1 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 3-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a typical duration of 1ms. The POR signal clears all internal registers. Following the POR signal, the LTC2439-1 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

The LTC2439-1 accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the REF⁺ and REF⁻ pins covers the entire range from GND to V_{CC}. For correct converter operation, the REF⁺ pin must always be more positive than the REF⁻ pin.

The LTC2439-1 can accept a differential reference voltage from 0.1V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will significantly improve the converter's effective resolution, since the thermal noise (1μV) is well below the quantization level of the device (75.6μV for a 5V reference). At the minimum reference (100mV) the thermal noise remains constant at 1μV RMS (or 6μV$_{P-P}$), while the quantization is reduced to 1.5μV per LSB. As a result, lowering the reference improves the effective resolution for low level input voltages.

Input Voltage Range

The two selected pins are labeled IN⁺ and IN⁻ (see Table 1). Once selected (either differential or single-ended multiplexing mode), the analog input is differential with a common mode range for the IN⁺ and IN⁻ input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2439-1 converts the bipolar differential input signal, V_{IN} = IN⁺ – IN⁻, from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF} where V_{REF} = REF⁺ – REF⁻. Outside this range the converter indicates the overrange or the underrange condition using distinct output codes.

Input signals applied to IN⁺ and IN⁻ pins may extend 300mV below ground or above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the IN⁺ or IN⁻ pins without affecting the performance of the device. In the physical layout, it is important to

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maintain the parasitic capacitance of the connection between these series resistors and the corresponding pins as low as possible; therefore, the resistors should be located as close as practical to the pins. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 10nA input leakage current will develop a 1LBS offset error on an 8k resistor if $V_{REF} = 5V$. This error has a very strong temperature dependency.

Table 1. Channel Selection

MUX ADDRESS					CHANNEL SELECTION																	
SGL	ODD/ SIGN	A2	A1	A0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	COM
* 0	0	0	0	0	IN+	IN−															
0	0	0	0	1			IN+	IN−													
0	0	0	1	0					IN+	IN−											
0	0	0	1	1							IN+	IN−									
0	0	1	0	0									IN+	IN−							
0	0	1	0	1											IN+	IN−					
0	0	1	1	0													IN+	IN−			
0	0	1	1	1															IN+	IN−	
0	1	0	0	0	IN−	IN+															
0	1	0	0	1			IN−	IN+													
0	1	0	1	0					IN−	IN+											
0	1	0	1	1							IN−	IN+									
0	1	1	0	0									IN−	IN+							
0	1	1	0	1											IN−	IN+					
0	1	1	1	0													IN−	IN+			
0	1	1	1	1															IN−	IN+	
1	0	0	0	0	IN+																IN−
1	0	0	0	1			IN+														IN−
1	0	0	1	0					IN+												IN−
1	0	0	1	1							IN+										IN−
1	0	1	0	0									IN+								IN−
1	0	1	0	1											IN+						IN−
1	0	1	1	0													IN+				IN−
1	0	1	1	1															IN+		IN−
1	1	0	0	0		IN+															IN−
1	1	0	0	1				IN+													IN−
1	1	0	1	0						IN+											IN−
1	1	0	1	1								IN+									IN−
1	1	1	0	0										IN+							IN−
1	1	1	0	1												IN+					IN−
1	1	1	1	0														IN+			IN−
1	1	1	1	1																IN+	IN−

*Default at power up

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Input Data Format

When the LTC2439-1 is powered up, the default selection used for the first conversion is IN+ = CH0 and IN− = CH1 (Address = 00000). In the data input/output mode following the first conversion, a channel selection can be updated using an 8-bit word. The LTC2439-1 serial input data is clocked into the SDI pin on the rising edge of SCK (see Figure 3a). The input is composed of an 8-bit word with the first 3 bits acting as control bits and the remaining 5 bits as the channel address bits.

The first 2 bits are always 10 for proper updating operation. The third bit is EN. For EN = 1, the following 5 bits are used to update the input channel selection. For EN = 0, previous channel selection is kept and the following bits are ignored. Therefore, the address is updated when the 3 control bits are 101 and kept for 100. Alternatively, the 3 control bits can be all zero to keep the previous address. This alternation is intended to simplify the SDI interface allowing the user to simply connect SDI to ground if no update is needed. Combinations other than 101, 100 and 000 of the 3 control bits should be avoided.

When update operation is set (101), the following 5 bits are the channel address. The first bit, SGL, decides if the differential selection mode (SGL = 0) or the single-ended selection mode is used (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input; for SGL = 1, one of the 16 channels (CH0-CH15) is selected as the positive input and the COM pin is used as the negative input. For a given channel selection, the converter will measure the voltage between the two channels indicated by IN+ and IN− in the selected row of Table 1.

Output Data Format

The LTC2439-1 serial output data stream is 19 bits long. The first 3 bits represent status information indicating the conversion state and sign. The next 16 bits are the conversion result, MSB first. The third and fourth bit together are also used to indicate an underrange condition (both bits low means the differential input voltage is below −FS) or an overrange condition (both bits high means the differential input voltage is above +FS).

Bit 18 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 17 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 16 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW.

Bit 15 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 16 also provides the underrange or overrange indication. If both Bit 16 and Bit 15 are HIGH, the differential input voltage is above +FS. If both Bit 16 and Bit 15 are LOW, the differential input voltage is below −FS.

The function of these bits is summarized in Table 2.

Table 2. LTC2439-1 Status Bits

Input Range	Bit 18 $\overline{EOC}$	Bit 17 DMY	Bit 16 SIG	Bit 15 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0	1	0
$-0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < -0.5 \cdot V_{REF}$	0	0	0	0

Bits 15-0 are the 16-Bit conversion result MSB first. Bit 0 is the least significant bit (LSB).

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3a. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 18 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 17 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 18th SCK and may be latched on the rising edge of the 19th SCK pulse. On the falling edge of the 19th SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$

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(Bit 18) for the next conversion cycle. Table 3 summarizes the output data format.

In order to remain compatible with some SPI microcontrollers, more than 19 SCK clock pulses may be applied. As long as these clock pulses are complete before the conversion ends, they will not effect the serial data. However, switching SCK during a conversion may generate ground currents in the device leading to extra offset and noise error sources.

As long as the voltage applied to any channel (CH0-CH15, COM) is maintained within the −0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below −FS, the conversion result is clamped to the value corresponding to −FS − 1LSB.

Simultaneous Frequency Rejection

The LTC2439-1 internal oscillator provides better than 87dB normal mode rejection over the range of 49Hz to 61.2Hz as shown in Figure 4. For simultaneous 50Hz/60Hz rejection using the internal oscillator, F_O should be connected to GND.

When a fundamental rejection frequency different from the range 49Hz to 61.2Hz is required or when the converter must be synchronized with an outside source, the LTC2439-1 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods, t_{HEO} and t_{LEO}, are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2439-1 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4%. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 5. Whenever an external clock is not present at the F_O pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2439-1 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

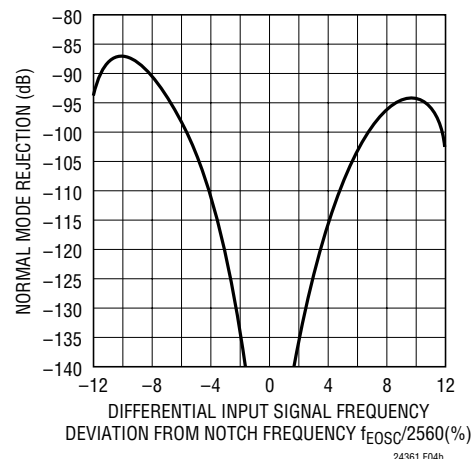Table 4 summarizes the duration of each state and the achievable output data rate as a function of F_O.

Figure 4. LTC2439-1 Normal Mode Rejection When Using an Internal Oscillator

Figure 5. LTC2439-1 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

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Table 3. LTC2439-1 Output Data Format

Differential Input Voltage V_{IN}*	Bit 18 $\overline{EOC}$	Bit 17 DMY	Bit 16 SIG	Bit 15 MSB	Bit 14	Bit 13	Bit 12	...	Bit 0
V_{IN}* ≥ 0.5 • V_{REF}**	0	0	1	1	0	0	0	...	0
0.5 • V_{REF}** − 1LSB	0	0	1	0	1	1	1	...	1
0.25 • V_{REF}**	0	0	1	0	1	0	0	...	0
0.25 • V_{REF}** − 1LSB	0	0	1	0	0	1	1	...	1
0	0	0	1	0	0	0	0	...	0
−1LSB	0	0	0	1	1	1	1	...	1
−0.25 • V_{REF}**	0	0	0	1	1	0	0	...	0
−0.25 • V_{REF}** − 1LSB	0	0	0	1	0	1	1	...	1
−0.5 • V_{REF}**	0	0	0	1	0	0	0	...	0
V_{IN}* < −0.5 • V_{REF}**	0	0	0	0	1	1	1	...	1

*The differential input voltage V_{IN} = IN^+ − IN^-.   **The differential reference voltage V_{REF} = REF^+ − REF^-.

Table 4. LTC2439-1 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW Simultaneous 50Hz/60Hz Rejection	147ms, Output Data Rate ≤ 6.8 Readings/s
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz (f_{EOSC}/2560 Rejection)	20510/f_{EOSC}s, Output Data Rate ≤ f_{EOSC}/20510 Readings/s
SLEEP			As Long As $\overline{CS}$ = HIGH Until $\overline{CS}$ = LOW and SCK ⌐
DATA OUTPUT	Internal Serial Clock	F_O = LOW (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.09ms (19 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than 152/f_{EOSC}ms (19 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than 19/f_{SCK}ms (19 SCK cycles)

SERIAL INTERFACE PINS

The LTC2439-1 transmits the conversion results and receives the start of conversion command through a synchronous 4-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data I/O state it is used to read the conversion result and write in channel selection bits.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 18) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock and each input bit is shifted in the SDI pin on the rising edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2439-1 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The Internal or External SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Serial Data Input (SDI)

The serial data input pin, SDI (Pin 20), is used to shift in the channel control bits during the data output state to prepare the channel selection for the following conversion.

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When $\overline{CS}$ (Pin 16) is HIGH or the converter is in the conversion state, the SDI input is ignored and may be driven HIGH or LOW. When $\overline{CS}$ goes LOW and the conversion is complete, SDO goes low and then SDI starts to shift in bits on the rising edge of SCK.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 17), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 16) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ = LOW.

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 16), is used to test the conversion status and to enable the data input/output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2439-1 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data input/output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ = LOW). If the device has not finished loading the last input bit (A0 of SDI) by the time $\overline{CS}$ pulled HIGH, the address information is discarded and the previous address is kept.

Finally, $\overline{CS}$ can be used to control the free-running mode of operation, see Serial Interface Timing Modes section. Grounding $\overline{CS}$ will force the ADC to continuously convert at the maximum output rate selected by F_O.

SERIAL INTERFACE TIMING MODES

The LTC2439-1's 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle conversion. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW) or an external oscillator connected to the F_O pin. Refer to Table 6 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 6.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ falling edge.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the conversion is complete. If $\overline{CS}$ is HIGH, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state, its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK

Table 6. LTC2439-1 Interface Timing Modes

| Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 6, 7
External SCK, 3-Wire I/O	External	SCK	SCK	Figure 8
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}$ ↓	$\overline{CS}$ ↓	Figures 9, 10
Internal SCK, 3-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 11

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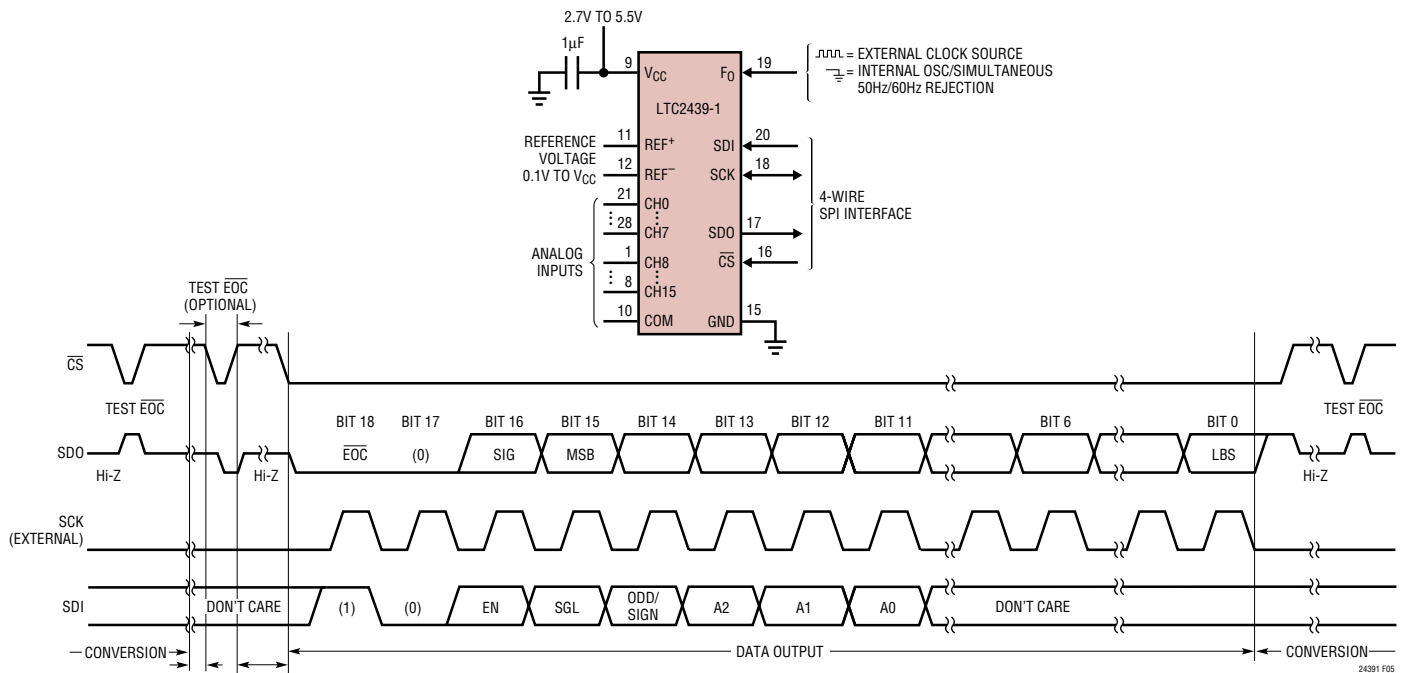
Figure 6. External Serial Clock, Single Cycle Operation

is seen while $\overline{CS}$ is LOW. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 19th rising edge of SCK. On the 19th falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC} = 1$) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z. As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first rising edge and the19th falling edge of SCK, see Figure 7. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. If the device has not finished loading the last input bit A0 of SDI by the time $\overline{CS}$ is pulled HIGH, the address information is discarded and the previ-

ous address is kept. This is useful for aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 3-Wire I/O

This timing mode utilizes a 3-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 8. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded typically 1ms after V_{CC} exceeds approximately 2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC} = 1$ while the conversion is in progress and $\overline{EOC} = 0$ once the conversion ends. On the falling edge of $\overline{EOC}$, the conversion result is loaded into an internal static

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shift register. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. $\overline{EOC}$ can be latched on the first

rising edge of SCK. On the 19th falling edge of SCK, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.
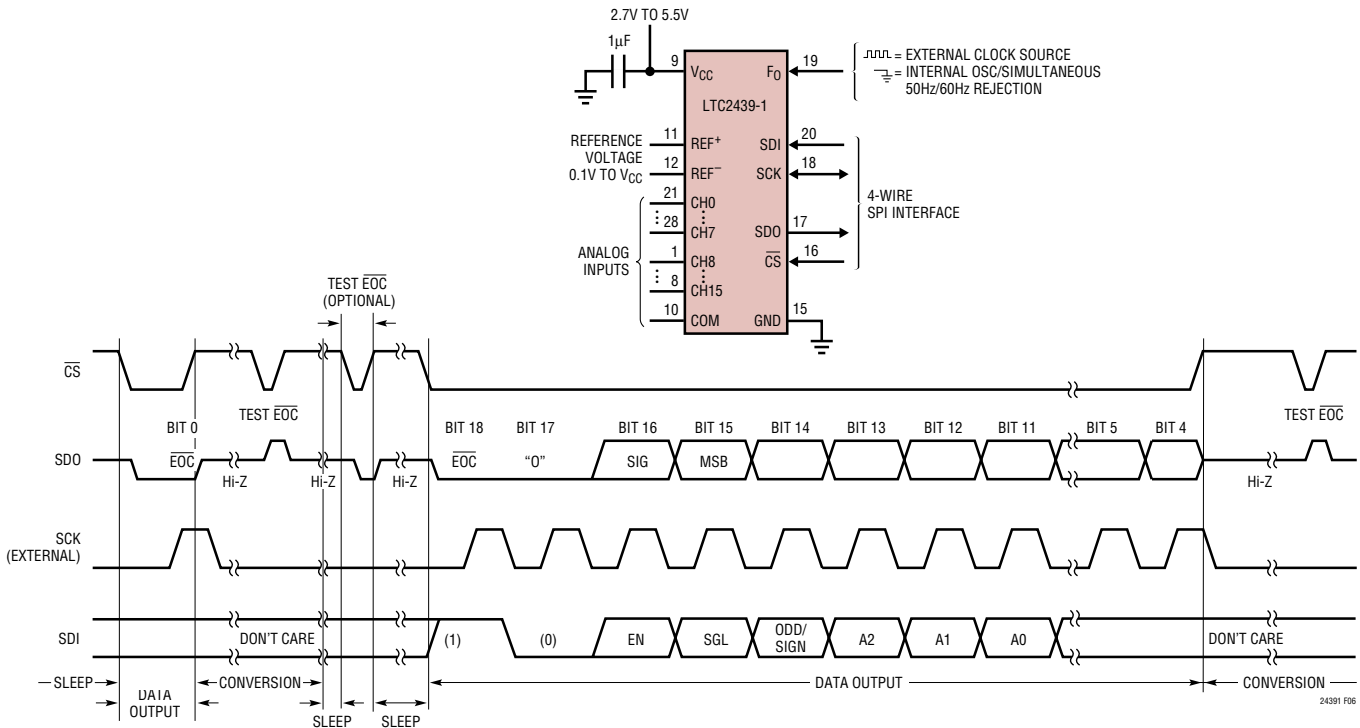

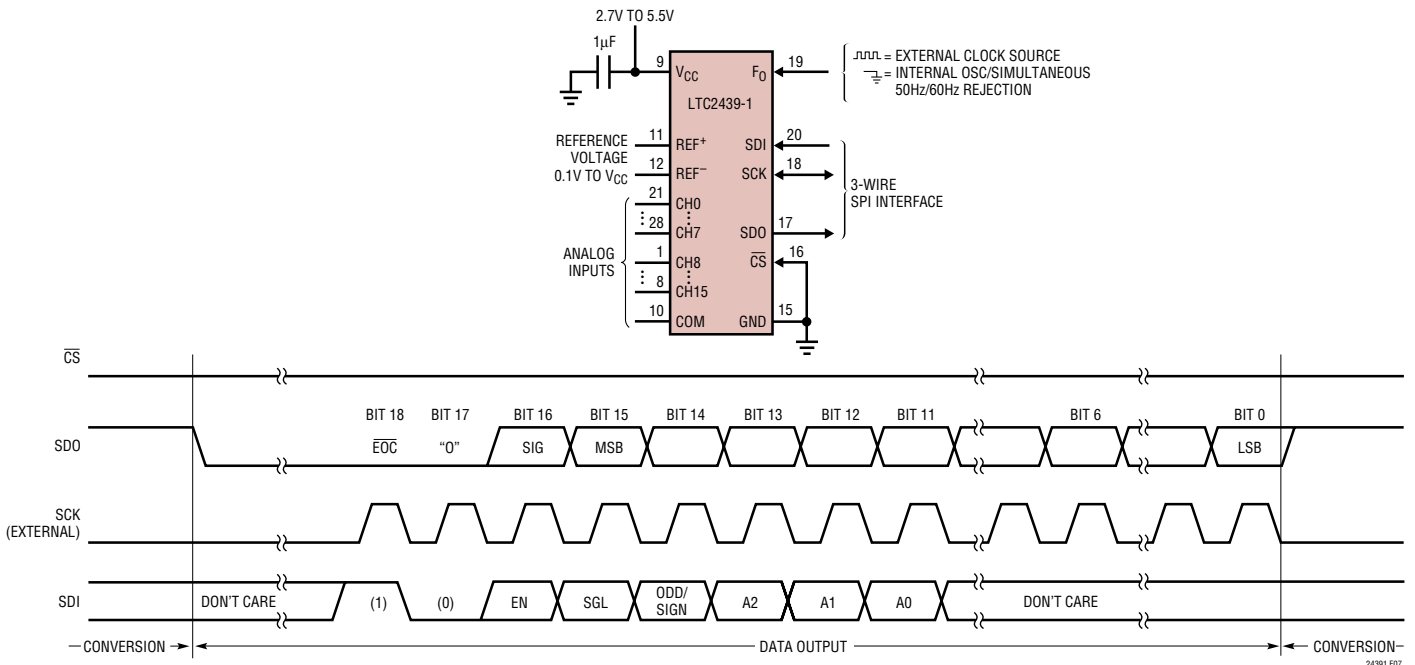**Figure 7. External Serial Clock, Reduced Data Output Length**

Figure 8. External Serial Clock, $\overline{CS}$ = 0 Operation

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Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 9.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is auto-matically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the conversion is complete.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the low power mode during the $\overline{EOC}$ test. In order to allow the device to return to the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of CS (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23μs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device returns to the sleep state and the conversion result is held in the internal static shift register.

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data I/O cycle concludes after the 19th rising edge. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 19th rising edge of SCK. After the 19th rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH and a new conversion starts.
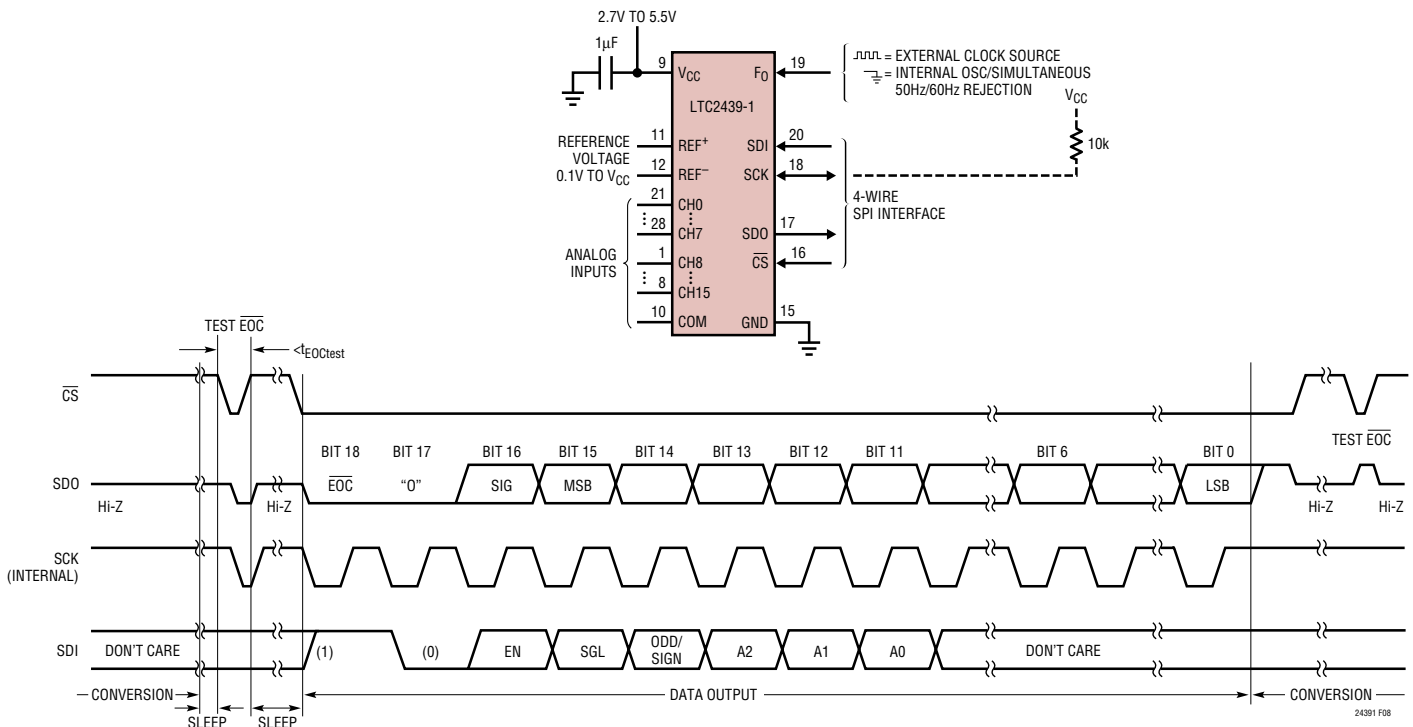

Figure 9. Internal Serial Clock, Single Cycle Operation

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Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 19th rising edge of SCK, see Figure 10. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. If the device has not finished loading the last input bit (A0 of SDI) by the time $\overline{CS}$ is pulled HIGH, the address information is discarded and the previous address is still kept. This is useful for aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2439-1's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode.

However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2439-1's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.
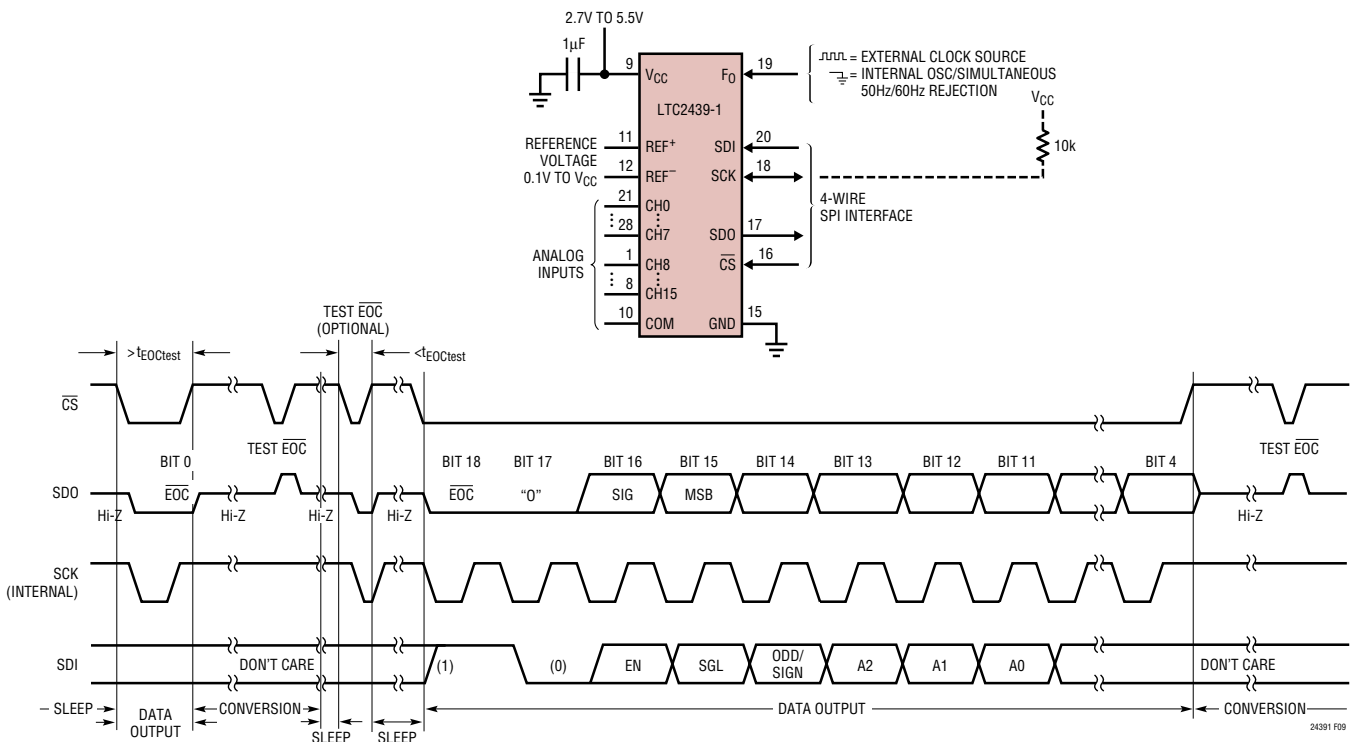
Figure 10. Internal Serial Clock, Reduced Data Output Length

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Internal Serial Clock, 3-Wire I/O, Continuous Conversion

This timing mode uses a 3-wire interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 11. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after V_{CC} exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period)

then immediately begins outputting data. The data input/ output cycle begins on the first rising edge of SCK and ends after the 19th rising edge. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 19th rising edge of SCK. After the 19th rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

PRESERVING THE CONVERTER ACCURACY

The LTC2439-1 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, antialiasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the accuracy capability of this part, some simple precautions are desirable.
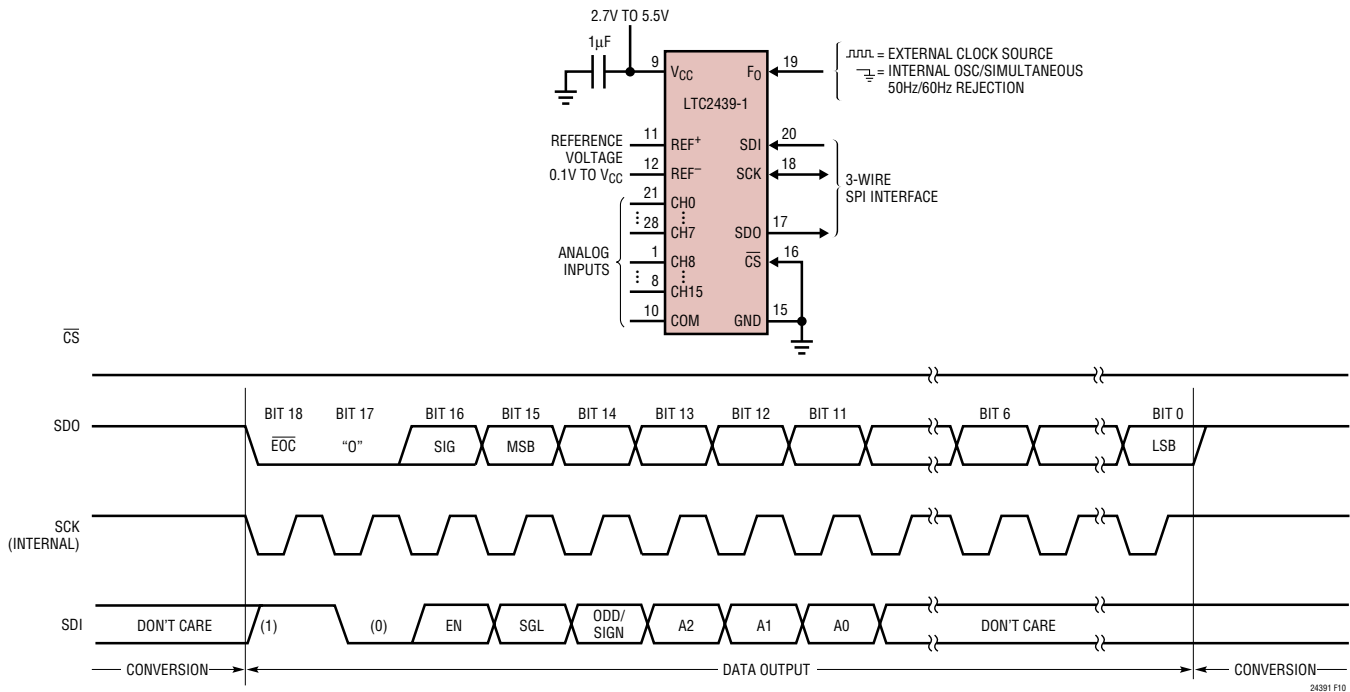
Figure 11. Internal Serial Clock, $\overline{CS}$ = 0 Continuous Operation

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Digital Signal Levels

The LTC2439-1's digital interface is easy to use. Its digital inputs (SDI, F_O, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100μs. However, some considerations are required to take advantage of the accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (SDI, F_O, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the power supply current may increase even if the signal in question is at a valid logic level. For micropower operation, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

During the conversion period, the undershoot and/or overshoot of a fast digital signal connected to the pins may severely disturb the analog to digital conversion process. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2439-1. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2439-1 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2439-1 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

An alternate solution is to reduce the edge rate of the control signals. It should be noted that using very slow edges will increase the converter power supply current during the transition time. The differential input and reference architecture reduce substantially the converter's sensitivity to ground currents.

Particular attention must be given to the connection of the F_O signal when the LTC2439-1 is used with an external conversion clock. This clock is active during the conversion time and the normal mode rejection provided by the internal digital filter is not very high at this frequency. A normal mode signal of this frequency at the converter reference terminals may result into DC gain and INL errors. A normal mode signal of this frequency at the converter input terminals may result into a DC offset error. Such perturbations may occur due to asymmetric capacitive coupling between the F_O signal trace and the converter input and/or reference connection traces. An immediate solution is to maintain maximum possible separation between the F_O signal trace and the input/reference signals. When the F_O signal is parallel terminated near the converter, substantial AC current is flowing in the loop formed by the F_O connection trace, the termination and the ground return path. Thus, perturbation signals may be inductively coupled into the converter input and/or reference. In this situation, the user must reduce to a minimum the loop area for the F_O signal as well as the loop area for the differential input and reference connections.

Driving the Input and Reference

The input and reference pins of the LTC2439-1 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage, these capacitors are switching between these four pins transferring small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 12.

For a simple approximation, the source impedance R_S driving an analog input pin (IN+, IN–, REF+ or REF–) can be considered to form, together with R_{SW} and C_{EQ} (see

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Figure 12), a first order passive network with a time constant $\tau = (R_S + R_{SW}) \cdot C_{EQ}$. The converter is able to sample the input signal with better than 1LSB accuracy if the sampling period is at least 11 times greater than the input circuit time constant τ. The sampling process on the four input analog pins is quasi-independent so each time constant should be considered by itself and, under worst-case circumstances, the errors may add.

When using the internal oscillator (F_O = LOW), the LTC2439-1's front-end switched-capacitor network is clocked at 69900Hz corresponding to a 14.3μs sampling period. Thus, for settling errors of less than 1LSB, the driving source impedance should be chosen such that $\tau \le 14.3\mu s/11 = 1.3\mu s$. When an external oscillator of frequency f_{EOSC} is used, the sampling period is $2/f_{EOSC}$ and, for a settling error of less than 1LSB, $\tau \le 0.18/f_{EOSC}$.

Input Current

If complete settling occurs on the input, conversion results will be unaffected by the dynamic input current. An incomplete settling of the input signal sampling process may result in gain and offset errors, but it will not degrade the INL performance of the converter. Figure 12 shows the mathematical expressions for the average bias currents flowing through the IN⁺ and IN⁻ pins as a result of the sampling charge transfers when integrated over a substantial time period (longer than 64 internal clock cycles).
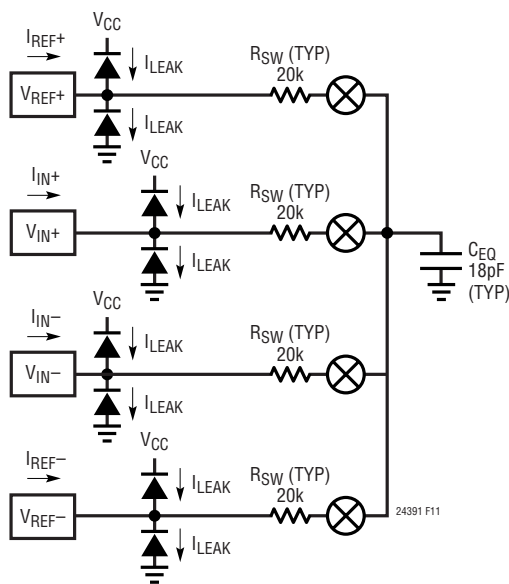
SWITCHING FREQUENCY
f_{SW} = 69900Hz INTERNAL OSCILLATOR (F_O = LOW)
$f_{SW} = 0.5 \cdot f_{EOSC}$ EXTERNAL OSCILLATOR

$$I\left(IN^+\right)_{AVG} = \frac{V_{IN} + V_{INCM} - V_{REFCM}}{0.5 \cdot R_{EQ}}$$

$$I\left(IN^-\right)_{AVG} = \frac{-V_{IN} + V_{INCM} - V_{REFCM}}{0.5 \cdot R_{EQ}}$$

$$I\left(REF^+\right)_{AVG} = \frac{1.5 \cdot V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \cdot R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \cdot R_{EQ}}$$

$$I\left(REF^-\right)_{AVG} = \frac{-1.5 \cdot V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \cdot R_{EQ}} + \frac{V_{IN}^2}{V_{REF} \cdot R_{EQ}}$$

where:

$$V_{REF} = REF^+ - REF^-$$

$$V_{REFCM} = \left(\frac{REF^+ + REF^-}{2}\right)$$

$$V_{IN} = IN^+ - IN^-$$

$$V_{INCM} = \left(\frac{IN^+ - IN^-}{2}\right)$$

$R_{EQ} = 3.97M\Omega$ INTERNAL OSCILLATOR 50Hz/60Hz Notch $\left(F_O = LOW\right)$

$R_{EQ} = \left(0.555 \cdot 10^{12}\right)/f_{EOSC}$ EXTERNAL OSCILLATOR

Figure 12. LTC2439-1 Equivalent Analog Input Circuit

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The effect of this input dynamic current can be analyzed using the test circuit of Figure 13. The C_{PAR} capacitor includes the LTC2439-1 pin capacitance (5pF typical) plus the capacitance of the test fixture used to obtain the results shown in Figures 14 and 15. A careful implementation can bring the total input capacitance ($C_{IN} + C_{PAR}$) closer to 5pF thus achieving better performance than the one predicted by Figures 14 and 15. For simplicity, two distinct situations can be considered.

For relatively small values of input capacitance (C_{IN} < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{IN} will deteriorate the converter offset and gain performance without significant benefits of signal filtering and the user is advised to avoid them. Nevertheless, when small values of C_{IN} are unavoidably present as parasitics of input multiplexers, wires, connectors or sensors, the LTC2439-1 can maintain its accuracy while operating with relative large values of source resistance as shown in Figures 14 and 15. These measured results may be slightly different from the first order approximation suggested earlier because they include the effect of the actual second order input network together with the nonlinear settling process of the input amplifiers. For small C_{IN} values, the settling on IN$^+$ and IN$^-$ occurs almost independently and there is little benefit in trying to match the source impedance for the two pins.

Larger values of input capacitors (C_{IN} > 0.01µF) may be required in certain configurations for antialiasing or general input signal filtering. Such capacitors will average the input sampling charge and the external source resistance will see a quasi constant input differential impedance. When F_O = LOW (internal oscillator and 50Hz/60Hz notch), the typical differential input resistance is 2MΩ which will generate a gain error of approximately 1LSB at full scale for each 60Ω of source resistance driving IN$^+$ or IN$^-$. When F_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential input resistance is $0.28 \cdot 10^{12}/f_{EOSC}\Omega$
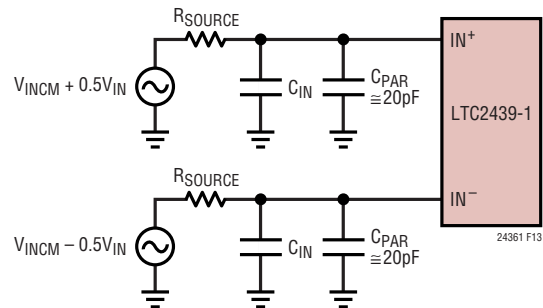
Figure 13. An RC Network at IN$^+$ and IN$^-$
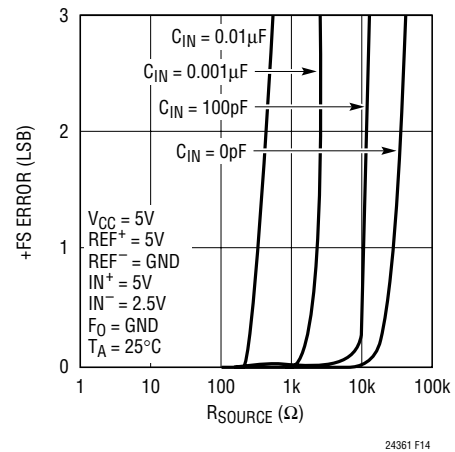
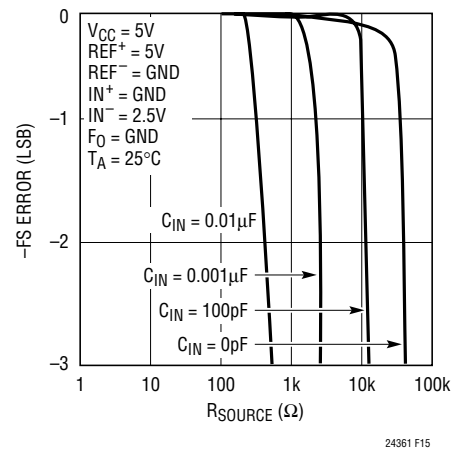Figure 14. +FS Error vs R_{SOURCE} at IN$^+$ or IN$^-$ (Small C_{IN})

Figure 15. –FS Error vs R_{SOURCE} at IN$^+$ or IN$^-$ (Small C_{IN})

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and each ohm of source resistance driving IN$^+$ or IN$^-$ will result in $1.11 \cdot 10^{-7} \cdot f_{EOSC}$ LSB gain error at full scale. The effect of the source resistance on the two input pins is additive with respect to this gain error. The typical +FS and –FS errors as a function of the sum of the source resistance seen by IN$^+$ and IN$^-$ for large values of C_{IN} are shown in Figures 16 and 17.

In addition to this gain error, an offset error term may also appear. The offset error is proportional with the mismatch between the source impedance driving the two input pins IN$^+$ and IN$^-$ and with the difference between the input and reference common mode voltages. While the input drive circuit nonzero source impedance combined with the converter average input current will not degrade the INL performance, indirect distortion may result from the modulation of the offset error by the common mode component of the input signal. Thus, when using large C_{IN} capacitor values, it is advisable to carefully match the source impedance seen by the IN$^+$ and IN$^-$ pins. When F_O = LOW (internal oscillator and 50Hz/60Hz notch), every 60Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 1LSB. When F_O is driven by an external oscillator with a frequency f_{EOSC}, every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $1.11 \cdot 10^{-7} \cdot f_{EOSC}$ LSB. Figure 18 shows the typical offset error due to input common mode voltage for various values of source resistance imbalance between the IN$^+$ and IN$^-$ pins when large C_{IN} values are used.

If possible, it is desirable to operate with the input signal common mode voltage very close to the reference signal common mode voltage as is the case in the ratiometric measurement of a symmetric bridge. This configuration eliminates the offset error caused by mismatched source impedances.

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by IN$^+$ and
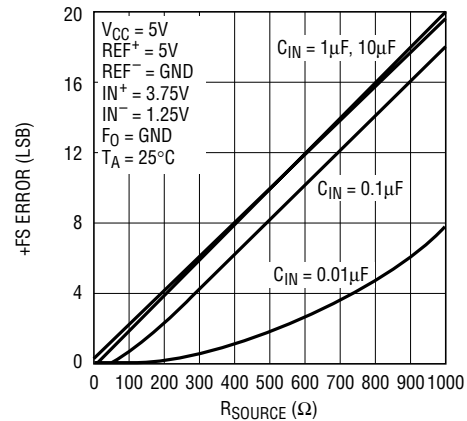

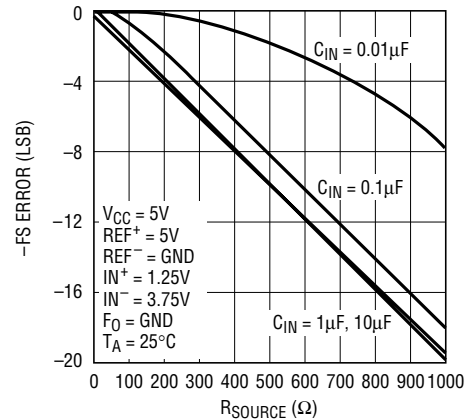Figure 16. +FS Error vs R_{SOURCE} at IN$^+$ or IN$^-$ (Large C_{IN})

Figure 17. –FS Error vs R_{SOURCE} at IN$^+$ or IN$^-$ (Large C_{IN})

A: ΔR_{IN} = +400Ω E: ΔR_{IN} = –100Ω
B: ΔR_{IN} = +200Ω F: ΔR_{IN} = –200Ω
C: ΔR_{IN} = +100Ω G: ΔR_{IN} = –400Ω
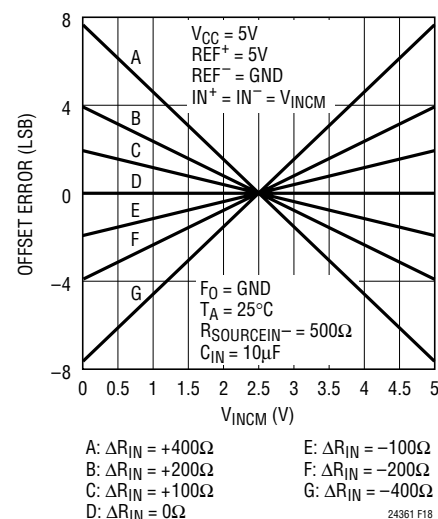D: ΔR_{IN} = 0Ω

Figure 18. Offset Error vs Common Mode Voltage (V_{INCM} = IN$^+$ = IN$^-$) and Input Source Resistance Imbalance (ΔR_{IN} = $R_{SOURCEIN+}$ – $R_{SOURCEIN-}$) for Large C_{IN} Values ($C_{IN} \geq 1\mu F$)

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IN⁻, the expected drift of the dynamic current, offset and gain errors will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 15k source resistance will create a 0LSB typical and 1LSB maximum offset voltage.

Reference Current

In a similar fashion, the LTC2439-1 samples the differential reference pins REF⁺ and REF⁻ transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in the same two distinct situations.

For relatively small values of the external reference capacitors (C_{REF} < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{REF} will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors (C_{REF} > 0.01µF) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge

and the external source resistance will see a quasi constant reference differential impedance. When F_O = LOW (internal oscillator and 50Hz/60Hz notch), the typical differential reference resistance is 1.4MΩ which will generate a gain error of approximately 1LSB full scale for each 40Ω of source resistance driving REF⁺ or REF⁻. When F_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential reference resistance is $0.20 \cdot 10^{12}/f_{EOSC}\Omega$ and each ohm of source resistance driving REF⁺ or REF⁻ will result in $1.54 \cdot 10^{-7} \cdot f_{EOSC}$LSB gain error at full scale. The effect of the source resistance on the two reference pins is additive with respect to this gain error. The typical +FS and –FS errors for various combinations of source resistance seen by the REF⁺ and REF⁻ pins and external capacitance C_{REF} connected to these pins are shown in Figures 19, 20, 21 and 22.

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. When F_O = LOW (internal oscillator and 50Hz/60Hz notch), every 1000Ω of source resistance driving REF⁺ or REF⁻ translates into about 1LSB additional INL error. When F_O is driven by an external oscillator with a frequency f_{EOSC}, every 100Ω of source resistance driving REF⁺ or REF⁻ translates into about $5.5 \cdot 10^{-7} \cdot f_{EOSC}$LSB additional INL error. Figure 23 shows the typical INL error due to the source resistance driving the REF⁺ or REF⁻ pins when large C_{REF} values are used. The effect of the source resistance on the two reference pins is additive with respect to this INL error. In general, matching of source
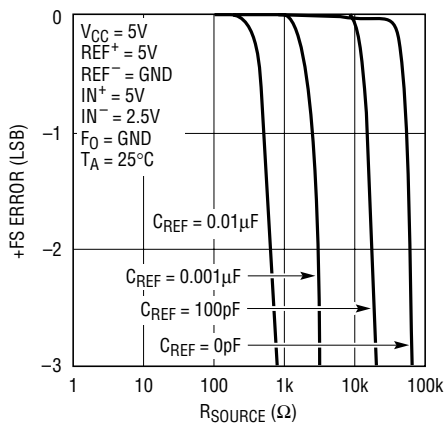

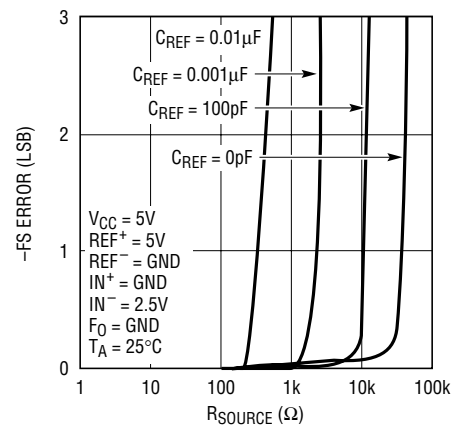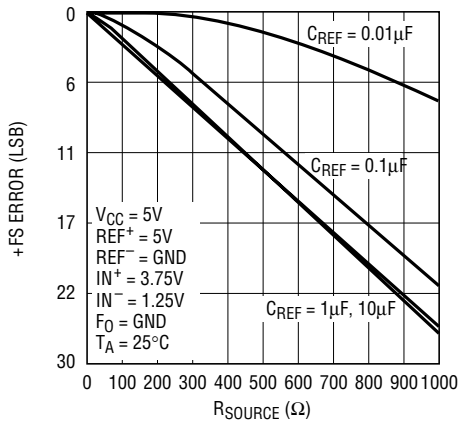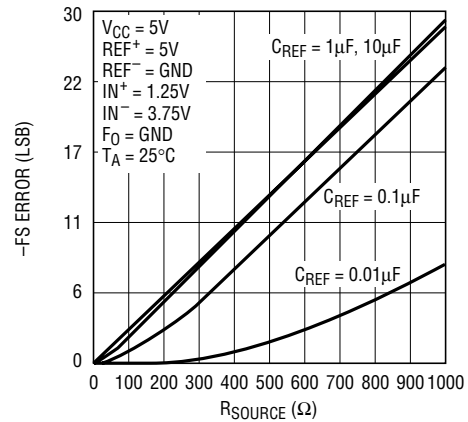Figure 19. +FS Error vs R_{SOURCE} at REF⁺ or REF⁻ (Small C_{IN})

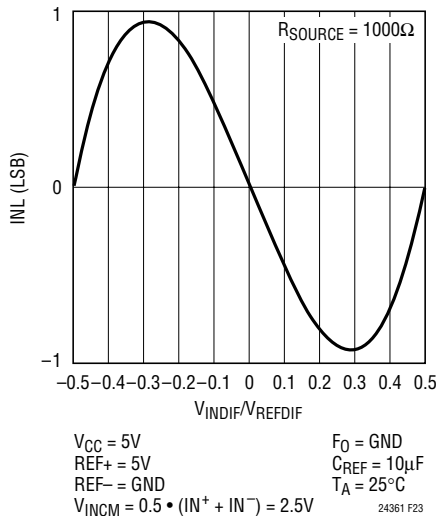Figure 20. –FS Error vs R_{SOURCE} at REF⁺ or REF⁻ (Small C_{IN})

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Figure 21. +FS Error vs R_{SOURCE} at REF+ and REF− (Large C_{REF})

Figure 22. −FS Error vs R_{SOURCE} at REF+ and REF− (Large C_{REF})

Figure 23. INL vs Differential Input Voltage (V_{IN} = IN+ − IN−) and Reference Source Resistance (R_{SOURCE} at REF+ and REF− for Large C_{REF} Values ($C_{REF} \geq 1\mu F$)

impedance for the REF+ and REF− pins does not help the gain or the INL error. The user is thus advised to minimize the combined source impedance driving the REF+ and REF− pins rather than to try to match it.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by REF+ and REF−, the expected drift of the dynamic

current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

Output Data Rate

When using its internal oscillator, the LTC2439-1 can produce up to 6.8 readings per second. The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock (F_O connected to an external oscillator), the LTC2439-1 output data rate can be increased as desired. The duration of the conversion phase is 20510/f_{EOSC}. If f_{EOSC} = 139,800Hz, the converter behaves as if the internal oscillator is used with simultaneous 50Hz/60Hz. There is no significant difference in the LTC2439-1 performance between these two operation modes.

An increase in f_{EOSC} over the nominal 139,800Hz will translate into a proportional increase in the maximum output data rate. This substantial advantage is nevertheless accompanied by three potential effects, which must be carefully considered.

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First, a change in f_{EOSC} will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2439-1's exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the IN$^+$ and IN$^-$ pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of f_{EOSC}. If small external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the effect of the external source resistance upon the LTC2439-1 typical performance can be inferred from Figures 14, 15, 19 and 20 in which the horizontal axis is scaled by $139,800/f_{EOSC}$.

Third, an increase in the frequency of the external oscillator above 460800Hz (a more than 3× increase in the output data rate) will start to decrease the effectiveness of the internal autocalibration circuits. This will result in a progressive degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 100 readings per second are shown in Figures 24, 25, 26, 27, 28 and 29. In order to obtain the highest possible level of accuracy from this converter at output data rates above 20 readings per second, the user is advised to maximize the power supply voltage used and to limit the maximum ambient operating temperature. In certain circumstances, a reduction of the differential reference voltage may be beneficial.

Increasing Input Resolution by Reducing Reference Voltage

The resolution of the LTC2439-1 can be increased by reducing the reference voltage. It is often necessary to amplify low level signals to increase the voltage resolution of ADCs that cannot operate with a low reference voltage. The LTC2439-1 can be used with reference voltages as low as 100mV, corresponding to a ±50mV input range with full 16-bit resolution. Reducing the reference voltage is functionally equivalent to amplifying the input signal, however no amplifier is required.

The LTC2439-1 has a 76µV LSB when used with a 5V reference, however the thermal noise of the inputs is $1µV_{RMS}$ and is independent of reference voltage. Thus reducing the reference voltage will increase the resolution at the inputs as long as the LSB voltage is significantly larger than $1µV_{RMS}$. A 325mV reference corresponds to a 5µV LSB, which is approximately the peak-to-peak value of the $1µV_{RMS}$ input thermal noise. At this point, the output code will be stable to ±1LSB for a fixed input. As the reference is decreased further, the measured noise will approach $1µV_{RMS}$.

Figure 30 shows two methods of dividing down the reference voltage to the LTC2439-1. Where absolute accuracy is required, a precision divider such as the Vishay MPM series dividers in a SOT-23 package may be used. A 51:1 divider provides a 98mV reference to the LTC2439-1 from a 5V source. The resulting ±49mV input range and 1.5µV LSB is suitable for thermocouple and 10mV full-scale strain gauge measurements.

If high initial accuracy is not critical, a standard 2% resistor array such as the Panasonic EXB series may be used. Single package resistor arrays provide better temperature stability than discrete resistors. An array of eight resistors can be configured as shown to provide a 294mV reference to the LTC2439-1 from a 5V source. The fully differential property of the LTC2439-1 reference terminals allow the reference voltage to be taken from four central resistors in the network connected in parallel, minimizing drift in the presence of thermal gradients. This is an ideal reference for medium accuracy sensors such as silicon micromachined pressure and force sensors. These devices typically have accuracies on the order of 2% and full-scale outputs of 50mV to 200mV.
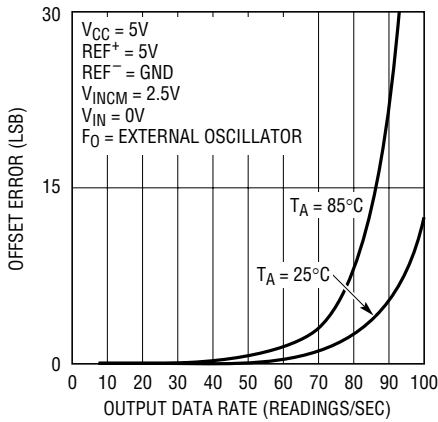
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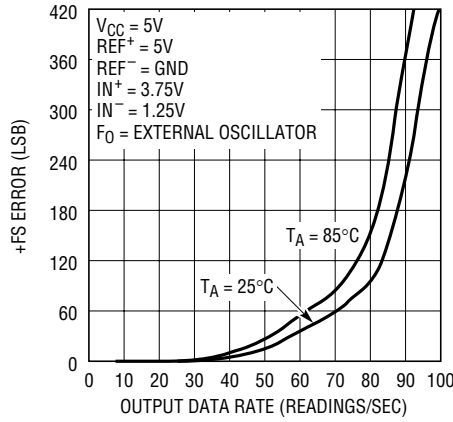Figure 24. Offset Error vs Output
Data Rate and Temperature

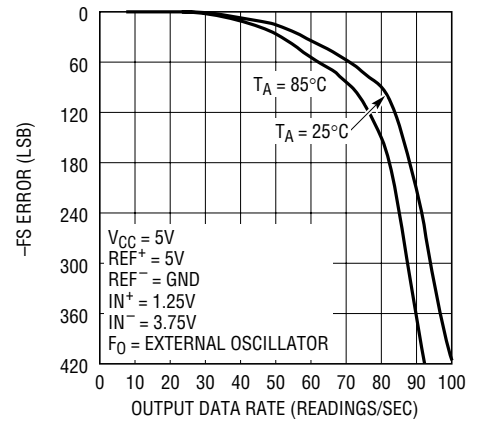Figure 25. +FS Error vs Output
Data Rate and Temperature

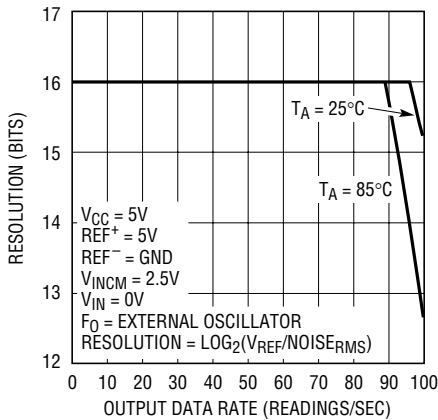Figure 26. –FS Error vs Output
Data Rate and Temperature

Figure 27. Resolution (Noise$_{RMS}$ ≤ 1LSB)
vs Output Data Rate and Temperature

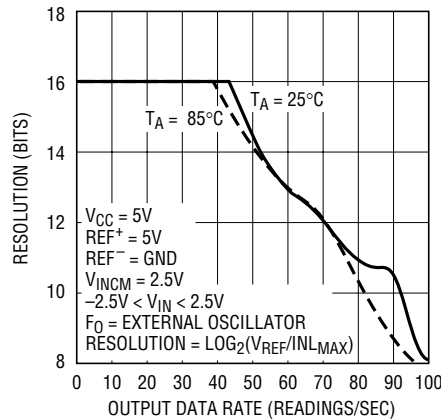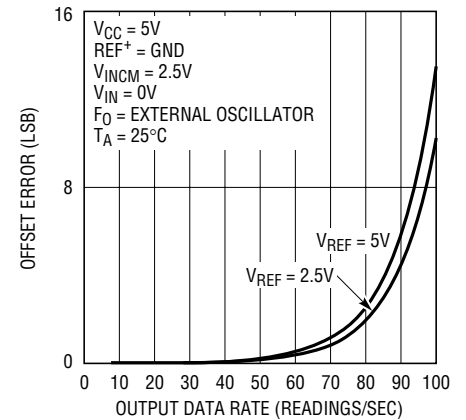Figure 28. Resolution (INL$_{MAX}$ ≤ 1LSB)
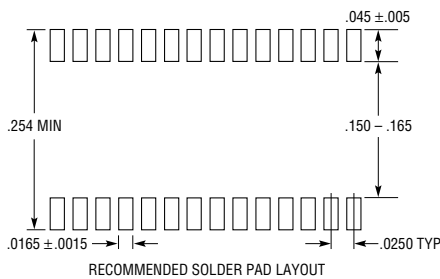vs Output Data Rate and Temperature

Figure 29. Offset Error vs Output
Data Rate and Reference Voltage

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{INCHES}{(MILLIMETERS)}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
 SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
 FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
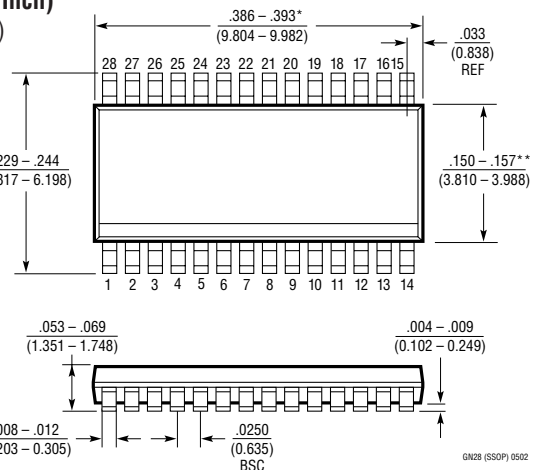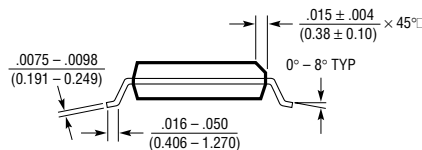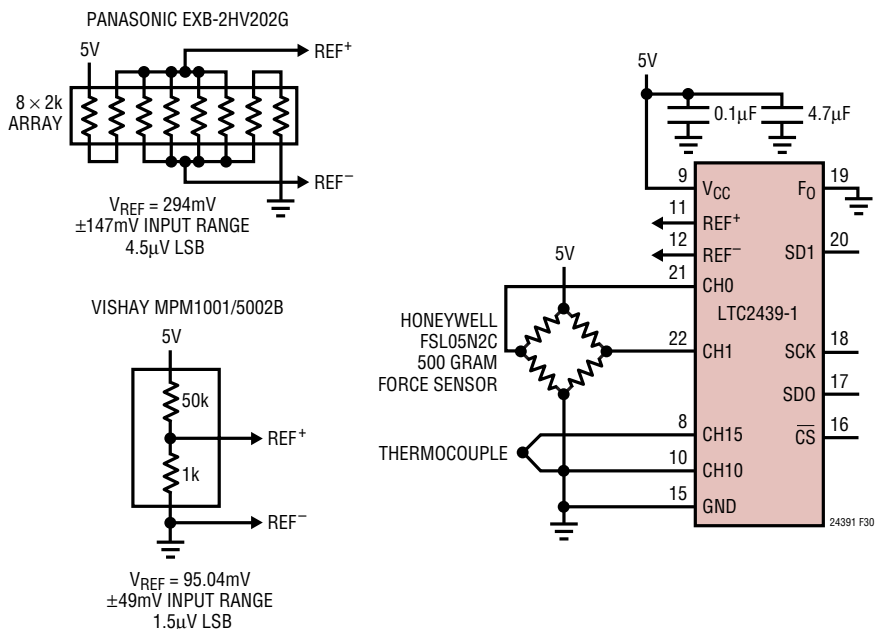
GN28 (SSOP) 0502

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TYPICAL APPLICATION

Figure 30. Increased Resolution Bridge/Temperature Measurement

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise, Charge Balanced Switching, Low Power
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1461	Micropower Precision LDO Reference	High Accuracy 0.04% Max, 3ppm/°C Max Drift
LTC2400	24-Bit, No Latency ΔΣ ADC in SO-8	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200μA
LTC2401/LTC2402	1-/2-Channel, 24-Bit, No Latency ΔΣ ADC in MSOP	0.6ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200μA
LTC2404/LTC2408	4-/8-Channel, 24-Bit, No Latency ΔΣ ADC	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200μA
LTC2410	24-Bit, Fully Differential, No Latency ΔΣ ADC	0.16ppm Noise, 2ppm INL, 3ppm Total Unadjusted Error, 200μA
LTC2411	24-Bit, No Latency ΔΣ ADC in MSOP	1.45μV_{RMS} Noise, 2ppm INL
LTC2411-1	24-Bit, Simultaneous 50Hz/60Hz Rejection ΔΣ ADC	0.3ppm Noise, 2ppm INL, Pin Compatible with LTC2411
LTC2412	2-Channel, 24-Bit, Pin Compatible with LTC2439-1	800nV Noise, 2ppm INL, 3ppm TUE, 200μA
LTC2413	24-Bit, No Latency ΔΣ ADC	Simultaneous 50Hz/60Hz Rejection, 800nV$_{RMS}$ Noise
LTC2414/LTC2418	8-/16-Channel, 24-Bit No Latency ΔΣ ADC	0.2ppm Noise, 2ppm INL, 3ppm Total Unadjusted Error, 200μA
LTC2415	24-Bit, No Latency ΔΣ ADC with 15Hz Output Rate	Pin Compatible with the LTC2410
LTC2420	20-Bit, No Latency ΔΣ ADC in SO-8	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2400
LTC2424/LTC2428	4-/8-Channel, 20-Bit, No Latency ΔΣ ADCs	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2404/LTC2408
LTC2433-1	Differential Single Channel 16-Bit ΔΣ ADC	Low Noise, 16-Bits at ±50mV Input Range
LTC2436-1	2-Channel Differential 16-Bit ΔΣ ADC	Low Noise, 16-Bits at ±50mV Input Range
LTC2440	High Speed, Low Noise 24-Bit ADC	4kHz Output Rate, 200nV Noise, 24.6 ENOBs
LTC2444/45/48/49	8-/16-Channel High Speed, Low Noise 24-Bit ADC	4kHz MUX Rate, 200nV Noise

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