National Semiconductor

April 8, 2009

ADC16V130

16-Bit, 130 MSPS A/D Converter with LVDS Outputs

General Description

The ADC16V130 is a monolithic high performance CMOS analog-to-digital converter capable of converting analog input signals into 16-bit digital words at rates up to 130 Mega Samples Per Second (MSPS). This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and external component count while providing excellent dynamic performance. Automatic power-up calibration enables excellent dynamic performance and reduces part-to-part variation, and the ADC16V130 could be re-calibrated at any time by asserting and then de-asserting power-down. An integrated low noise and stable voltage reference and differential reference buffer amplifier easies board level design. On-chip duty cycle stabilizer with low additive jitter allows wide duty cycle range of input clock without compromising its dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.4 GHz. The digital data is provided via full data rate LVDS outputs – making possible the 64-pin, 9mm x 9mm LLP package. The ADC16V130 operates on dual power supplies +1.8V and +3.0V with a power-down feature to reduce the power consumption to very low levels while allowing fast recovery to full operation.

Features

- Dual Supplies: 1.8V and 3.0V operation
- On chip automatic calibration during power-up
- Low power consumption
- Multi-level multi-function pins for CLK/DF and PD
- Power-down and sleep modes
- On chip precision reference and sample-and-hold circuit
- On chip low jitter duty-cycle stabilizer
- Offset binary or 2's complement data format
- Full data rate LVDS output port
- 64-pin LLP package (9x9x0.8, 0.5mm pin-pitch)

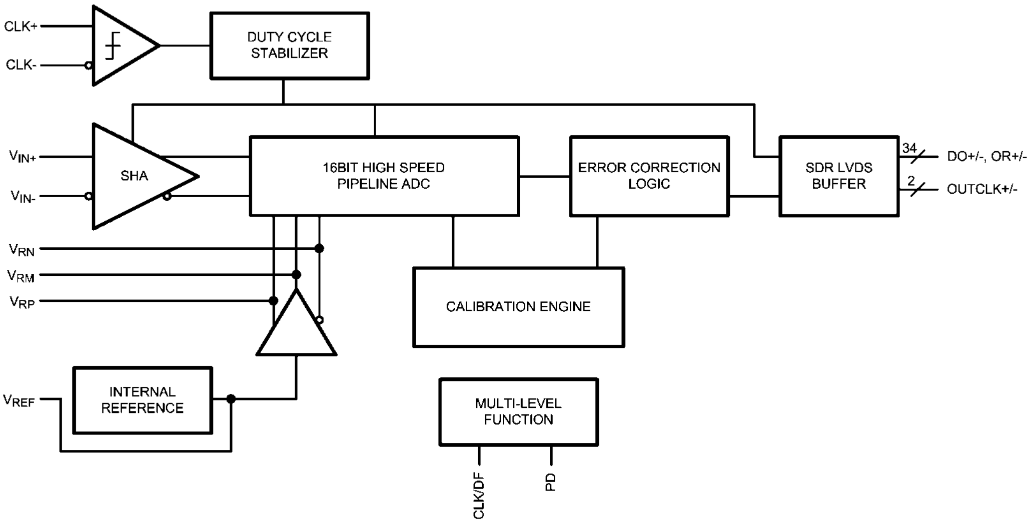
Key Specifications

Resolution	16 Bits
Conversion Rate	130 MSPS
SNR	
(f_{IN} = 10MHz)	78.5 dBFS (typ)
(f_{IN} = 70MHz)	77.8 dBFS (typ)
(f_{IN} = 160MHz)	76.7 dBFS (typ)
SFDR	
(f_{IN} = 10 MHz)	95.5 dBFS (typ)
(f_{IN} = 70MHz)	92.0 dBFS (typ)
(f_{IN} = 160MHz)	90.6 dBFS (typ)
Full Power Bandwidth	1.4 GHz (typ)
Power Consumption	
Core	650 mW (typ)
LVDS Driver	105 mW (typ)
Total	755 mW (typ)
Operating Temperature Range	-40°C ~ 85°C

Applications

- High IF Sampling Receivers
- Multi-carrier Base Station Receivers GSM/EDGE, CDMA2000, UMTS, LTE and WiMax
- Test and Measurement Equipment
- Communications Instrumentation
- Data Acquisition
- Portable Instrumentation

Block Diagram



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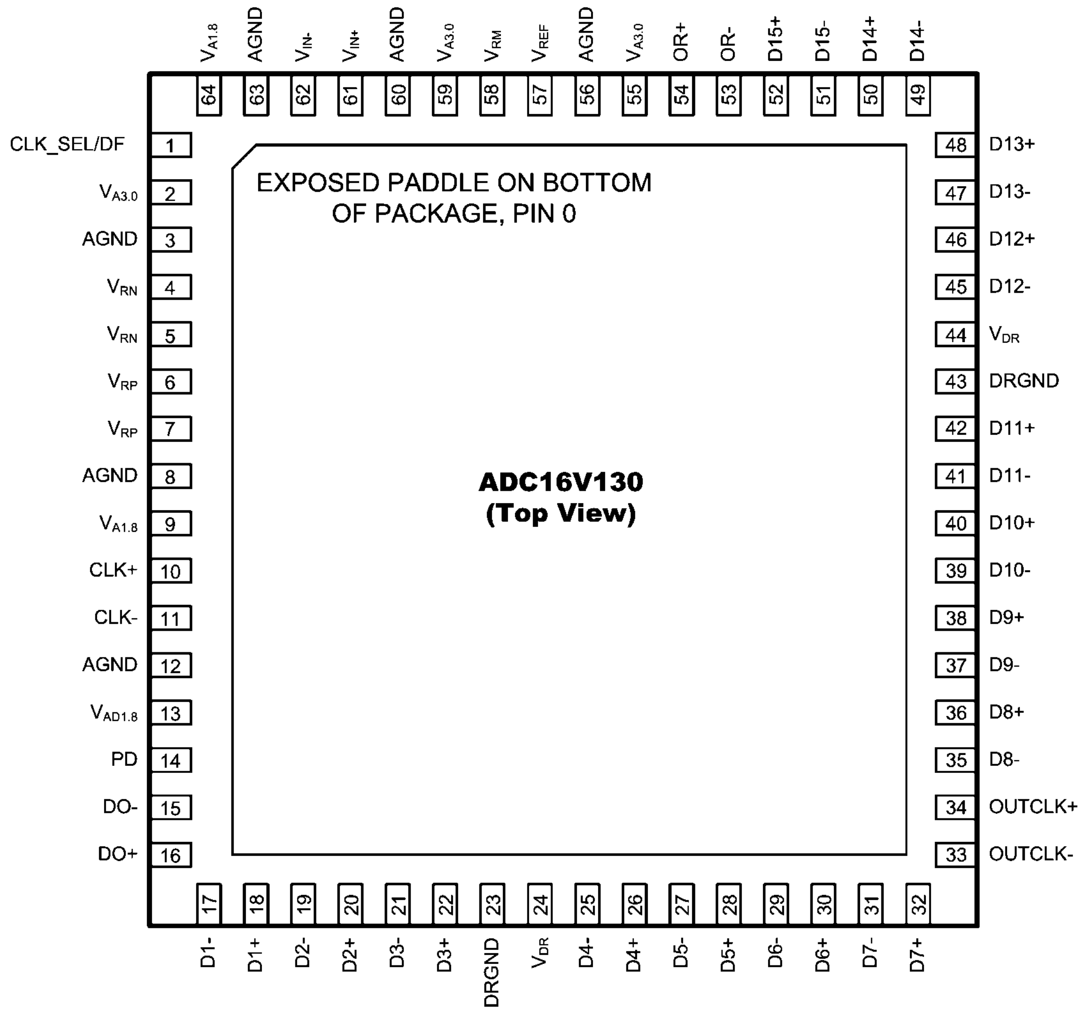
Connection Diagram


$V_{A1.8}$
AGND
V_{IN-}
V_{IN+}
AGND
$V_{A3.0}$
V_{RM}
V_{REF}
AGND
$V_{A3.0}$
OR+
OR-
D15+
D15-
D14+
D14-
64
63
62
61
60
59
58
57
56
55
54
53
52
51
50
49
CLK_SEL/DF 1
$V_{A3.0}$ 2
AGND 3
V_{RN} 4
V_{RN} 5
V_{RP} 6
V_{RP} 7
AGND 8
$V_{A1.8}$ 9
CLK+ 10
CLK- 11
AGND 12
$V_{AD1.8}$ 13
PD 14
DO- 15
DO+ 16
EXPOSED PADDLE ON BOTTOM
OF PACKAGE, PIN 0
ADC16V130
(Top View)
48 D13+
47 D13-
46 D12+
45 D12-
44 V_{DR}
43 DRGND
42 D11+
41 D11-
40 D10+
39 D10-
38 D9+
37 D9-
36 D8+
35 D8-
34 OUTCLK+
33 OUTCLK-
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
D1-
D1+
D2-
D2+
D3-
D3+
DRGND
V_{DR}
D4-
D4+
D5-
D5+
D6-
D6+
D7-
D7+

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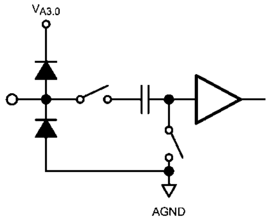
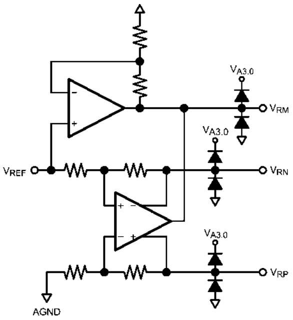
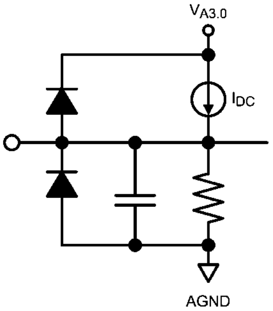
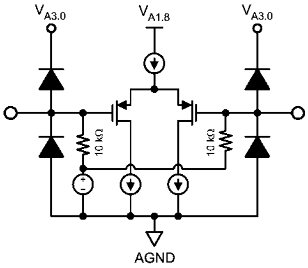
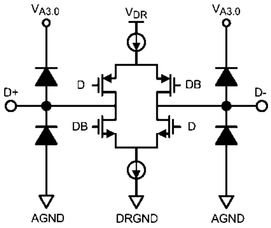
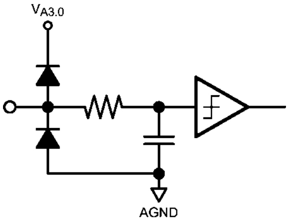
Ordering Information

Industrial (−40°C ≤ T_A ≤ +85°C)	Package
ADC16V130CISQ	64 Pin LLP
ADC16V130EB	Evaluation Board

Pin Descriptions

Pin No.	Symbol	Equivalent Circuit	Function and Connection
ANALOG I/O			
61	V_{IN+}		Differential analog input pins. The differential full-scale input signal level is 2.4Vpp as default. Each input pin signal centered on a common mode voltage, V_{CM}.
62	V_{IN-}		
6,7	V_{RP}	 $V_{A3.0}$ V_{RM} $V_{A3.0}$ V_{REF} V_{RN} $V_{A3.0}$ V_{RP} AGND	Upper reference voltage. This pin should not be used to source or sink current. The decoupling capacitor to AGND (low ESL 0.1µF) should be placed very close to the pin to minimize stray inductance. V_{RP} needs to be connected to V_{RN} through a low ESL 0.1µF and a low ESR 10µF capacitors in parallel.
4,5	V_{RN}		Lower reference voltage. This pin should not be used to source or sink current. The decoupling capacitor to AGND (low ESL 0.1µF) should be placed very close to the pin to minimize stray inductance. V_{RN} needs to be connected to V_{RP} through a low ESL 0.1µF and a low ESR 10µF capacitors in parallel.
58	V_{RM}		Common mode voltage The decoupling capacitor to AGND (low ESL 0.1µF) should be placed as close to the pin as possible to minimize stray inductance. It is recommended to use V_{RM} to provide the common mode voltage for the differential analog inputs.
57	V_{REF}		Internal reference voltage output / External reference voltage input. By default, this pin is the output for the internal 1.2V voltage reference. This pin should not be used to sink or source current and should be decoupled to AGND with a 0.1µF, low ESL capacitor. The decoupling capacitors should be placed as close to the pins as possible to minimize inductance and optimize ADC performance. The size of decoupling capacitor should not be larger than 0.1µF, otherwise dynamic performance after power-up calibration can drop due to the long V_{REF} settling. This pin can also be used as the input for a low noise external reference voltage. The output impedance for the internal reference at this pin is 9 kΩ and this can be overdriven provided the impedance of the external source is <<9 kΩ. Careful decoupling is just as essential when an external reference is used. The 0.1µF low ESL decoupling capacitor should be placed as close to this pin as possible. The Input differential voltage swing is equal to 2 * V_{REF}.
10	CLK+	 $V_{A3.0}$ $V_{A1.8}$ $V_{A3.0}$ 10 kΩ 10 kΩ AGND	Differential clock input pins. DC biasing is provided internally. For single-ended clock mode, drive CLK+ through AC coupling while decoupling CLK- pin to AGND.
11	CLK–		

Pin No.	Symbol	Equivalent Circuit	Function and Connection
DIGITAL I/O			
15 – 22 25 – 32 35 – 42 45 – 52	D0+/- to D3+/- D4+/- to D7+/- D8+/- to D11+/- D12+/- to D15 +/-	 $V_{A3.0}$ V_{DR} $V_{A3.0}$ D+ D DB D- DB D AGND DRGND AGND	LVDS Data Output. The 16-bit digital output of the data converter is provided on these ports in a full data rate manner. A 100 Ω termination resistor must be placed between each pair of differential signals at the far end of the transmission line.
53, 54	OR+/-		Over-Range Indicator. Active High. This output is set High when analog input signal exceeds full scale of 16 bit conversion range (<0,> 65535). This signal is asserted coincidently with the over-range data word. A 100 Ω termination resistor must be placed between the differential signals at the far end of the transmission.
33, 34	OUTCLK+/-		Output Clock. This pin is used to clock the output data. It has the same frequency as the sampling clock. One word of data is output in each cycle of this signal. A 100 Ω termination resistor must be placed between the differential clock signals at the far end of the transmission line. The rising edge of this signal should be used to capture the output data. See the detail Section on *Timing Diagrams* .
14	PD		This is a three-state pin. **PD = $V_{A3.0}$**, then Power Down is enabled. In the Power Down state, only the reference voltage circuitry remains active and power dissipation is reduced. **PD =$V_{A3.0}$ * (2/3)**, then Sleep mode is enabled. In Sleep mode is similar to Power Down mode - it consumes more power but has a faster recovery time. **PD = AGND**, then Normal operation mode is turned on.
1	CLK_SEL/DF		This is a four-state pin controlling two parameters: input clock selection and output data format. **CLK_SEL/DF = $V_{A3.0}$**, then CLK+ and CLK– are configured as a differential clock input and the output data format is 2's complement. **CLK_SEL/DF = $V_{A3.0}$ * (2/3)**, then CLK+ and CLK– are configured as a differential clock input and the output data format is offset binary. **CLK_SEL/DF = $V_{A3.0}$ * (1/3)**, then CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is 2's complement. **CLK_SEL/DF = AGND**, then CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is offset binary.
POWER SUPPLIES			
2, 55, 59	$V_{A3.0}$	Analog Power	3.0V Analog Power Supply. These pins should be connected to a quiet source and should be decoupled to AGND with 0.1μF capacitors located close to the power pins.
9, 64	$V_{A1.8}$	Analog Power	1.8V Analog Power Supply. These pins should be connected to a quiet source and should be decoupled to AGND with 0.1μF capacitors located close to the power pins.
13	$V_{AD1.8}$	Analog/Digital Power	1.8V Analog/Digital Power Supply. These pins should be connected to a quiet source and should be decoupled to AGND with 0.1μF capacitors located close to the power pins.
0, 3, 8, 12, 56, 60, 63	AGND	Analog Ground	Analog Ground Return. The exposed pad (Pin 0) on back of the package must be soldered to ground plane to ensure rated performance.

Pin No.	Symbol	Equivalent Circuit	Function and Connection
24, 44	V_{DR}	Power	Output Driver Power Supply. This pin should be connected to a quiet voltage source and be decoupled to DRGND with a 0.1µF capacitor close to the power pins.
23, 43	DRGND	Ground	Output Driver Ground Return.

Absolute Maximum Ratings (Notes , 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_{A3.0}$)	−0.3V to 4.2V
Supply Voltage ($V_{A1.8}$, $V_{AD1.8}$, V_{DR})	−0.3V to 2.35V
Voltage at any Pin except D0-D15, OVR, OUTCLK, CLK, V_{IN}	−0.3V to ($V_{A3.0}$ +0.3V) (Not to exceed 4.2V)
Voltage at CLK, V_{IN} Pins	-0.3V to (V_{DR} +0.3V) (Not to exceed 2.35V)
Voltage at D0-D15, OR, OUTCLK Pins	0.3V to (V_{DR} + 0.3V) (Not to exceed 2.35V)
Input Current at any pin (Note 3)	5 mA
Storage Temperature Range	-65°C to +150°C
ESD Rating(Note 4)	
Machine Model	200 V
Human Body Model	2000 V

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 5)

Operating Ratings (Notes 1,)

Specified Temperature Range:	-40°C to +85°C
3.0V Analog Supply Voltage Range: ($V_{A3.0}$)	+2.7V to +3.6V
1.8V Supply Voltage Range: $V_{A1.8}$, $V_{AD1.8}$, V_{DR}	+1.7V to +1.9V
Clock Duty Cycle	30/70 %

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	**Parameter**	**Conditions**	**Typical** (Note 6)	**Limits**	**Units (Limits)**
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**16**	Bits (min)
INL	Integral Non Linearity		±1.5		LSB
DNL	Differential Non Linearity		±0.45		LSB
PGE	Positive Gain Error		-4.2		%FS
NGE	Negative Gain Error		3.7		%FS
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)		0.12		%FS
	Under Range Output Code		0	**0**	
	Over Range Output Code		65535	**65535**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{CM}	Common Mode Input Voltage	V_{RM} is the common mode reference voltage	V_{RM} ±0.05		V
V_{RM}	Reference Ladder Midpoint Output Voltage		1.15		V
V_{REF}	Internal Reference Voltage		1.20		V
	Differential Analog Input Range	Internal Reference	2.4		V_{PP}

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Limits	Units
	Resolution with no missing codes			**16**	Bits
DR	Dynamic Range	0V analog input is applied	79		dBFS
SNR	Signal-to-Noise Ratio (Note 9)	Fin = 10 MHz	78.5		dBFS
		Fin = 40 MHz	78.2		dBFS
		Fin = 70 MHz	77.8		dBFS
		Fin = 160 MHz	76.7	**75.5**	dBFS
		Fin = 240 MHz	75.6		dBFS
SFDR	Single-tone Spurious Free Dynamic Range (Note 9)	Fin = 10 MHz	95.5		dBFS
		Fin = 40 MHz	91		dBFS
		Fin = 70 MHz	92		dBFS
		Fin = 160 MHz	90.6	**87**	dBFS
		Fin = 240 MHz	85.3		dBFS
THD	Total Harmonic Distortion (Note 9)	Fin = 10 MHz	-91.5		dBFS
		Fin = 40 MHz	-88.4		dBFS
		Fin = 70 MHz	-89.4		dBFS
		Fin = 160 MHz	-87.1	**-81**	dBFS
		Fin = 240 MHz	-82.8		dBFS
H2	Second-order Harmonic(Note 9)	Fin = 10 MHz	-95.5		dBFS
		Fin = 40 MHz	-104.1		dBFS
		Fin = 70 MHz	-95.6		dBFS
		Fin = 160 MHz	-91.5	**-88**	dBFS
		Fin = 240 MHz	-85.3		dBFS
H3	Third-order Harmonic (Note 9)	Fin = 10 MHz	-98.3		dBFS
		Fin = 40 MHz	-89.4		dBFS
		Fin = 70 MHz	-92		dBFS
		Fin = 160 MHz	-90.6	**-87**	dBFS
		Fin = 240 MHz	-87.8		dBFS
Spur-H2/3	Worst Harmonic or Spurious Tone excluding H2 and H3(Note 9)	Fin = 10 MHz	106		dBFS
		Fin = 40 MHz	103.2		dBFS
		Fin = 70 MHz	104.1		dBFS
		Fin = 160 MHz	101.5	**94**	dBFS
		Fin = 240 MHz	98.4		dBFS
SINAD	Signal-to-Noise and Distortion Ratio (Note 9)	Fin = 10 MHz	78.3		dBFS
		Fin = 40 MHz	77.8		dBFS
		Fin = 70 MHz	77.5		dBFS
		Fin = 160 MHz	76.3		dBFS
		Fin = 240 MHz	74.8		dBFS
ENOB	Effective Number of Bits	Fin = 10 MHz	12.7		Bits
		Fin = 40 MHz	12.6		Bits
		Fin = 70 MHz	12.6		Bits
		Fin = 160 MHz	12.4		Bits
		Fin = 240 MHz	12.1		Bits
	Full Power Bandwidth	-3dB Compression Point	1.4		GHz

Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
$I_{A3.0}$	Analog 3.0V Supply Current	Full Operation(Note 12)	174.5	208	mA (max)
$I_{A1.8}$	Analog 1.8V Supply Current	Full Operation(Note 12)	36	42	mA (max)
$I_{AD1.8R}$	Digital 1.8V Supply Current	Full Operation (Note 12)	34	41	mA (max)
I_{DR}	Output Driver Supply Current	Full Operation	58.3		mA
	Core Power Consumption	Excludes I_{DR} (Note 12)	650	773	mW (max)
	Driver Power Consumption	Current drawn from the V_{DR} supply; Fin = 10 MHz Rterm = 100Ω	105		mW
	Total Power Consumption	Normal operation; Fin = 10 MHz	755		mW
		Power down state, with external clock	3		mW
		Sleep state, with external clock	30		mW

LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS DC SPECIFICATIONS (apply to pins DO to D15, OR)						
V_{OD}	Output Differential Voltage	100 Ω Differential Load	175	250	325	mV
V_{OS}	Output Offset Voltage	100 Ω Differential Load	1.15	1.2	1.25	V
I_{OS}	Output Short Circuit Current	0 Ω Differential Load		2.5		mA
I_{OZ}	Output Open Circuit Current	Termination is open	-20	± 1	20	μA

Timing Specifications

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DRGND = 0V, $V_{A3.0}$= +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, Internal V_{REF} = +1.2V, f_{CLK} = 130 MHz, V_{CM} = V_{RM}, C_L = 5 pF, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Parameter	Conditions	Typ	Limits	Units
Input Clock Frequency			**130**	MHz (max)
Minimum Clock Frequency		1		MHz (min)
Data Output Setup Time (Tsu) (Note 10)	Measured @ Vdr/2; Fclk = 130 MHz.	3.3	**2.5**	nS (min)
Data Output Hold Time (Th) (Note 10)	Measured @ Vdr/2; Fclk = 130 MHz.	3.3	**2.5**	nS (min)
Pipeline Latency(Note 11)		11		Clock Cycles
Aperture Jitter		80		fS rms
Power-Up Time	From assertion of Power to specified level of performance.	$0.5+ 10^3*(2^{22}+2^{16})/FCLK$		mS
Power-Down Recovery Time	From de-assertion of power down mode to output data available.	$0.1+ 10^3*(2^{19}+2^{16})/FCLK$		mS
Sleep Recovery Time	From de-assertion of sleep mode to output data available.	100		μS

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

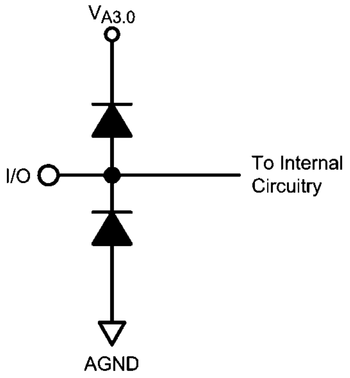
Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Note 4: Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω.

Note 5: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 6: Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 7: The inputs are protected as shown below. Input voltage magnitudes above $V_{A3.0}$ or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



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Note 8: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 9: This parameter is specified in units of dBFS – indicating the equivalent value that would be attained with a full-scale input signal.

Note 10:) This parameter is a function of the CLK frequency - increasing directly as the frequency is lowered. At frequencies less than 130 MHz, use the following formulae to calculate the setup and hold times:

For Data and OR+/- Outputs:	Tsu = ½*Tp – 0.5 ns (typical)
For Data and OR+/- Outputs:	Th = ½*Tp – 0.5 ns (typical)

where Tp = CLK input period = OUTCLK period

Note 11: Input signal is sampled with the falling edge of the CLK input.

Note 12: This parameter is guaranteed only at 25°C. For power dissipation over temperature range, refer to Core Power vs. Temperature plot in *Typical Performance Characteristics, Dynamic Performance*

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and the time when data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC16V130 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages ($V_{IN+} – V_{IN-}$) required to cause a transition from code 32767LSB and 32768LSB with offset binary data format.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the power of input signal to the total power of all other spectral components below one-half the sampling frequency, not including harmonics and DC.

SIGNAL TO NOISE AND DISTORTION (SINAD) Is the ratio, expressed in dB, of the power of the input signal to the total power of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the power of input signal and the peak spurious signal power, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the total power of the first seven harmonic to the input signal power. THD is calculated as:

$$\mathrm{THD} = 20\log_{10}\sqrt{\frac{f_2^2 + f_3^2 + \ldots + f_8^2}{f_1^2}}$$

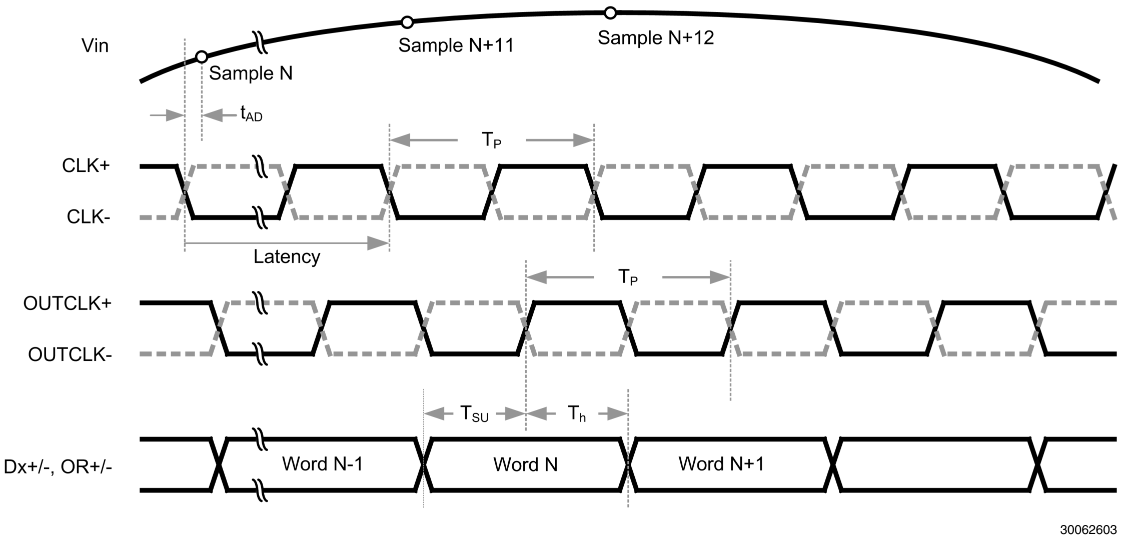
where f_1^2 is the power of the fundamental frequency and f_2^2 through f_8^2 are the powers of the first seven harmonics in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM or H2) is the difference expressed in dB, from the power of its 2nd harmonic level to the power of the input signal.

THIRD HARMONIC DISTORTION (3RD HARM or H3) is the difference expressed in dB, from the power of the 3nd harmonic level to the power of the input signal.

HIGHEST SPURIOUS EXCEPT H2 and H3 (Spur-H2/3) is the difference, expressed in dB, between the power of input signal and the peak spurious signal power except H2 and H3, where a spurious signal is any signal present in the output spectrum that is not present at the input.

Timing Diagrams


Vin
Sample N
Sample N+11
Sample N+12
t_{AD}
T_P
CLK+
CLK-
Latency
OUTCLK+
OUTCLK-
T_P
T_{SU}
T_h
Dx+/-, OR+/-
Word N-1
Word N
Word N+1
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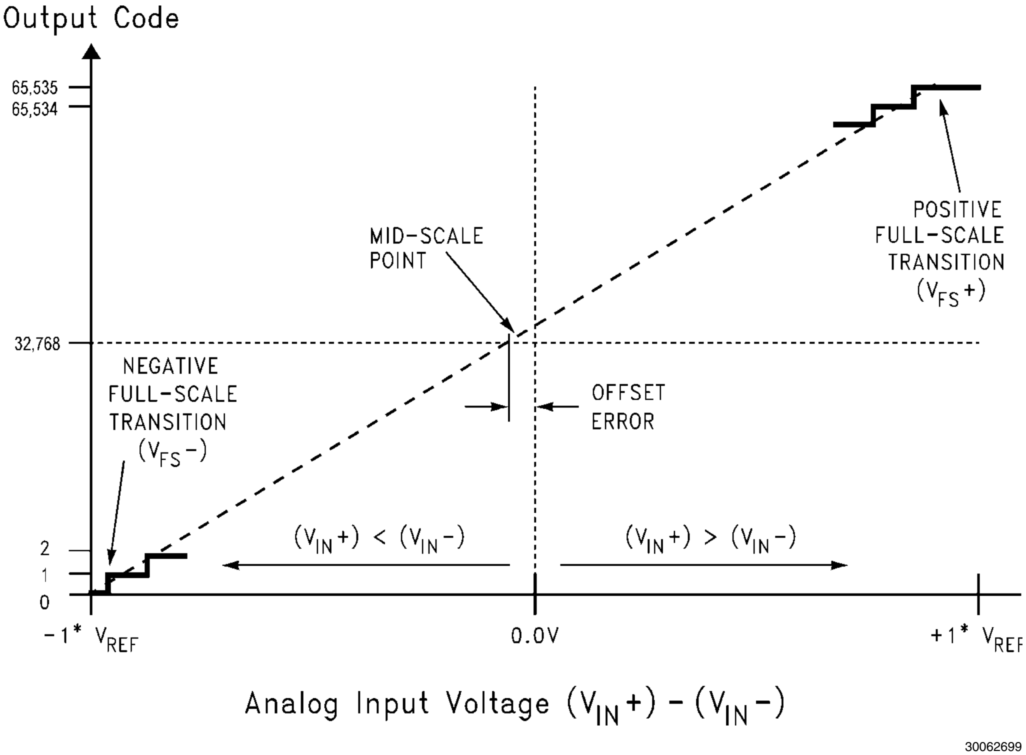
Digital Output Timing

Transfer Characteristic

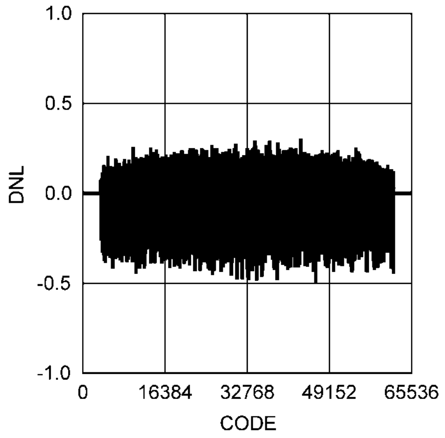


Transfer Characteristic (Offset Binary Format)

Typical Performance Characteristics, DNL, INL

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, $V_{AD1.8}$, V_{DR} = 1.8V, f_{CLK} = 130 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 10MHz with –1dBFS.

DNL



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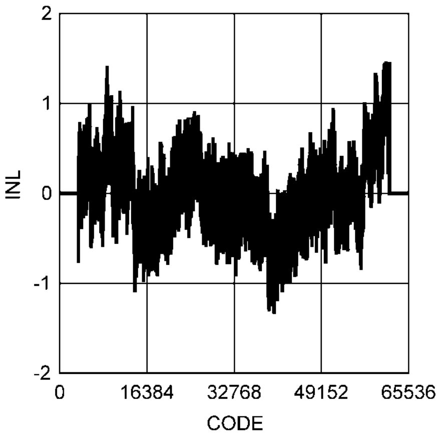
INL



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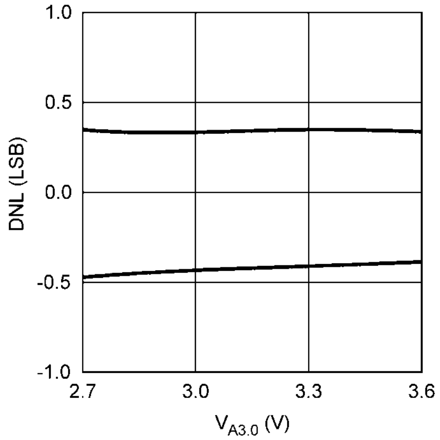
DNL vs.$V_{A3.0}$



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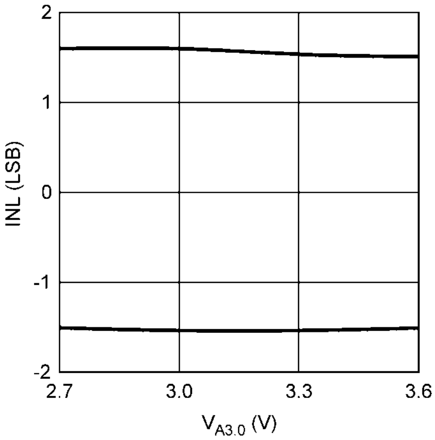
INL vs .$V_{A3.0}$



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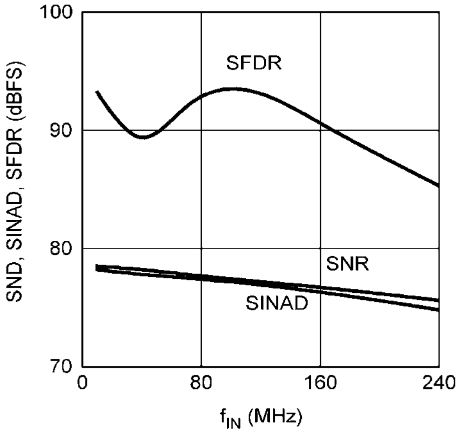
Typical Performance Characteristics, Dynamic Performance

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, $V_{AD1.8}$, V_{DR} = 1.8V, f_{CLK} = 130 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 160MHz with –1dBFS..



SNR, SINAD, SFDR vs. f_{IN}

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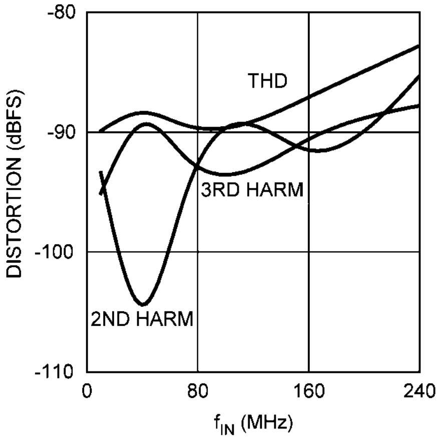

DISTORTION vs. f_{IN}

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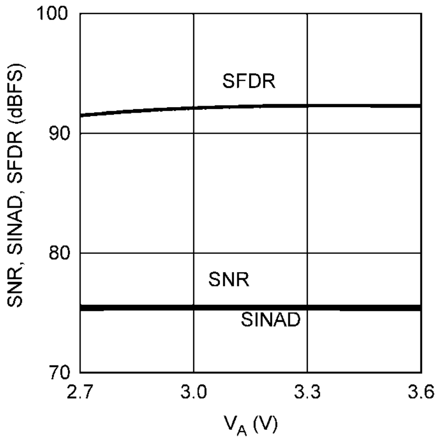

SNR, SINAD, SFDR vs. $V_{A3.0}$

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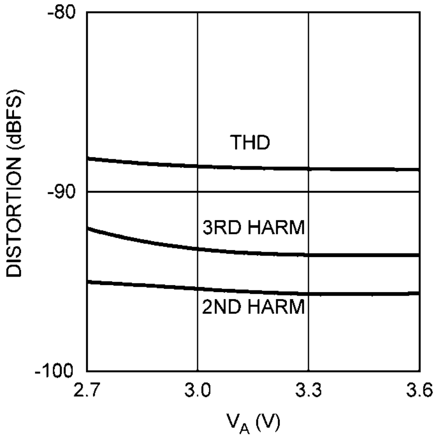

DISTORTION vs. $V_{A3.0}$

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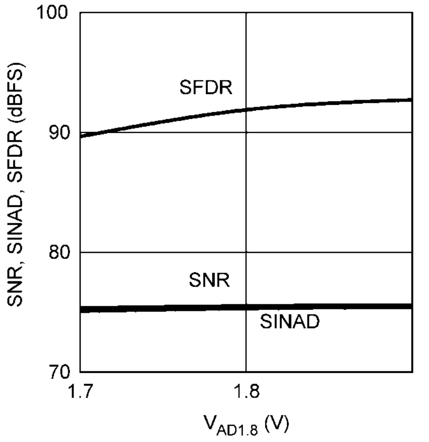

SNR, SINAD, SFDR vs. $V_{AD1.8}$

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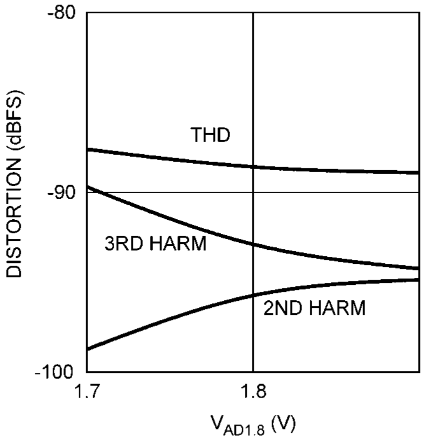

DISTORTION vs. $V_{AD1.8}$

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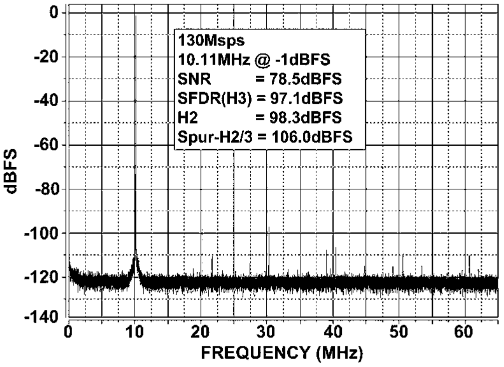
Spectral Response @ 10.11 MHz



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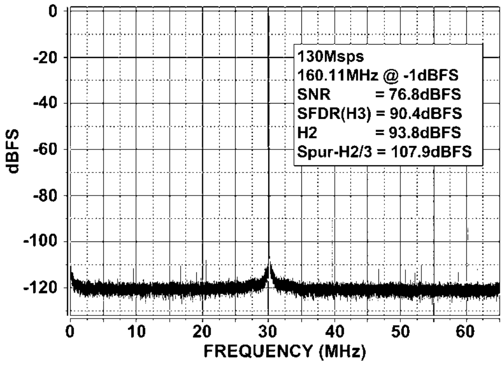
Spectral Response @ 160.11 MHz



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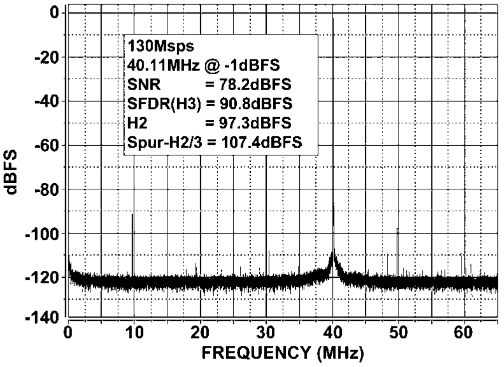
Spectral Response @ 40.11 MHz



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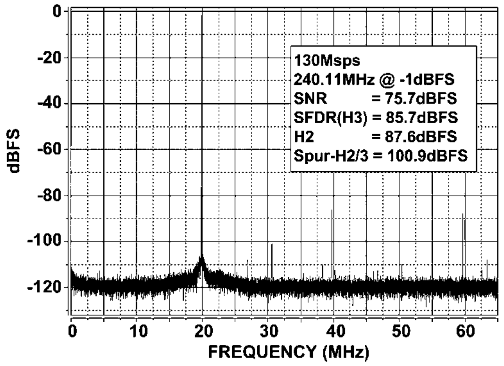
Spectral Response @ 240.11 MHz



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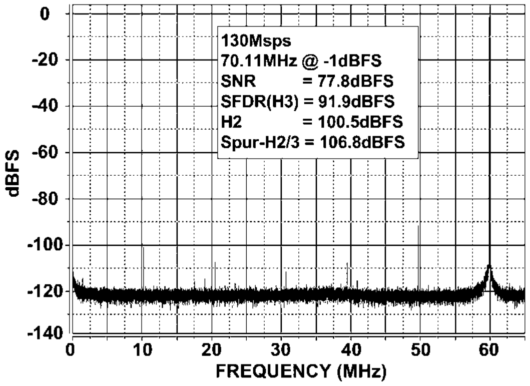
Spectral Response @ 70.11 MHz



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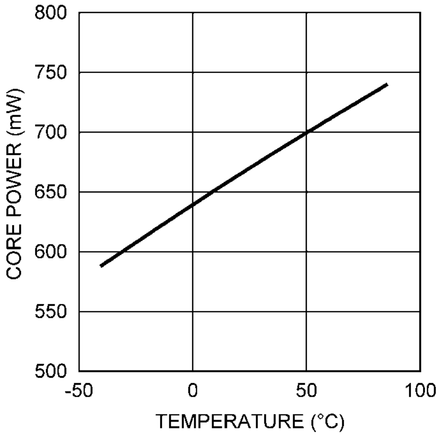
Core Power vs. Temperature (Excludes I_{DR})



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Functional Description

Operating on dual +1.8 and +3.0V supplies, the ADC16V130 digitizes a differential analog input signals to 16 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance. The user has the choice of using an internal 1.2V stable reference, or using an external 1.2V reference. Internal 1.2V reference has high output impedance of > 9 kΩ and can be easily over-driven by external reference. Two multi-level multi-function pins can program data format, clock mode, power down and sleep mode.

ADC Architecture

The ADC16V130 architecture consists of a highly linear and wide bandwidth sample-and-hold circuit, followed by a switched capacitor pipeline ADC. Each stage of the pipeline ADC consists of low resolution flash sub-ADC and an inter-stage multiplying digital-to-analog converter (MDAC), which is a switched capacitor amplifier with a fixed stage signal gain and DC level shifting circuits. The amount of DC level shifting is dependent on sub-ADC digital output code. 16bit final digital output is the result of the digital error correction logic, which receives digital output of each stage including redundant bits to correct offset error of each sub-ADC.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC16V130:

$2.7V \leq V_{A3.0} \leq 3.6V$

$1.7V \leq V_{A1.8} \leq 1.9V$

$1.7V \leq V_{AD1.8} \leq 1.9V$

$1.7V \leq V_{DR} \leq 1.9V$

$5\ MSPS \leq F_{CLK} \leq 130\ MSPS$

$V_{REF} \leq 1.2V$

$V_{CM} = 1.15V$ (from V_{RM})

2.0 ANALOG INPUTS

Analog input circuit of the ADC16V130 is a differential switched capacitor sample-and-hold circuit (see *Figure 1*) that provides optimum dynamic performance wide input frequency range with minimum power consumption. The clock signal alternates sample mode (Q_S) and hold mode (Q_H). An integrated low jitter duty cycle stabilizer ensures constant optimal sample and hold time over wide range of input clock duty cycle. The duty cycle stabilizer is always turned on during normal operation.

During sample mode, analog signals (V_{IN+}, V_{IN-}) are sampled across two sampling capacitor (C_S) while the amplifier in the sample-and-hold circuit is idle. The dynamic performance of the ADC16V130 is likely determined during sampling mode. The sampled analog inputs (V_{IN+}, V_{IN-}) are held during hold mode by connecting input side of the sampling capacitors to output of the amplifier in the sample-and-hold circuit while driving pipeline ADC core.

The signal source, which drives the ADC16V130, is recommended to have source impedance less than 100 Ω over wide frequency range for optimal dynamic performance.

A shunt capacitor can be placed across the inputs to provide high frequency dynamic charging current during sample mode and also absorb any switching charge coming from the ADC16V130. A shunt capacitor can be placed across each input to GND for similar purpose. Smaller physical size and low ESR and ESL shunt capacitor is recommended.

The value of shunt capacitor should be carefully chosen to optimize the dynamic performance at certain input frequency range. Larger value shunt capacitors can be used for low input frequency range, but the value has to be reduced at high input frequency range.

Balancing impedance at positive and negative input pin over entire signal path must be ensured for optimal dynamic performance.

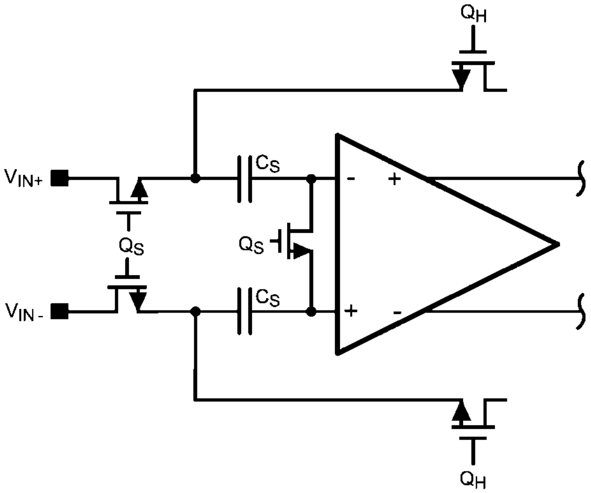

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FIGURE 1. Simplified Switched-Capacitor Sample-and-hold Circuit

2.1 Input Common Mode

The analog inputs of the ADC16V130 are not internally dc biased and the range of input common mode is very narrow. Hence it is highly recommended to use the common mode voltage (V_{RM}, typically 1.15V) as input common mode for optimal dynamic performance regardless of DC and AC coupling applications. Input common mode signal must be decoupled with low ESL 0.1µF at the far end of load point to minimize noise performance degradation due to any coupling or switching noise between the ADC16V130 and input driving circuit.

2.2 Driving Analog Inputs

For low frequency applications, either a flux or balun transformer can convert single-ended input signal into differential and drive the ADC16V130 without additive noise. An example is shown in *Figure 2*. V_{RM} pin is used to bias the input common mode by connecting the center tap of the transformer's secondary ports. Flux transformer is used for this example, but AC coupling capacitors should be added once balun type transformer is used.

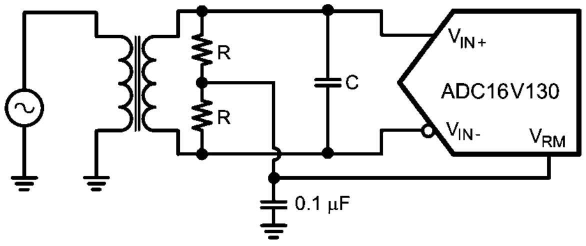

FIGURE 2. Transformer Drive Circuit for Low Input Frequency

Transformer has a characteristic of band pass filtering. It sets lower band limit by being saturated at frequencies below a few MHz and sets upper frequency limit due to its parasitic resistance and capacitance. The transformer core will be saturated with excessive signal power and it causes distortion as equivalent load termination becomes heavier at high input frequencies. This is a reason to reduce shunt capacitors for high IF sampling application to balance the amount of distortion caused by transformer and charge kick-back noise from the device.

As input frequency goes higher with the input network in *Figure 3*, amplitude and phase unbalance increase between positive and negative inputs (V_{IN+} and V_{IN-}) due to the inherent impedance mismatch between the two primary ports of the transformer while one is connected to the signal source and the other is connected to GND. Distortion increases as the result.

Cascaded transmission line transformers can be used for high frequency applications like high IF sampling base station receiver channel. Transmission line transformer has less stray capacitance between primary and secondary ports and so the amount of impedance at secondary ports is effectively less even with the given inherent impedance mismatch on the primary ports. Cascading two transmission line transformers further reduces the effective stray capacitance from the secondary of ports of the secondary transformer to primary ports of first transformer, where impedance is mismatched. A transmission line transformer, for instance MABACT0040 from M/A-COM, with center tap on secondary port could further reduce amplitude and phase mismatch.

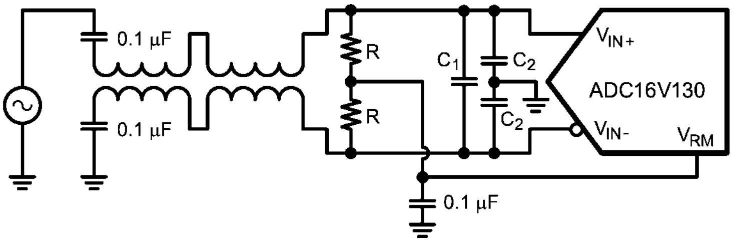

FIGURE 3. Transformer Drive Circuit for High Input Frequency

2.3 Equivalent Input Circuit and Its S11

Input circuit of the ADC16V130 during sample mode is a differential switched capacitor as shown in *Figure 4*. Bottom plate sampling switch is bootstrapped in order to reduce its turn on impedance and its variation across input signal amplitude. Bottom plate sampling switches and top plate sampling switch are all turned off during hold mode. The sampled analog input signal is processed throughout the following pipeline ADC core. Equivalent impedance changes drastically between sample and hold mode while significant amount of charge injection occurs during the transition between the two operating modes.

Distortion and SNR heavily rely on the signal integrity, impedance matching during sample mode and charge injection while switching sampling switches.

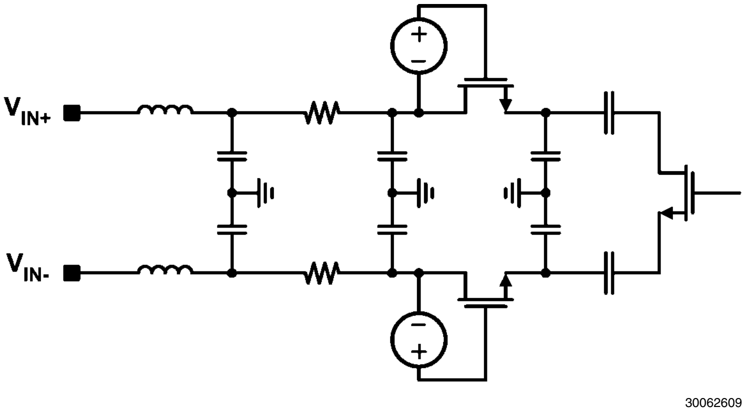

FIGURE 4. Input Equivalent Circuit

A measured S11 of the input circuit of the ADC16V130 is shown in *Figure 5* (Currently the figure is a simulated one. It is subject to be changed later. Note that the simulated S11 closely matches with the measured S11). Up to 500 MHz, it is predominantly capacitive loading with small stray resistance and inductance as shown in *Figure 5*. An appropriate resistive termination at a given input frequency band has to be added to improve signal integrity. Any shunt capacitor on analog input pin deteriorates signal integrity but it provides high frequency charge to absorb the charge inject generated while sampling switches are toggling. A optimal shunt capacitor is dependent on input signal frequency as well as impedance characteristic of analog input signal path including components like transformer, termination resistor, DC coupling capacitors.

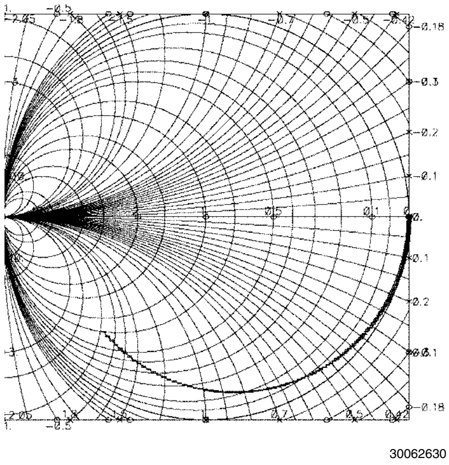

FIGURE 5. S11 Curve of Input Circuit

3.0 CLOCK INPUT CONSIDERATIONS

3.1 Clock Input Modes

The ADC16V130 provides a low additive jitter differential clock receiver for optimal dynamic performance at wide input frequency range. Input common mode of the clock receiver is internally biased at $V_{A1.8}/2$ through a 10 kΩ each to be driven by DC coupled clock input as shown in *Figure 6*. However while DC coupled clock input drives CLK+ and CLK-, it is recommend the common mode (average voltage of CLK+ and CLK-) not to be higher than $V_{A1.8}/2$ in order to prevent substantial tail current reduction, which might cause lowered jitter performance. Meanwhile, CLK+ and CLK- should not become lower than AGND. A high speed back-to-back diode connected between CLK+ and CLK- could limit the maximum swing, but this could cause signal integrity concerns when the diode turns on and reduce load impedance instantaneously.

A preferred differential clocking through a transformer coupled is shown in *Figure 7*. A 0.1µF decoupling capacitor on the center tap of the secondary ports of a flux type transformer stabilizes clock input common mode. Differential clocking increases the maximum amplitude of the clock input at the pins twice as large as that with singled-ended mode as shown in *Figure 8*. Clock amplitude is recommended to be as large as possible while CLK+ and CLK- both never exceed supply rails of $V_{A1.8}$ and AGND. With a given equivalent input noise of the differential clock receiver shown in *Figure 6*, larger clock amplitude at CLK+ and CLK- pins increases its slope around zero-crossing point so that higher signal-to-noise could be obtained by reducing the noise contributed by clock signal path.

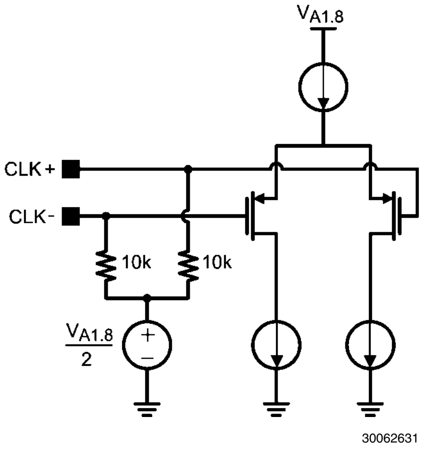

FIGURE 6. Equivalent Clock Receiver

The differential receiver of the ADC16V130 has excellent low noise floor but its bandwidth is wide as multiple times of clock rate. The wide band noise folds back to nyquist frequency band in frequency domain at ADC output. Increased slope of the input clock lowers the equivalent noise contributed by the differential receiver.

A band-pass filter (BPF) with narrow pass band and low insertion loss could be added on the clock input signal path when wide band noise of clock source is noticeably large compared to the input equivalent noise of the differential clock receiver.

Load termination could be a combination of R and C instead of a pure R. This RC termination could improve noise performance of clock signal path by filtering out high frequency noise through a low pass filter. The size of R and C is dependent on the clock rate and slope of the clock input.

A LVPECL and/or LVDS driver could also drive the ADC16V130. However the full dynamic performance of the ADC16V130 might not be achieved due to the high noise floor of the driving circuit itself especially in high IF sampling application.

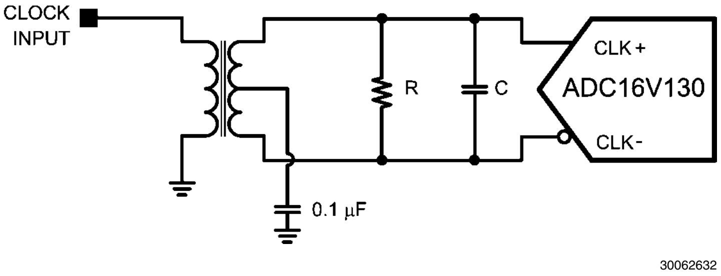

FIGURE 7. Differential Clocking, Transformer Coupled

Singled-ended clock can drive CLK+ pin through a 0.1µF AC coupling capacitor while CLK- is decoupled to AGND through a 0.1µF capacitor as shown in *Figure 8*.

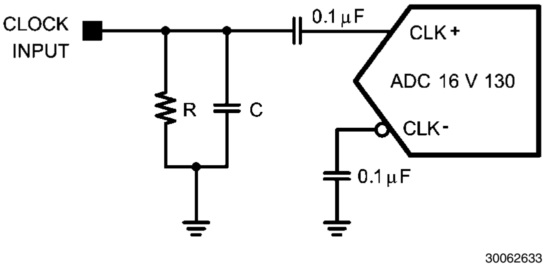

FIGURE 8. Singled-Ended 1.8V Clocking, Capacitive AC Coupled

3.2 Duty Cycle Stabilizer

Highest operating speed with optimal performance could be only achieved with 50% of clock duty cycle because the switched-capacitor circuit of the ADC16V130 is designed to have equal amount of settling time between each stage. The maximum operating frequency could be reduced accordingly while clock duty cycle departs from 50%.

The ADC16V130 contains a duty cycle stabilizer that adjusts non-sampling (rising) clock edge to make the duty cycle of the internal clock over 30 to 70% of input clock duty cycle. The duty cycle stabilizer is always on because the noise and distortion performance are not affected at all. It is not recommended to use the ADC16V130 at the clock frequencies less than 5 MSPS, at which the feedback loop in the duty cycle stabilizer becomes unstable.

3.3 Clock Jitter vs. Dynamic Performance

High speed and high resolution ADCs require low noise clock input to ensure its full dynamic performance over wide input frequency range. SNR (SNR_{Fin}) at a given input frequency (Fin) can be calculated by:

$$SNR_{Fin} = 10\log_{10}\left[\frac{A^2/2}{V_N^2 + (2\pi Fin \times Tj)^2/2}\right]$$

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with a given total noise power (V_N^2) of an ADC, total rms jitter (Tj), and input amplitude (A) in dBFS.

Clock signal path must be treated as an analog signal whenever aperture jitter affects the dynamic performance of the ADC16V130. Power supplies for the clock drivers has to be separated from the ADC output drive supplies to prevent modulated clock signal with the ADC digital output signals. Higher noise floor and/or increased distortion/spur might result from any coupling noise from ADC digital output signals to analog input and clock signals.

In IF sampling applications, the signal-to-noise ratio is particularly affected by clock jitter as shown in *Figure 9*. *Tj* is the integrated noise power of the clock signal divided by the slope of clock signal around tripping point. Upper limit of the noise integration is independent of applications and set by the bandwidth of the clock signal path. However lower limit of the noise integration highly relies on the applications. In base station receiver channel applications, the lower limit is determined by channel bandwidth and space from an adjacent channel.

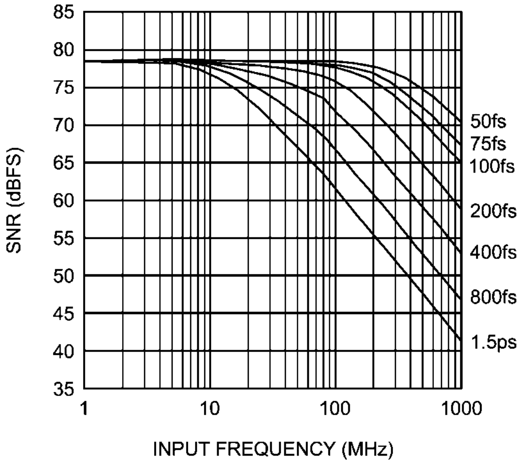

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FIGURE 9. SNR with given Jitter vs. Input Frequency

4.0 CALIBRATION

Automatic calibration engine contained within the ADC16V130 improves dynamic performance and reduces its part-to-part variation. Digital output signals including output clock (OUTCLK+/-) are all logic low while calibrating. The ADC16V130 is automatically calibrated when the device is powered up. Optimal dynamic performance might not be obtained if power-up time is longer than internal delay time (~32mS @ 130 MSPS clock rate). In this case, the ADC16V130 could be re-calibrated by asserting and then de-asserting power down mode. Re-calibration is recommended whenever operating clock rate changes.

5.0 VOLTAGE REFERENCE

A stable and low noise voltage reference and its buffer amplifier are built into the ADC16V130. The input full scale is two times of V_{REF}, which is same as VBG (On-chip bandgap output having 9 kΩ output impedance) as well as V_{RP} - V_{RN} as shown in *Figure 10*. The input range can be adjusted by changing V_{REF} either internally or externally. An external reference with low output impedance can easily over-drive V_{REF} pin. Default V_{REF} is 1.2V. Input common mode voltage (V_{RM}) is a fixed voltage level of 1.15V. Maximum SNR can be achieved at maximum input range of 1.2V V_{REF}. Although the ADC16V130 dynamic and static performance is optimized at V_{REF} of 1.2V, reducing V_{REF} can improve SFDR performance with sacrificing SNR of the ADC16V130.

5.1 Reference Decoupling

It is highly recommended to place external decoupling capacitors connected to V_{RP}, V_{RN}, V_{RM} and V_{REF} pins as close to pins as possible. The external decoupling capacitor should have minimal ESL and ESR. During normal operation, inappropriate external decoupling with large ESL and/or ESR capacitors increase settling time of ADC core and results in lower SFDR and SNR performance. V_{RM} pin may be loaded up to 1mA for setting input common mode. The remaining pins should not be loaded. Smaller capacitor values might result in degraded noise performance. Decoupling capacitor on V_{REF} pin must not exceed 0.1µF, heavier decoupling on this pin will cause improper calibration during power-up. All reference pins except V_{REF} have very low output impedance. Driving these pins via low output impedance external circuit for long time period might damage the device.

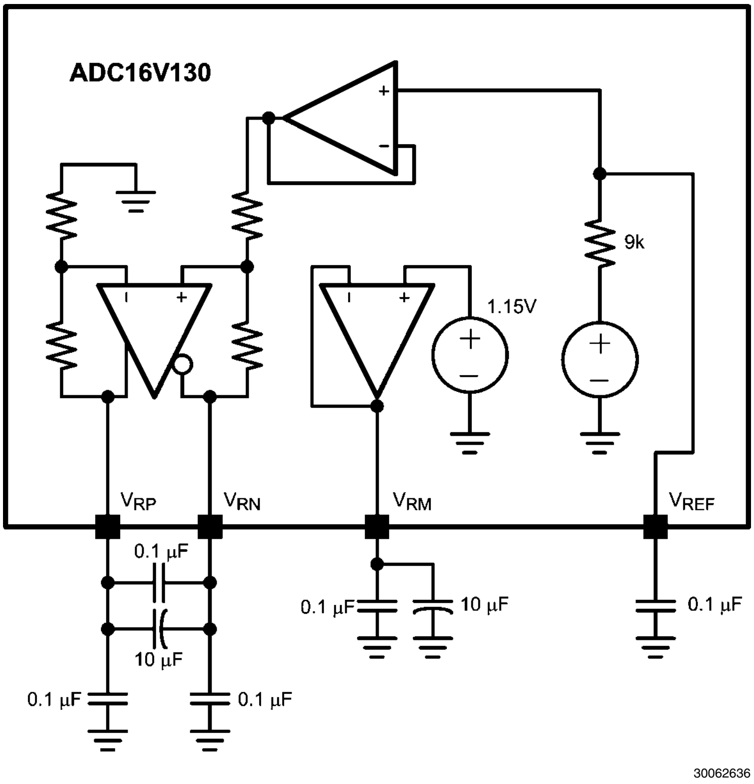


FIGURE 10. Internal References and their Decoupling

While V_{RM} pin is used to set input common mode level via transformer, a smaller serial resistor could be placed on the signal path to isolate any switching noise interfering between ADC core and input signal. The serial resistor introduces voltage error between V_{RM} and V_{CM} due to charge injection while sampling switches toggling. The serial resistance should not be larger than 50 Ω.

All grounds associated with each reference and analog input pins should be connected to a solid and quite ground on PC board. Coupling noise from digital outputs and their supplies to the reference pins and their ground can cause degraded SNR and SFDR performance.

6.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC16V130 between these areas, is required to achieve specified performance.

Even though LVDS output reduces ground bounding during its transition, the positive and negative signal path has to be well matched and their trace should be kept as short as possible. It is recommend to place LVDS repeater between the ADC16V130 and digital data receiver block to isolate coupling noise from receiving block while the length of the traces are long or the noise level of the receiving block is high.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than its total ground plane area.

Generally, analog and digital lines should not be crossing each. However whenever it is inevitable, make sure that these lines are crossing each other at 90° to minimize cross talk. Digital output and output clock signals must be separated from analog input, references and clock signals unconditionally to ensure the maximum performance from ADC16V130. Any coupling might result degraded SNR and SFDR performance especially at high IF applications.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should not be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling. It is recommended to place the transformers of input signal path on the top plate, but the transformer of clock signal path on the bottom plate. Every critical analog signal path like analog inputs and clock inputs must be treated as a transmission line and should have a solid ground return path with a small loop.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference pins and ground should be connected to a very clean point in the ground plane. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC16V130 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

Ground return current path can be well managed when supply current path is precisely controlled and ground layer is continuous and placed next to the supply layer. This is because of the proximity effect. Ground return current path with a large loop will cause electro-magnetic coupling and results in poor noise performance. Not that even if there is a large plane for a current path, high frequency current path is not spread evenly over the large plane, but only takes a path with lowest impedance. Instead of large plane, using thick trace for supplies makes it easy to control return current path. It is recommended to place supply next to GND layer with thin dielectric for smaller ground return loop. Proper location and size of decoupling capacitors provide short and clean return current path.

7.0 SUPPLIES AND THEIR SEQUENCE

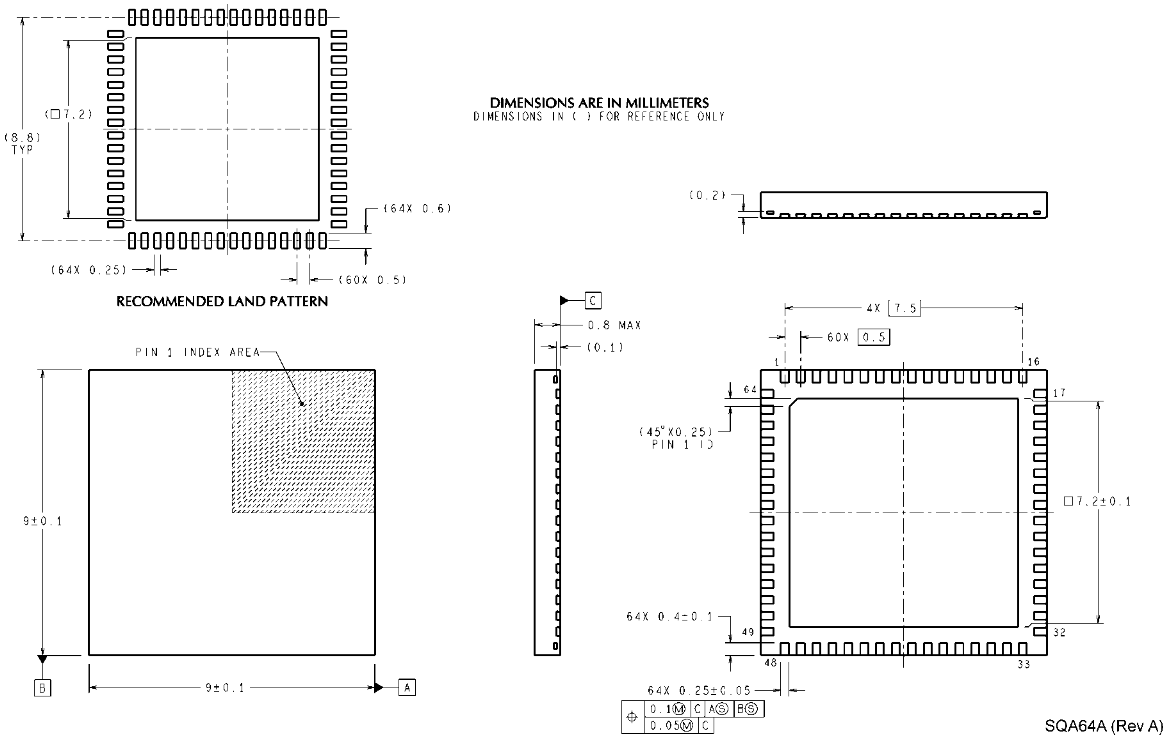
There are four supplies for the ADC16V130; one 3.0V supply $V_{A3.0}$ and three 1.8V supplies $V_{A1.8}$, $V_{AD1.8}$ and V_{DR}. It is recommended to separate V_{DR} from $V_{A1.8}$ supplies, any coupling from V_{DR} to rest of supplies and analog signals could cause lower SFDR and noise performance. When $V_{A1.8}$ and V_{DR} are both from same supply source, coupling noise can be mitigated by adding ferrite-bead on V_{DR} supply path.

The user can use different decoupling capacitors to provide current over wide frequency range. The decoupling capacitors should be located close to the point of entry and close to the supply pins with minimal trace length. A single ground plane is recommended because separating ground under the ADC16V130 could cause unexpected long return current path.

$V_{A3.0}$ supply must turn on before $V_{A1.8}$ and/or V_{DR} reaches single diode turn-on voltage level. If this supply sequence is reversed, excessive amount of current will flow through $V_{A3.0}$ supply. Ramp rate of $V_{A3.0}$ supply must be kept less than 60V/mS (i.e., 60µS for 3.0V supply) in order to prevent excessive surge current through ESD protection devices.

The exposed pad (Pin #0) on the bottom of the package should be soldered to AGND in order to get optimal noise performance. The exposed pad is a solid ground for the device and also is heat sinking path.

Physical Dimensions inches (millimeters) unless otherwise noted


DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
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TYP
(64X 0.6)
(64X 0.25)
(60X 0.5)
RECOMMENDED LAND PATTERN
(0.2)
C
0.8 MAX
(0.1)
4X 7.5
60X 0.5
1
16
17
64
(45°X0.25)
PIN 1 ID
□7.2±0.1
64X 0.4±0.1
49
32
48
33
64X 0.25±0.05
0.1Ⓜ C AⓈ BⓈ
0.05Ⓜ C
PIN 1 INDEX AREA
9±0.1
B
9±0.1
A
SQA64A (Rev A)

64-Lead LLP Package
Ordering Number ADC16V130CISQ
NS Package Number SQA64A

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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