National Semiconductor

December 2006

# LMV951
# 1V, 2.7 MHz, Rail-to-Rail Input and Output Amplifier with Shutdown Option

## General Description

The LMV951 amplifier is capable of operating at supply voltages from 0.9V to 3V with guaranteed specs at 1V and 1.8V single supply.

The input common mode range extends to both power supply rails without the offset glitch and input bias current phase reversal inherent to most rail to rail input amplifiers.

Contrary to a conventional rail to rail output amplifier the LMV951 has a buffered output stage providing an open loop gain which is relatively unaffected by resistive output loading. At 1V supply voltage, the LMV951 is able to source and sink in excess of 35 mA and offers a gain bandwidth product of 2.7 MHz.

In shutdown mode the LMV951 consumes less than 50 nA of supply current.

## Features

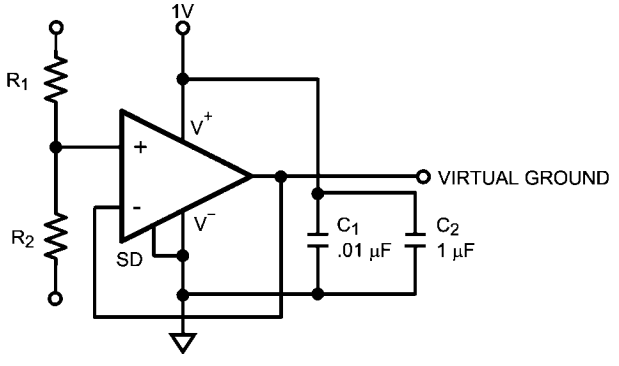
(Typical 1.0V supply, unless otherwise noted)

- Guaranteed 1V single supply operation
- Wide bandwidth
- No $V_{OS}$ glitch over the input CMVR
- No input $I_{BIAS}$ current reversal over $V_{CM}$ range
- Buffered output stage
- High output drive capability
- Output short circuit
  - — Sink current 35 mA
  - — Source current 45 mA
- Rail-to-rail buffered output
  - — @ 600Ω load 32 mV from either rail
  - — @ 2 kΩ load 12 mV from either rail
- Temperature range –40°C to 125°C

## Applications

- Battery operated systems
- Battery monitoring
- Supply current monitoring

**Virtual Ground Circuit**

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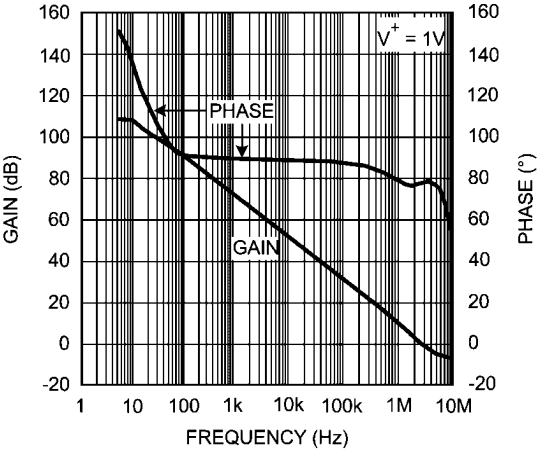
**Open Loop Gain and Phase**

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance (Note 2) | |
| Human Body Model | 2000V |
| Machine Model | 200V |
| Supply Voltage ($V^+ - V^-$) | 3.1V |
| $V_{IN}$ Differential | ±0.3V |
| Voltage at Input/Output Pin | $V^+$ +0.3V, $V^-$ −0.3V |
| Current at Input Pin | ±10 mA |
| Junction Temperature (Note 3) | +150°C |
| Mounting Temperature | |
| Infrared or Convection (20 sec) | 235°C |

## Operating Ratings (Note 1)

| | |
|---|---|
| Temperature Range (Note 3) | −40°C to +125°C |
| Supply Voltage | 0.9V to 3V |
| Thermal Resistance ($\theta_{JA}$) (Note 3) | 170°C/W |

## 1V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits guaranteed for at $T_A$ = 25°C, $V^+$ = 1, $V^-$ = 0V, $V_{CM}$ = 0.5V, Shutdown = 0V, and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | 1.5 | 2.8<br>**3.0** | mV |
| TC $V_{OS}$ | Input Offset Average Drift | | | 0.15 | | µV/°C |
| $I_B$ | Input Bias Current | | | 32 | 80<br>**85** | nA |
| $I_{OS}$ | Input Offset Current | | | 0.2 | | nA |
| CMRR | Common Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 1V | 67<br>**55** | 77 | | dB |
| | | 0.1V ≤ $V_{CM}$ ≤ 1V | 76<br>**73** | 85 | | |
| PSRR | Power Supply Rejection Ratio | 1V ≤ $V^+$ ≤ 1.8V, $V_{CM}$ = 0.5V | 70<br>**67** | 92 | | dB |
| | | 1V ≤ $V^+$ ≤ 3V, $V_{CM}$ = 0.5V | 68<br>**65** | 85 | | |
| $V_{CM}$ | Input Common-Mode Voltage Range | CMRR ≥ 67 dB | 0 | | 1.2 | V |
| | | **CMRR ≥ 55 dB** | **0** | | **1.2** | |
| $A_V$ | Large Signal Voltage Gain | $V_{OUT}$ = 0.1V to 0.9V<br>$R_L$ = 600Ω to 0.5V | 90<br>**85** | 106 | | dB |
| | | $V_{OUT}$ = 0.1V to 0.9V<br>$R_L$ = 2 kΩ to 0.5V | 90<br>**86** | 112 | | |
| $V_{OUT}$ | Output Voltage Swing High | $R_L$ = 600Ω to 0.5V | 50<br>**62** | 25 | | mV from rail |
| | | $R_L$ = 2 kΩ to 0.5V | 25<br>**36** | 12 | | |
| | Output Voltage Swing Low | $R_L$ = 600Ω to 0.5V | 70<br>**85** | 32 | | |
| | | $R_L$ = 2 kΩ to 0.5V | 35<br>**40** | 10 | | |
| $I_{OUT}$ | Output Short Circuit Current (Note 7) | Sourcing<br>$V_O$ = 0V, $V_{IN(DIFF)}$ = ±0.2V | 20<br>**15** | 45 | | mA |
| | | Sinking<br>$V_O$ = 1V, $V_{IN(DIFF)}$ = ±0.2V | 20<br>**13** | 35 | | |
| $I_S$ | Supply Current | Active Mode $V_{SD}$ <0.4V | | 370 | 480<br>**520** | µA |
| | | Shutdown Mode $V_{SD}$ >0.6V | | 0.01 | 1.0<br>**3.0** | |
| SR | Slew Rate | (Note 8) | | 1.4 | | V/µs |

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| GBWP | Gain Bandwidth Product | | | 2.7 | | MHz |
| $e_n$ | Input - Referred Voltage Noise | f = 1 kHz | | 25 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input-Referred Current Noise | f = 1 kHz | | 0.2 | | $pA/\sqrt{Hz}$ |
| THD | Total Harmonic Distortion | f = 1 kHz, $A_V$ = 1, $R_L$ = 1 kΩ | | 0.02 | | % |
| $I_{SD}$ | Shutdown Pin Current | Active Mode, $V_{SD}$ = 0V | | .001 | 1 | µA |
| | | Shutdown Mode, $V_{SD}$ = 1V | | .001 | 1 | |
| $V_{SD}$ | Shutdown Pin Voltage Range | Active Mode | 0 | | 0.4 | V |
| | | Shutdown Mode | 0.65 | | 1 | |

## 1.8V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits guaranteed for at $T_A$ = 25°C, $V^+$ = 1.8V, $V^-$ = 0V, $V_{CM}$ = 0.9V, Shutdown = 0V, and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | 1.5 | 2.8<br>**3.0** | mV |
| TC $V_{OS}$ | Input Offset Average Drift | | | 0.15 | | µV/°C |
| $I_B$ | Input Bias Current | | | 36 | 80<br>**85** | nA |
| $I_{OS}$ | Input Offset Current | | | 0.2 | | nA |
| CMRR | Common Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 1.8V | 82<br>**80** | 93 | | dB |
| PSRR | Power Supply Rejection Ratio | 1V ≤ $V^+$ ≤ 1.8V, $V_{CM}$ = 0.5V | 70<br>**67** | 92 | | dB |
| | | 1V ≤ $V^+$ ≤ 3V, $V_{CM}$ = 0.5V | 68<br>**65** | 85 | | |
| $V_{CM}$ | Input Common-Mode Voltage Range | CMRR ≥ 82 dB | −0.2 | | 2 | V |
| | | **CMRR ≥ 80 dB** | **−0.2** | | **2** | |
| $A_V$ | Large Signal Voltage Gain | $V_{OUT}$ = 0.2 to 1.6V<br>$R_L$ = 600Ω to 0.9V | 86<br>**83** | 110 | | dB |
| | | $V_{OUT}$ = 0.2 to 1.6V<br>$R_L$ = 2 kΩ to 0.9V | 86<br>**83** | 116 | | |
| $V_{OUT}$ | Output Voltage Swing High | $R_L$ = 600Ω to 0.9V | 50<br>**60** | 33 | | mV from rail |
| | | $R_L$ = 2 kΩ to 0.9V | 25<br>**34** | 13 | | |
| | Output Voltage Swing Low | $R_L$ = 600Ω to 0.9V | 80<br>**105** | 54 | | |
| | | $R_L$ = 2 kΩ to 0.9V | 35<br>**44** | 17 | | |
| $I_{OUT}$ | Output Short Circuit Current (Note 7) | Sourcing<br>$V_O$ = 0V, $V_{IN(DIFF)}$ = ±0.2V | 50<br>**35** | 85 | | mA |
| | | Sinking<br>$V_O$ = 1.8V, $V_{IN(DIFF)}$ = ±0.2V | 45<br>**25** | 80 | | |
| $I_S$ | Supply Current | Active Mode $V_{SD}$ <0.5V | | 570 | 780<br>**880** | µA |
| | | Shutdown Mode $V_{SD}$ >1.3V | | 0.3 | 2.2<br>**10** | |
| SR | Slew Rate | (Note 8) | | 1.4 | | V/µs |
| GBWP | Gain Bandwidth Product | | | 2.8 | | MHz |

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 6) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $e_n$ | Input - Referred Voltage Noise | f = 1 kHz | | 25 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input-Referred Current Noise | f = 1 kHz | | 0.2 | | $pA/\sqrt{Hz}$ |
| THD | Total Harmonic Distortion | f = 1 kHz, $A_V$ = 1, $R_L$ = 1 kΩ | | 0.02 | | % |
| $I_{SD}$ | Shutdown Pin Current | Active Mode, $V_{SD}$ = 0V | | .001 | 1 | µA |
| | | Shutdown Mode, $V_{SD}$ = 1.8V | | .001 | 1 | |
| $V_{SD}$ | Shutdown Pin Voltage Range | Active Mode | 0 | | 0.5 | V |
| | | Shutdown Mode | 1.45 | | 1.8 | |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

**Note 3:** The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

**Note 4:** Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions is very limited self-heating of the device.

**Note 5:** All limits are guaranteed by testing or statistical analysis.

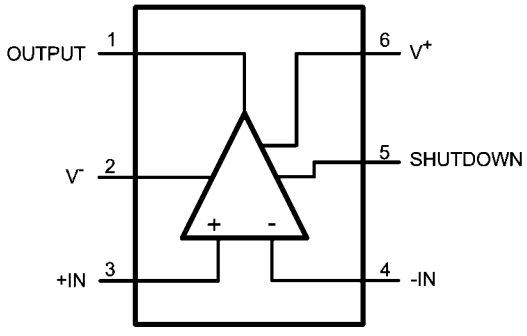
**Note 6:** Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

**Note 7:** The short circuit test is a momentary test, the short circuit duration is 1.5 ms

**Note 8:** Number specified is the average of the positive and negative slew rates.

## Connection Diagram

**6-Pin SOT23**

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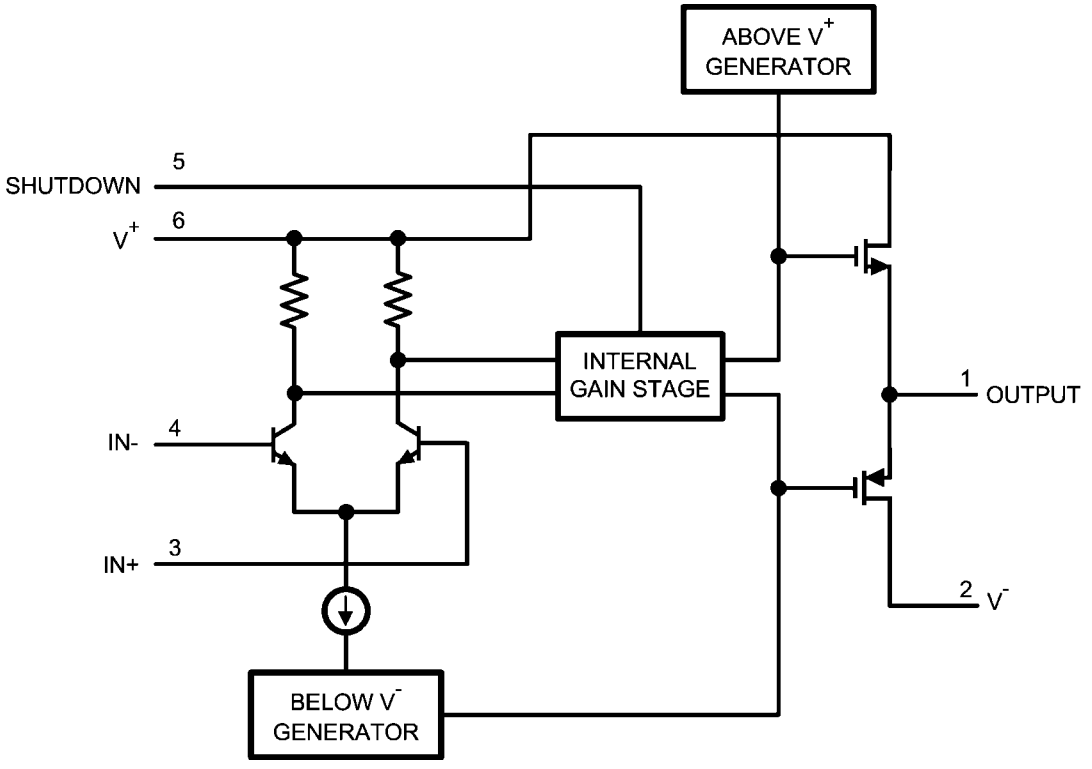
**Top View**

## Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 6-Pin SOT23 | LMV951MK | AS3A | 1k Units Tape and Reel | MK06A |
| | LMV951MKX | | 3k Units Tape and Reel | |

## Simplified Schematic

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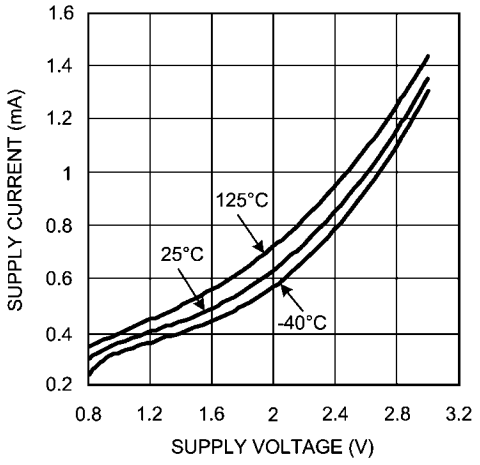
## Typical Performance Characteristics

Unless otherwise specified, all limits are guaranteed for $T_A$ = 25°C, $V^+$ = 1V, $V^-$ = 0V, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes.

**Supply Current vs. Supply Voltage**

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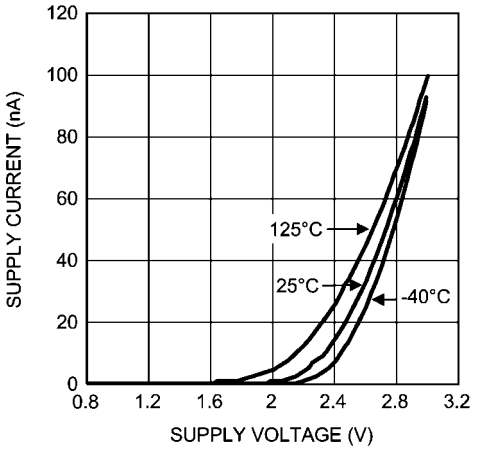
**Supply Current vs. Supply Voltage in Shutdown Mode**

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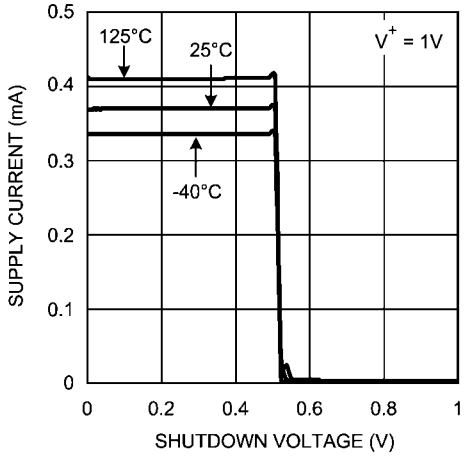
**Supply Current vs. Shutdown Voltage**

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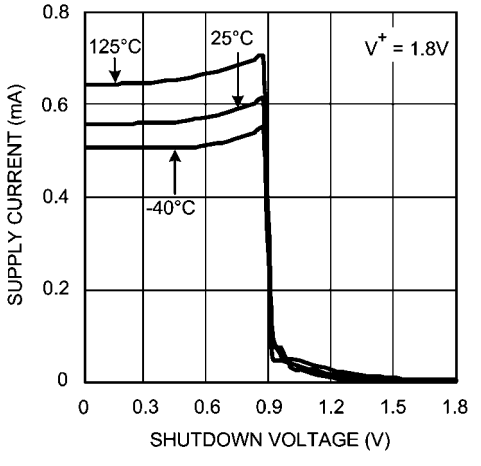
**Supply Current vs. Shutdown Voltage**

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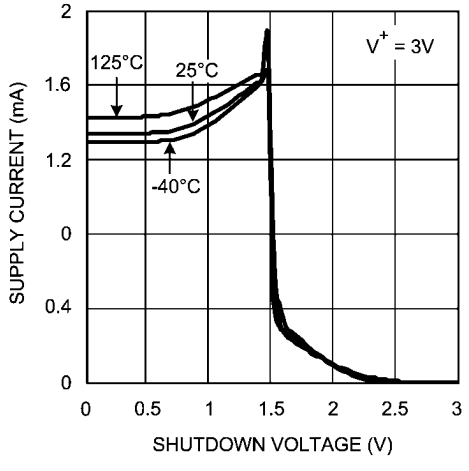
**Supply Current vs. Shutdown Voltage**

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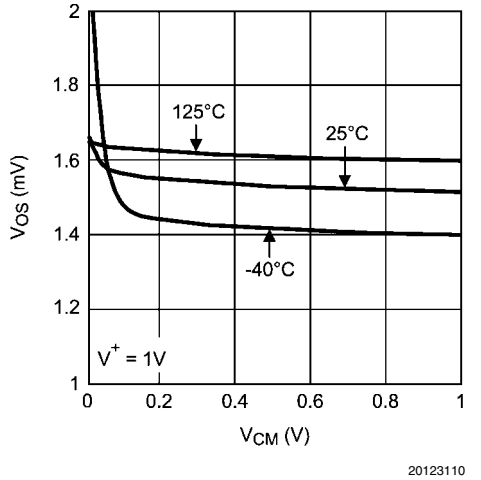
**$V_{OS}$ vs. $V_{CM}$**

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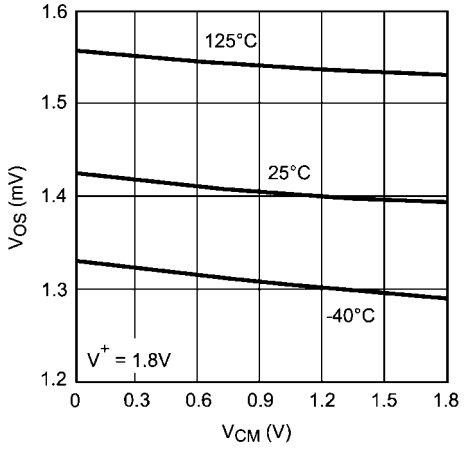
**$V_{OS}$ vs. $V_{CM}$**

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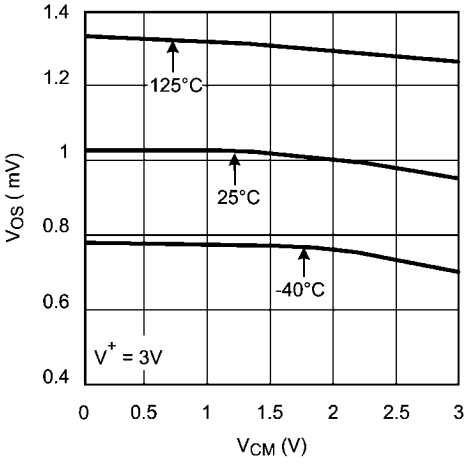
**$V_{OS}$ vs. $V_{CM}$**

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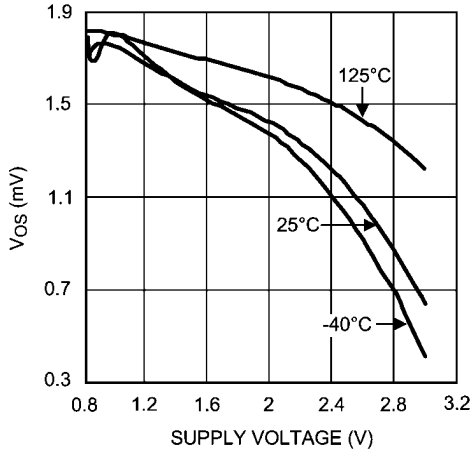
**$V_{OS}$ vs. Supply Voltage**

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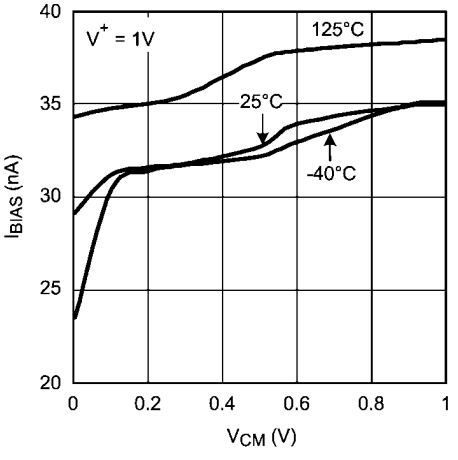
**$I_{BIAS}$ vs. $V_{CM}$**

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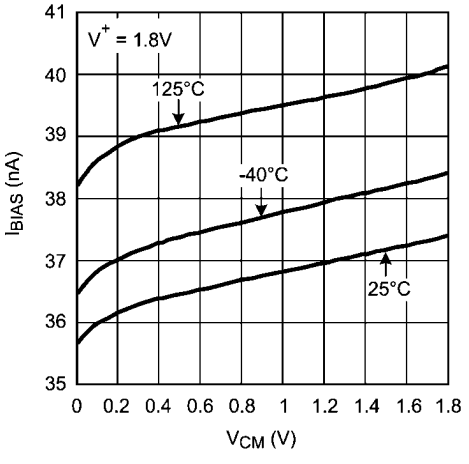
**$I_{BIAS}$ vs. $V_{CM}$**

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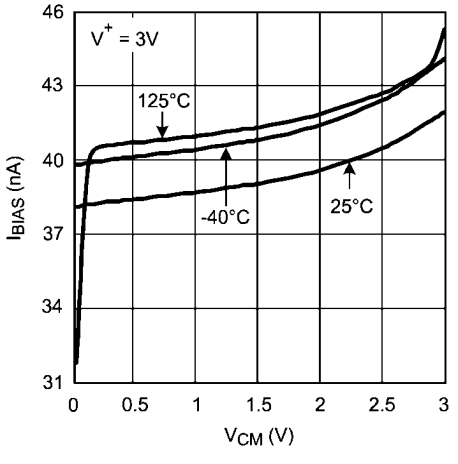
**$I_{BIAS}$ vs. $V_{CM}$**

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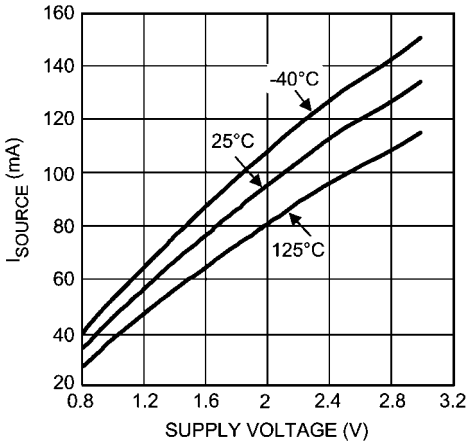
**Sourcing Current vs. Supply Voltage**

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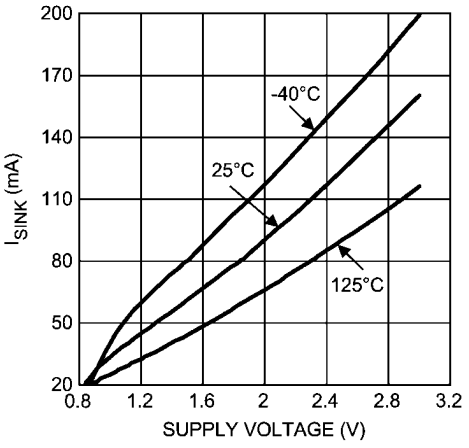
**Sinking Current vs Supply Voltage**

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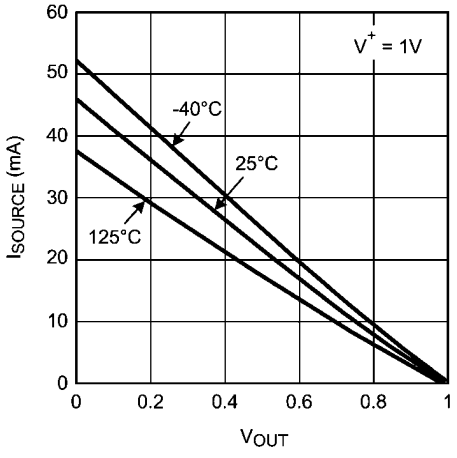
**Sourcing Current vs. Output Voltage**

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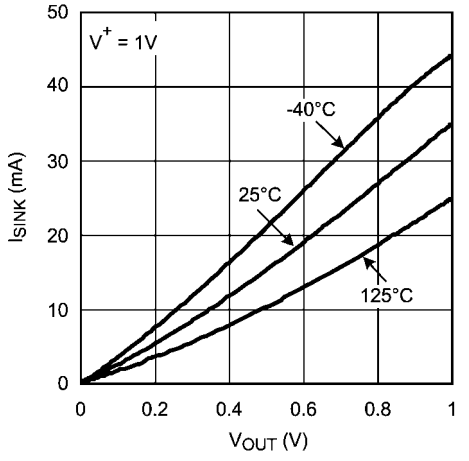
**Sinking Current vs. Output Voltage**

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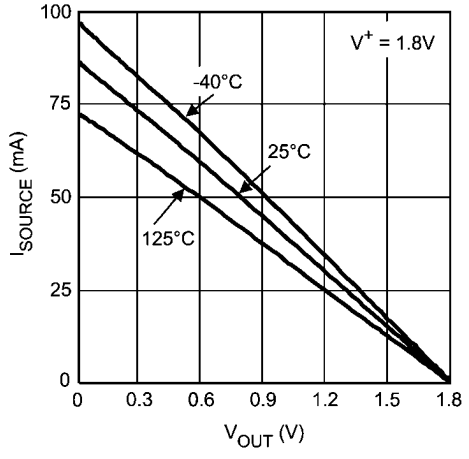
**Sourcing Current vs. Output Voltage**

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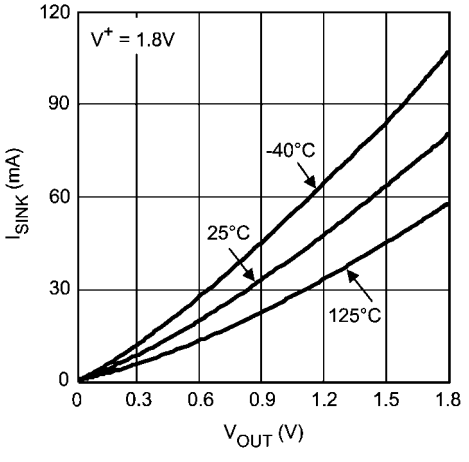
**Sinking Current vs. Output Voltage**

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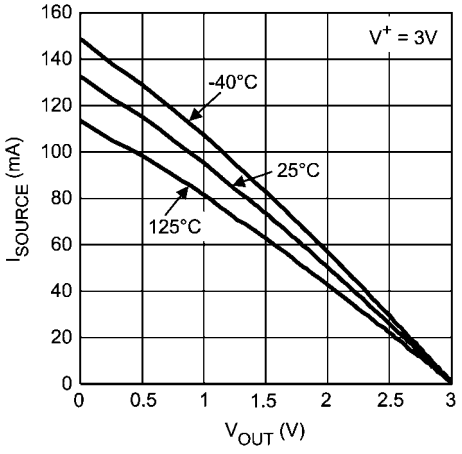
**Sourcing Current vs. Output Voltage**

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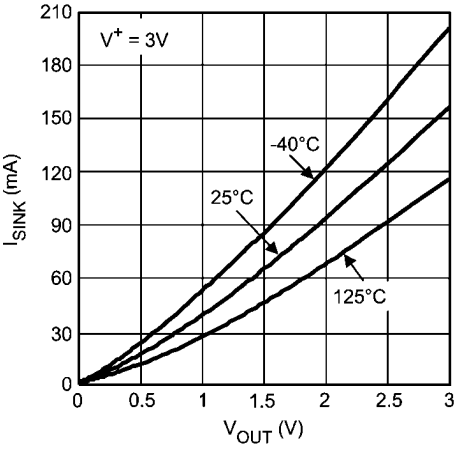
**Sinking Current vs. Output Voltage**

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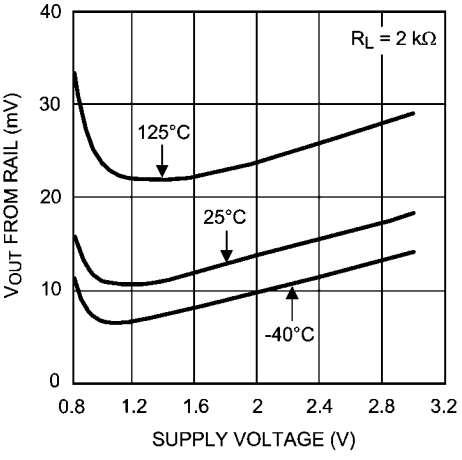
**Positive Output Swing vs. Supply Voltage**

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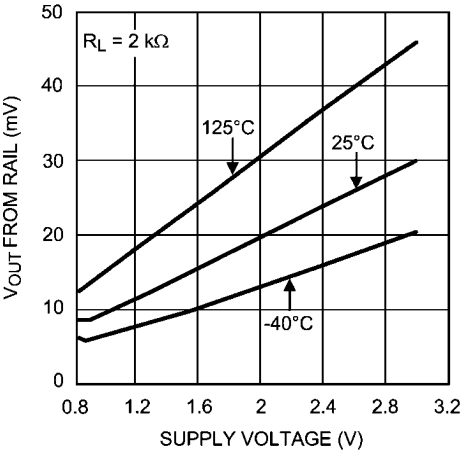
**Negative Output Swing vs. Supply Voltage**

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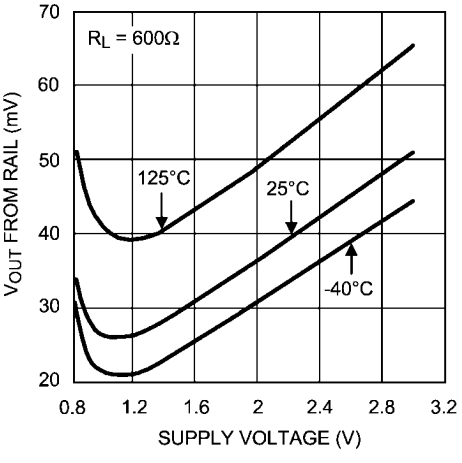
**Positive Output Swing vs. Supply Voltage**

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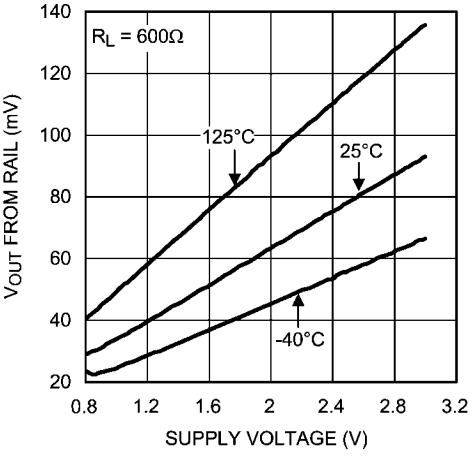
**Negative Output Swing vs. Supply Voltage**

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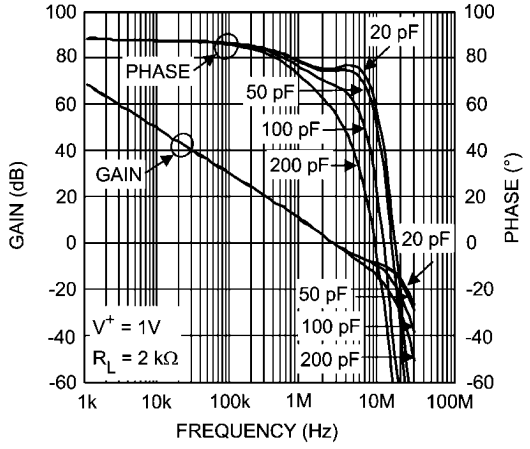
**Open Loop Gain and Phase with Capacitive Load**

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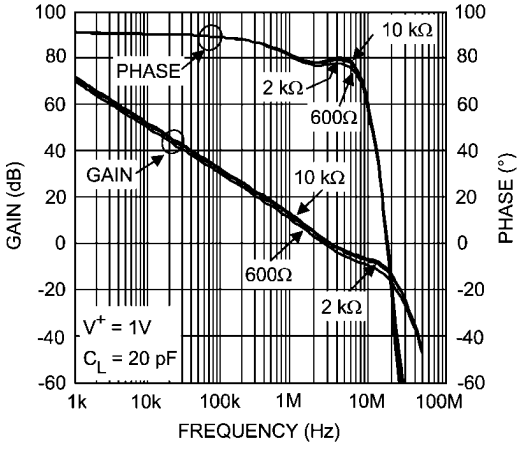
**Open Loop Gain and Phase with Resistive Load**

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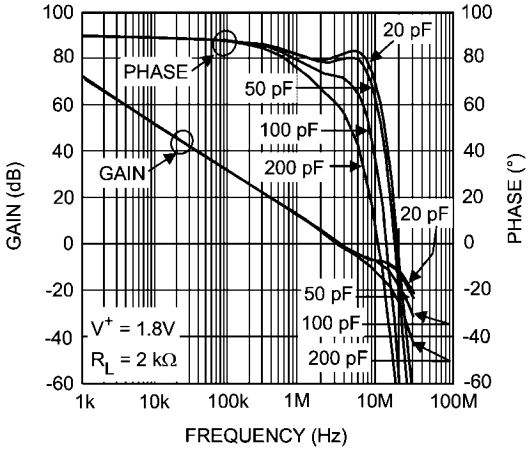
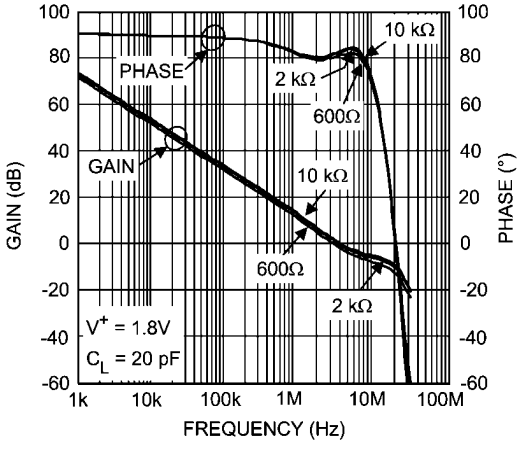
**Open Loop Gain and Phase with Capacitive Load**



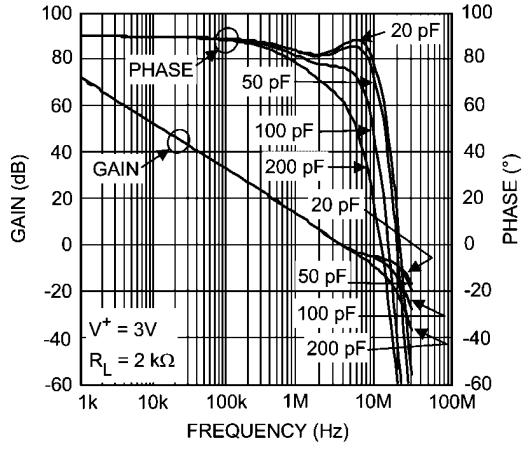

20123128

**Open Loop Gain and Phase with Resistive Load**



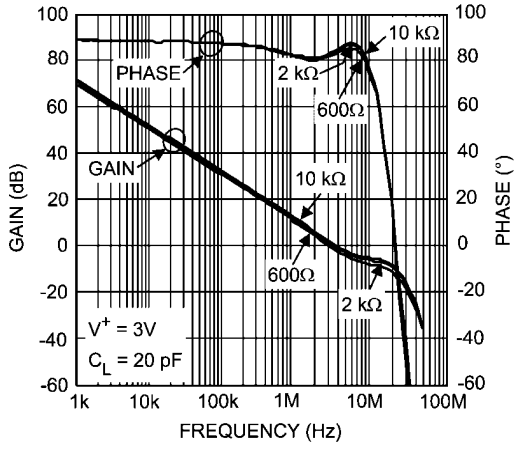

20123129

**Open Loop Gain and Phase with Capacitive Load**



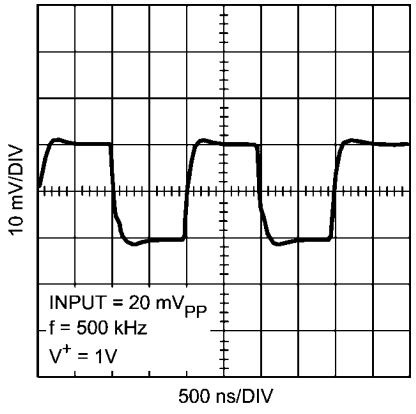

20123130

**Open Loop Gain and Phase with Resistive Load**



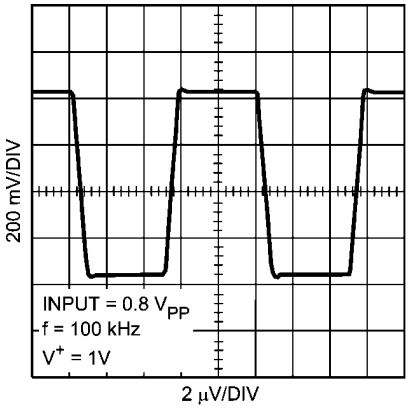

20123131

**Small Signal Transient Response, $A_V$ = +1**



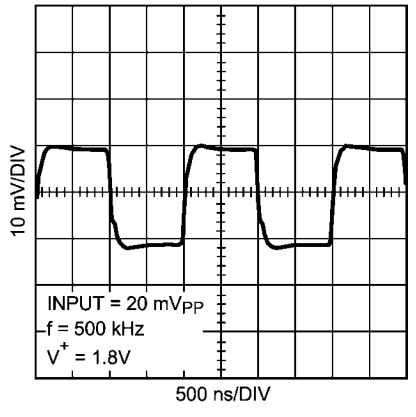

20123132

**Large Signal Transient Response, $A_V$ = +1**



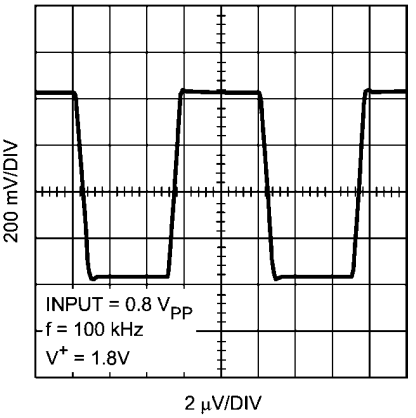

20123133

**Small Signal Transient Response, $A_V$ = +1**



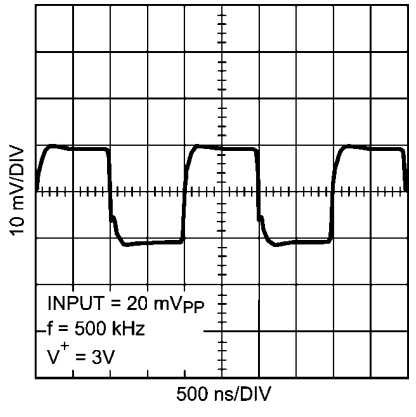

20123134

**Large Signal Transient Response, $A_V$ = +1**



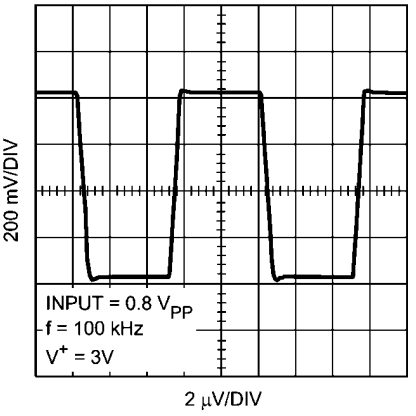

20123135

**Small Signal Transient Response, $A_V$ = +1**



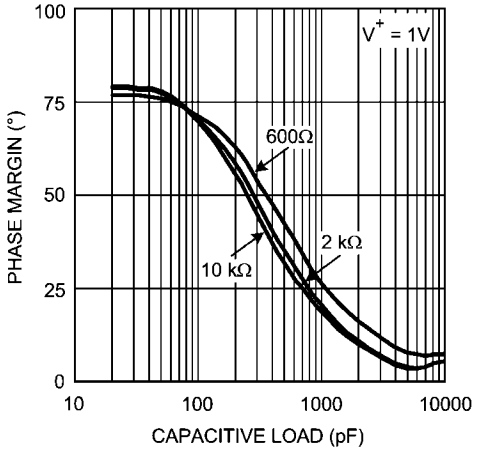

20123136

**Large Signal Transient Response, $A_V$ = +1**



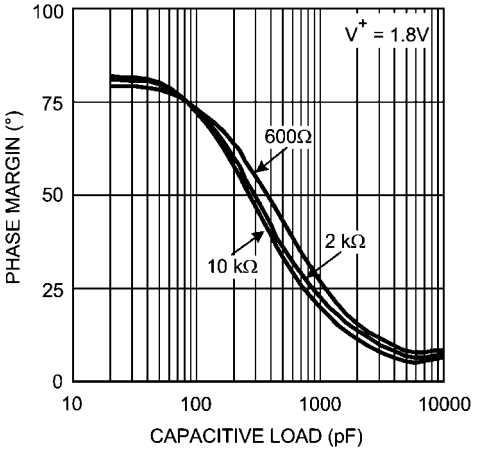

20123137

**Phase Margin vs. Capacitive Load (stability)**



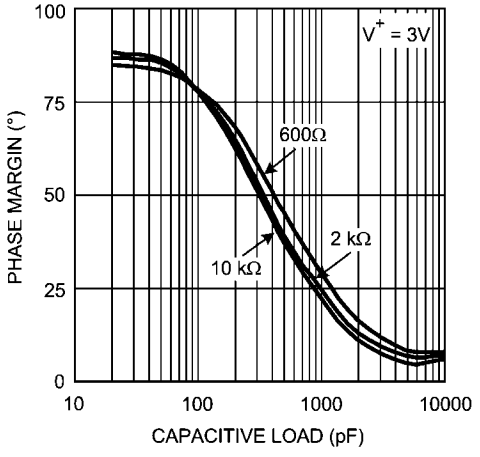

20123138

**Phase Margin vs. Capacitive Load (stability)**



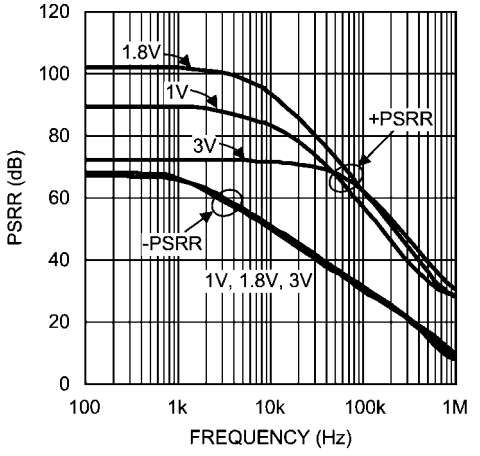

20123139

**Phase Margin vs. Capacitive Load (stability)**



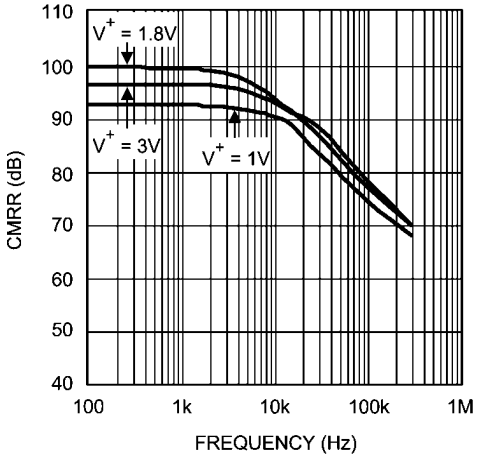

20123140

**PSRR vs. Frequency**



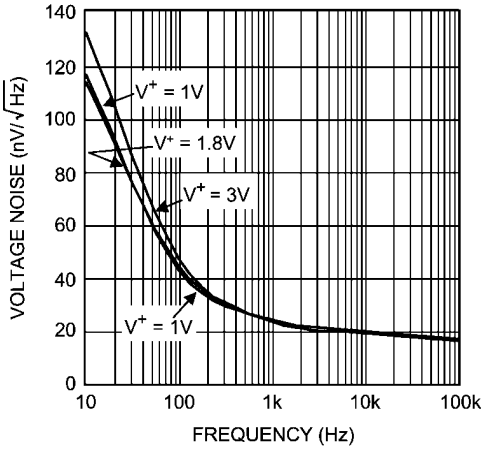

20123141

**CMRR vs. Frequency**



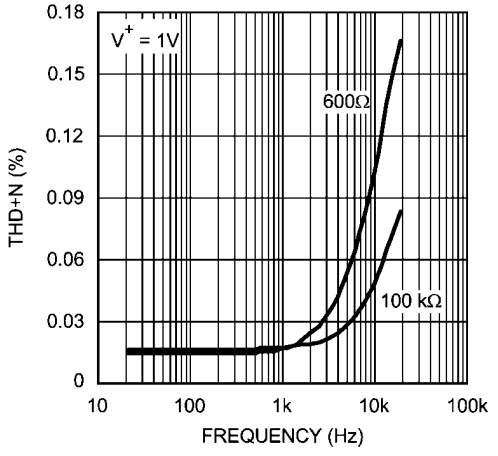

20123142

**Input Referenced Voltage Noise vs. Frequency**



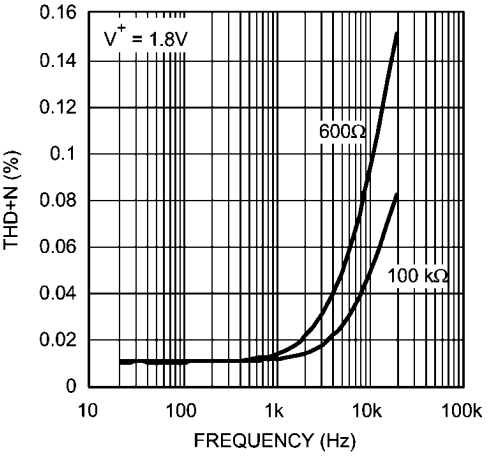

20123143

**THD+N vs. Frequency**



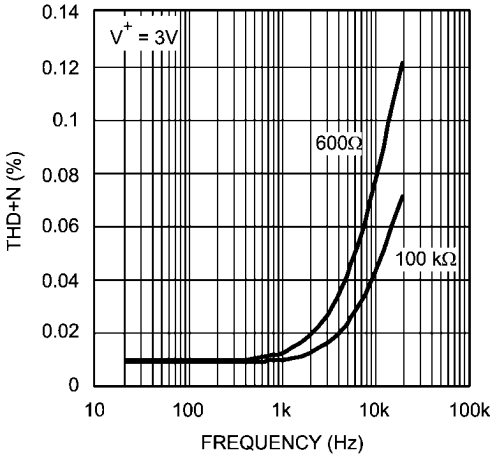

20123147

**THD+N vs. Frequency**



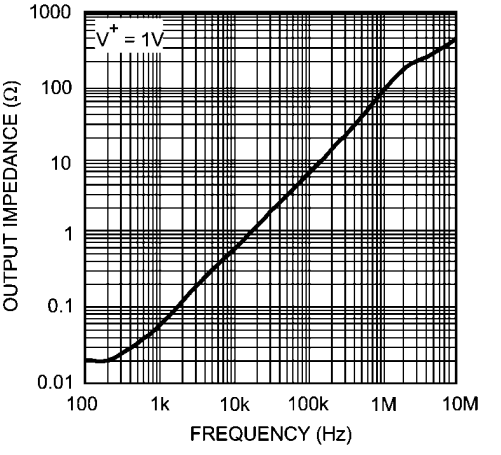

20123148

**THD+N vs. Frequency**




20123149

**Closed Loop Output Impedance vs. Frequency**




20123155

# Application Information

### CIRCUIT DESCRIPTION AND ADVANTAGE OF THE LMV951

The LMV951 utilizes an internal voltage generator which allows for rail to rail input and output operation from 1 to 3V supplies. An internal switching frequency between 10 MHz and 15 MHz is used for generating the internal voltages.

The bipolar input stage provides rail to rail input operation with no input bias current phase reversal and a constant input offset voltage over the entire input common mode range.

The CMOS output stage provides a gain that is virtually independent of resistive loads and an output drive current in excess of 35 mA at 1V. A further benefit of the output stage is that the LMV951 is stable in positive unity gain at capacitive loads in excess of 1000 pF.

#### Battery Operated Systems

The maximum operating voltage is 3V and the operating characteristics are guaranteed down to 1V which makes the LMV951 an excellent choice for battery operated systems using one or two NiCd or NiMH cells. The LMV951 is also functional at 0.9V making it an appropriate choice for a single cell alkaline battery.

#### Shutdown Capability

While in shutdown mode, the LMV951 typically consumes less than 50 nA of supply current making it ideal for power conscious applications. Full functionality is restored within 3 µs of enable.

#### Small Size

The small footprint of the LMV951 package is ideal for high density board systems. By using the small 6-Pin SOT23 package, the amplifier can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

#### Power Supply Bypassing

As in any high performance IC, proper power supply bypassing is necessary for optimizing the performance of the LMV951. The internal voltage generator needs proper bypassing for optimum operation. A surface mount ceramic .01 µF capacitor must be located as close as possible to the $V^+$ and $V^-$ pins (pins 2 and 6). This capacitor needs to have low ESR and a self resonant frequency above 15 MHz. A small tantalum or electrolytic capacitor with a value between 1 µF and 10 µF also needs to be located close to the LMV951.

### DRIVING CAPACITIVE LOAD

The unity gain follower is the most sensitive op amp configuration to capacitive loading; the LMV951 can drive up to 10,000 pF in this configuration without oscillation. If the application requires a phase margin greater than those shown in the datasheet graphs, a snubber network is recommended. The snubber offers the advantage of reducing the output signal ringing while maintaining the output swing which ensures a wider dynamic range; this is especially important at lower supply voltages.

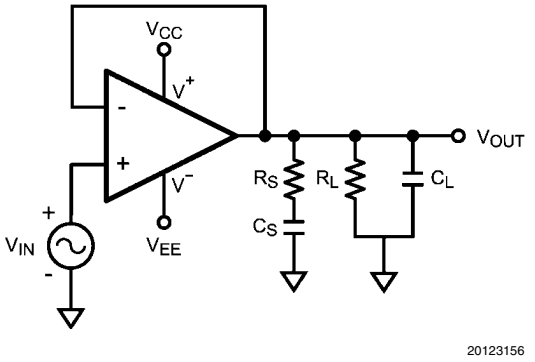



**FIGURE 1. Snubber Network to Improve Phase Margin**

The chart below gives recommended values for some common values of large capacitors. For these values $R_L$ = 2 kΩ;

| $C_L$ | $R_S$ | $C_S$ |
|---|---|---|
| 500 pF | 330Ω | 6800 pF |
| 680 pF | 270Ω | 8200 pF |
| 1000 pF | 220Ω | .015 µF |

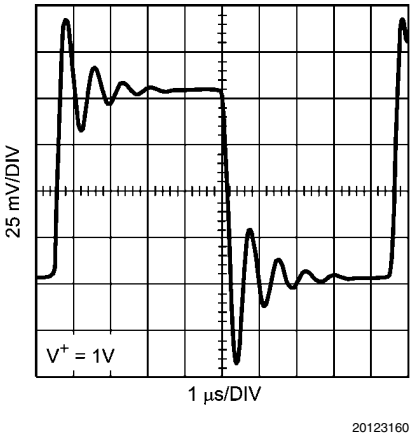



**FIGURE 2. 1000 pF and no Snubber**

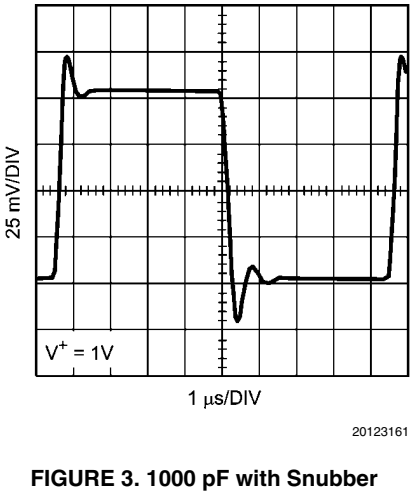



**FIGURE 3. 1000 pF with Snubber**

## BRIDGE CONFIGURATION AMPLIFIER

Some applications may benefit from doubling the voltage across the load. With $V^+$ = 1V a bridge configuration can provide a 2 $V_{PP}$ output to the load with a resistance as low as 300Ω. The output stage of the LMV951 enables it to drive a load of 120Ω and still swing at least 70% of the supply rails.

The bridge configuration shown in *Figure 4* enables the amplifier to maintain a low dropout voltage thus maximizing its dynamic range. It has been configured in a gain of 1 and uses the fewest number of parts.

Resistor values have been selected to keep the current consumption to a minimum and voltage errors due to bias currents negligible. Using the selected resistor values makes this circuit quite practical in a battery operated design. $R_1$, $R_2$ and $R_5$, $R_6$ set up a virtual ground that is half of $V^+$. Note that the accuracy of the resistor values will establish how well the two virtual grounds match. Any errors in the virtual grounds will show as current across $R_L$ when there is no input signal.

AC coupling the input signal sets the DC bias point of this signal to the virtual ground of the circuit. Using the large resistor values with a 1 µF capacitor ($C_1$) sets the frequency rolloff of this circuit below 10 Hz.

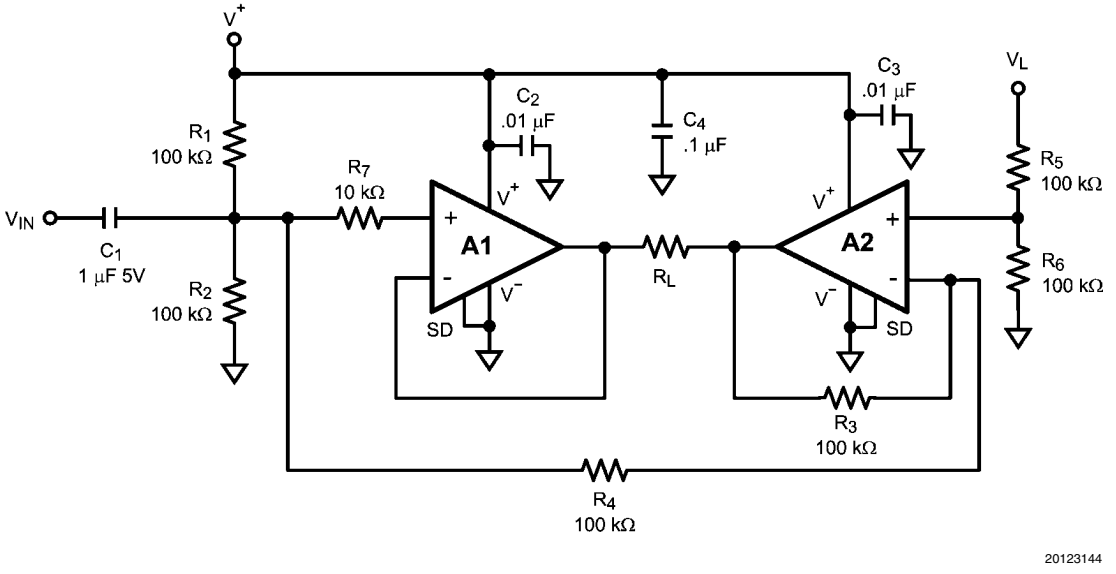



**FIGURE 4. Bridge Amplifier**

- $C_2$ and $C_3$ are .01 µF ceramic capacitors that must be located as close as possible to pin 6, the $V^+$ pin. As covered in the power supply bypassing section these capacitors must have low ESR and a self resonant frequency above 15 MHz.
- $C_4$ is a 1 µF tantalum or electrolytic capacitor that should also be located close to the supply pin.
- To use the shutdown feature tie pin 5 of the two parts together and connect through a 470 kΩ resistor to $V^+$. Add a switch between pin 5 and ground. Closing the switch keeps the parts in the active mode, opening the switch sets the parts in the shutdown mode without adding any additional current to $V^+$.

## VIRTUAL GROUND CIRCUIT

The front page of this data sheet shows the LMV951 being used in a system establishing a virtual ground. Having a buffered output stage gives this part the ability to handle load currents higher than 35 mA at 1V.

$R_3$ and $R_4$ are used to set the voltage of the virtual ground. To maintain low noise the values should be between 1 kΩ and 10 kΩ. $C_1$ and $C_2$ provide the recommended bypassing for the LMV951. These caps must be placed as close as possible to pins 2 and 6.

## TWO WIRE LINE TRANSMISSION

The robust output stage of the LMV951 makes it an excellent choice for driving long cables. The circuit shown below in *Figure 5* can drive a long cable using only two wires; power and ground.

When many sensors are located remotely from the control area the wiring becomes a significant expense. Using only two wires helps minimize the wiring expense in a large project such as an industrial plant. *Figure 6* shows a 25 kHz signal after passing though 1000 ft. of twisted pair cable. *Figure 7* shows a 200 kHz signal after passing through 50 ft. of twisted pair cable.

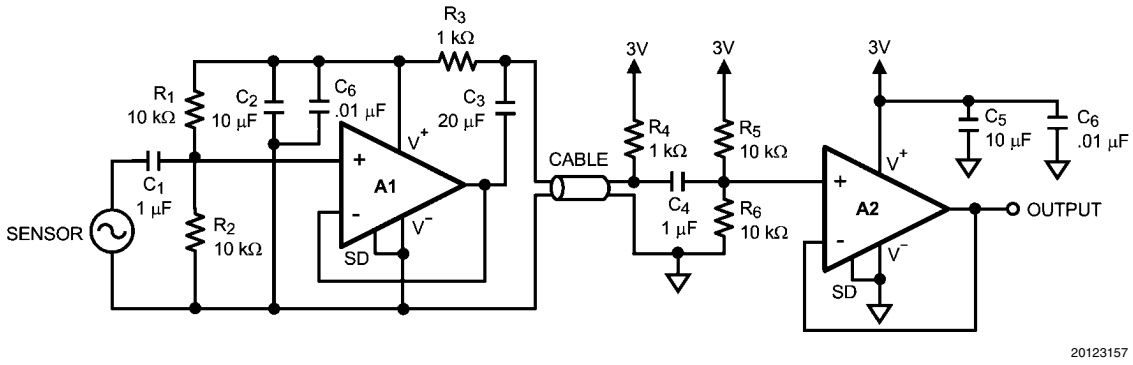



**FIGURE 5. Two Wire Line Driver**

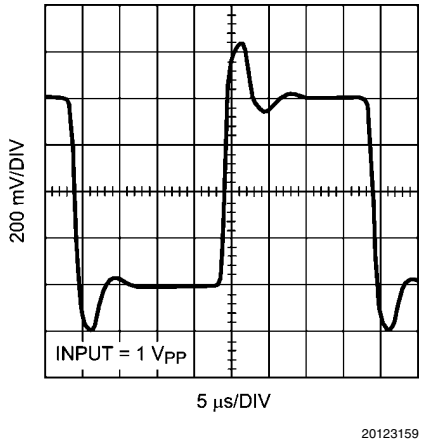



**FIGURE 6. 25 kHz Through 1000 ft.**

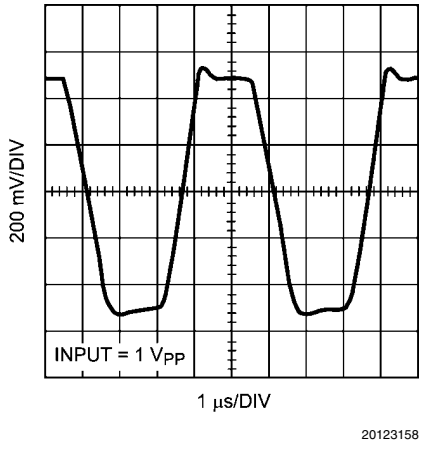
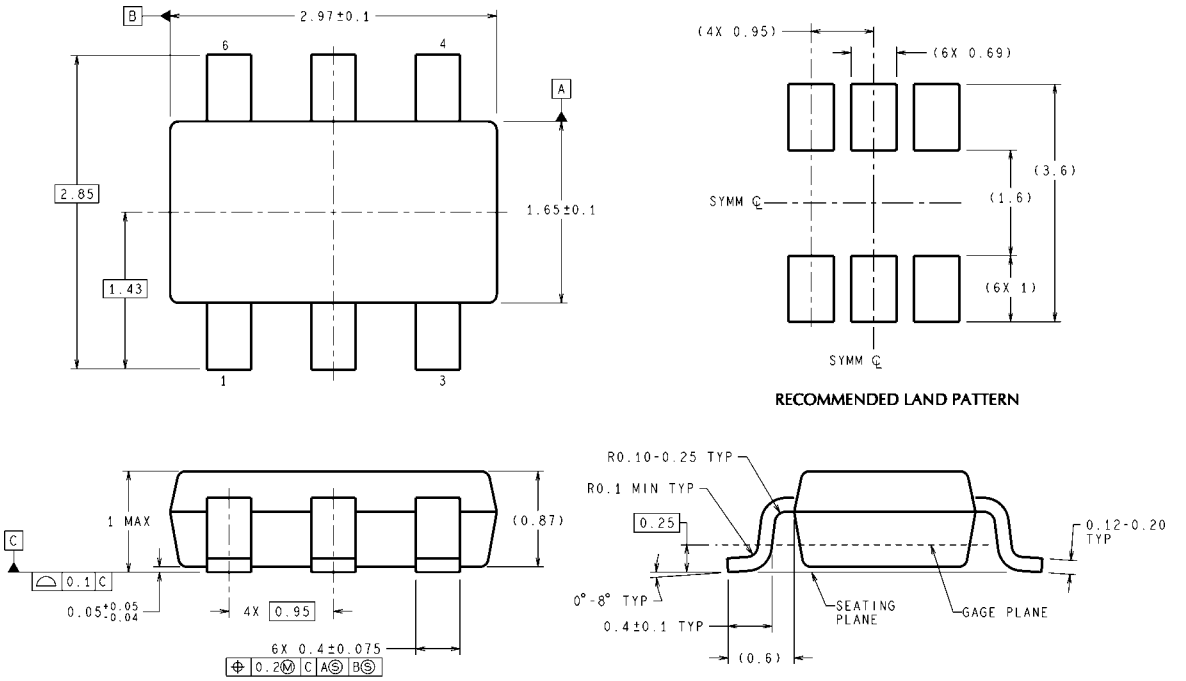



**FIGURE 7. 200 kHz Through 50 ft.**

The power supply of 3V is recommended to power this system. A1 and A2 are set up as unity gain buffers. It is easy to configure A1 with the required gain if a gain of greater than one is required. $C_1$ along with $R_1$ and $R_2$ are used to ensure the correct DC operating point at the input of A1. $C_4$ along with $R_5$ and $R_6$ are used to setup the correct DC operating point for A2. $C_1$, $C_3$, and $C_4$ have been selected to give about a 20% droop with a 1 kHz square wave input.

## Physical Dimensions inches (millimeters) unless otherwise noted




**6-Pin SOT23**
**NS Package Number MK06A**

# Notes



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