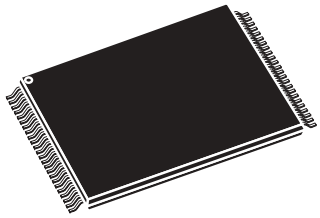
NAND16GW3B4D

16-Gbit (4 x 4 Gbits), two Chip Enable, 2112-byte page, 3 V supply, single level, multiplane, NAND flash memory

Preliminary Data

Features

- High-density NAND flash memory
  - 16 Gbits of memory array
  - 512 Mbits of spare area
  - Cost-effective solutions for mass storage applications
- NAND interface
  - x8 bus width
  - Multiplexed address/data
- Supply voltage: V_{DD} = 2.7 to 3.6 V
- Page size: (2048 + 64 spare) bytes
- Block size: (128 K + 4 K spare) bytes
- Multiplane architecture
  - Array split into two independent planes
  - All operations can be performed on both planes simultaneously
- Memory cell array:
  - (2 K + 64) bytes x 64 pages x 16384 blocks (4 dice x 4 Gbits, 2 Chip Enable)
- page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25 ns (min)
  - Page program operation time: 200 µs (typ)
- Multipage program time (2 pages): 200 µs (typ)
- Copy-back program with automatic error detection code (EDC)
- Fast block erase
  - Block erase time: 1.5 ms (typ)



TSOP48 12 x 20 mm (N)

- Multiblock erase time (2 blocks): 1.5 ms (typ)
- Status register
- Electronic signature
- Serial number option
- Chip enable ‘don’t care’
- Data protection
  - Hardware program/erase locked during power transitions
- Development tools
  - Error correction code models
  - Bad block management and wear leveling algorithm
  - HW simulation models
- Data integrity
  - 100,000 program/erase cycles (with ECC)
  - 10 years data retention
- ECOPACK® packages available

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1 Description

The NAND16GW3B4D is part of the single level cell (SLC) NAND flash 2112-byte/ 1056-word page family of non-volatile flash memories. The device has a density of 16 Gbits and combines four 4-Gbit dice in a stacked device. The 4 dice are coupled for access as two 8-Gbit devices, each with its own Chip Enable and Ready/Busy pin. This means each 8-Gbit can be driven independently using the relative Chip Enable pin. In addition, each 8-Gbit device has its own maximum number of bad blocks and its own electronic signature code. The device operates from a 3 V power supply.

This document must be read in conjunction with the NAND04G-B2D_NAND08G-BxC datasheet, which fully details all the specifications required to operate this 4-Gbit/8-Gbit flash memory device.

The device is available in TSOP48 (12 × 20 mm) package and is shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to ‘1’.

Refer to the list of available part numbers and *Table 8: Ordering information scheme* for information on how to order these options.

Table 1. NAND16GW3B4D device summary

Density	Bus width	Page size	Block size	Memory array	Operating voltage (V_{DD})	Timings				Package
						Random access time (max)	Sequential access time (min)	Page program (typ)	Block erase (typ)	
16 Gbits	x8	2048+ 64 bytes	128 K + 4 K bytes	64 pages x 16384 blocks	2.7 to 3.6 V	25 ns	25 µs	200 µs	1.5 ms	TSOP48

Figure 1. Functional block diagram

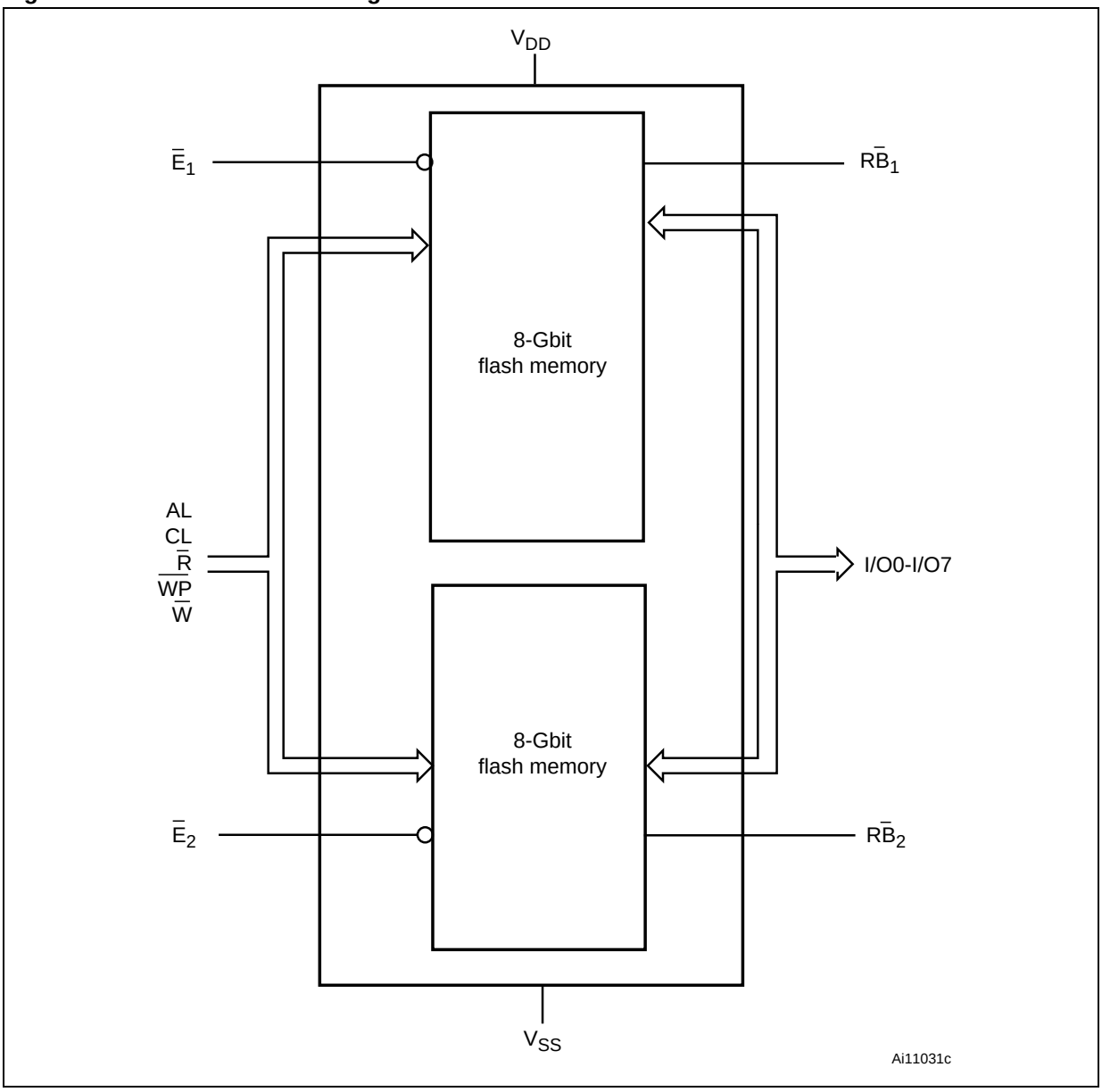


Figure 2. Logic diagram

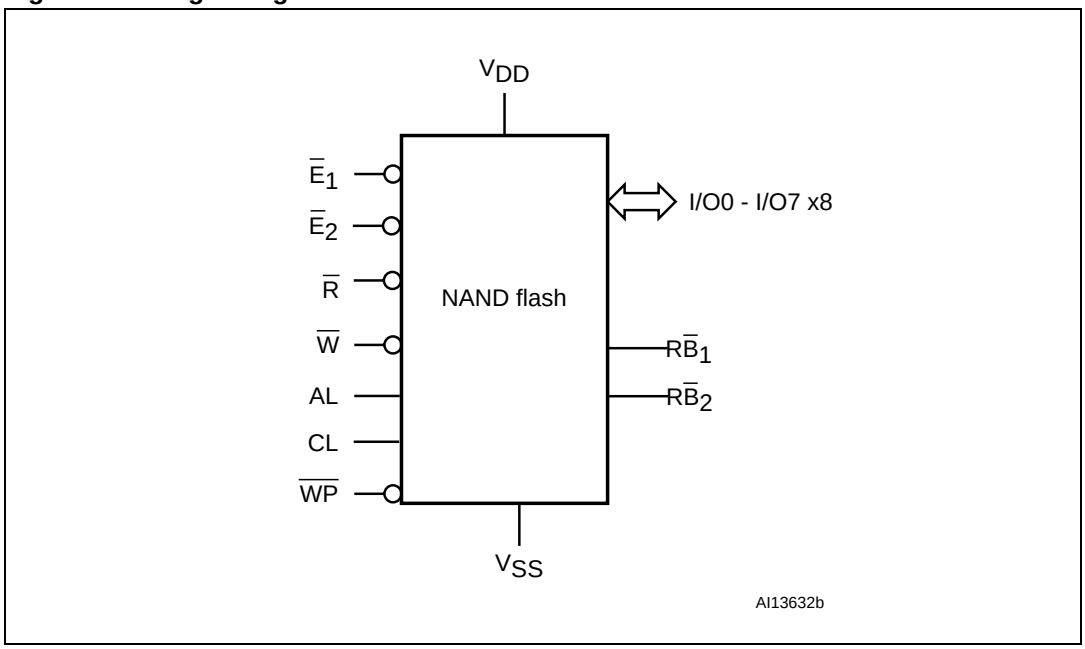
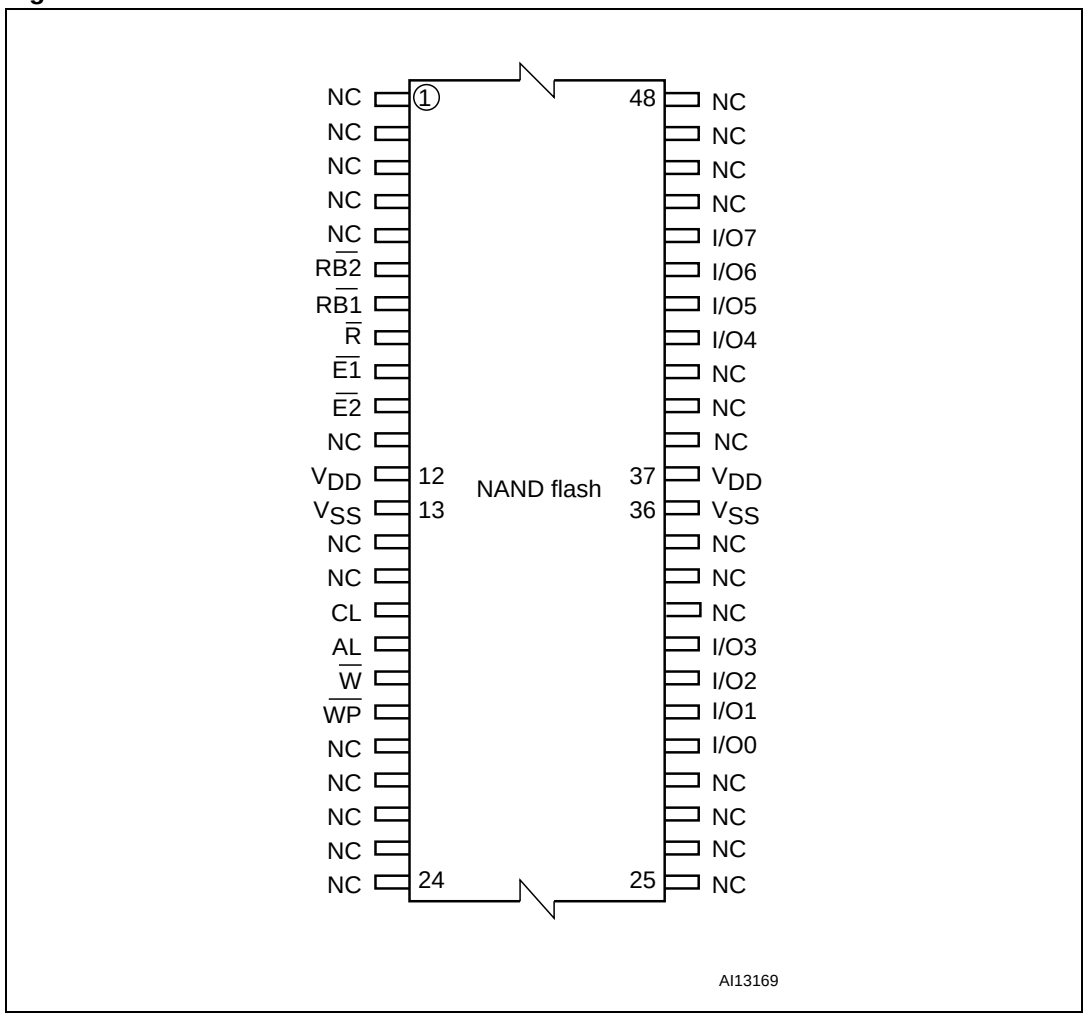


Table 2. Signal names

Signal	Function	Direction
I/O0 - I/O7	Data input/outputs	Input/output
CL	Command Latch Enable	Input
AL	Address Latch Enable	Input
$\overline{E}_1$, $\overline{E}_2$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
$R\overline{B}_1$, $R\overline{B}_2$	Ready/Busy (open drain output)	Output
V_{DD}	Power supply	Power supply
V_{SS}	Ground	Ground
NC	No connection	–
DU	Do not use	–

Figure 3. TSOP48 connections



2 Memory array organization

The memory array is split into two dice. Each dice is comprised of NAND structures where 32 cells are connected in series.

The array is organized into blocks, where each block contains 64 pages. The array is split into two areas: the main area and the spare area. The main area of the array stores data, whereas the spare area typically stores software flags or bad block identification.

The pages are split into a 2048-byte main area and a spare area of 64 bytes.

2.1 Bad blocks

The NAND16GW3B4D device may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to the bad block management section of the NAND04G-B2D_NAND08G-BxC datasheet for more details).

Table 3: Valid blocks shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on. Each 8-Gbit device can have the same maximum number of bad blocks.

These blocks need to be managed using bad blocks management and block replacement (refer to the software algorithms section of the NAND04G-B2D_NAND08G-BxC datasheet).

Table 3. Valid blocks

Density of device	Minimum	Maximum
16 Gbits	16064	16384

2.2 Parallel operation

The NAND16GW3B4D is composed of two 8-Gbit devices, each one driven by its Chip Enable pin ($\overline{E}_1$ and $\overline{E}_2$, respectively). It is possible to drive the two 8-Gbit devices in parallel, thus increasing the throughput in Mbyte/s.

When one of the two devices is in a busy state, other operations can be issued on the other available device.

3 Signal descriptions

See *Figure 1: Functional block diagram*, and *Table 2: Signal names* for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Chip Enable ($\overline{E}_1$, $\overline{E}_2$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.7 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.8 Ready/Busy ($R\overline{B}_1$, $R\overline{B}_2$)

The Ready/Busy output, $R\overline{B}_1$ and $R\overline{B}_2$, is an open-drain output that can identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low indicates that one, or more, of the memories is busy.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the Ready/Busy signal is Low, V_{OL}.

Refer to *Section 6: Package mechanical* for details on how to calculate the value of the pull-up resistor.

3.9 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for operations (read, program, and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.10 V_{SS} ground

Ground, $V_{SS,}$ is the reference for the power supply. It must be connected to the system ground.

4 Maximum ratings

Stressing the device above the ratings listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	– 50	125	°C
T_{STG}	Storage temperature	– 65	150	°C
V_{IO}(1)	Input or output voltage	– 0.6	4.6	V
V_{DD}	Supply voltage	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

5 DC and AC parameters

This section summarizes the operating and measurement conditions as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in *Table 5: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement conditions

Parameter	Min	Max	Units
Supply voltage (V_{DD})	2.7	3.6	V
Ambient temperature (T_A)	0	70	°C
	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	50		pF
Input pulses voltages	0	V_{DD}	V
Input and output timing ref. voltages	$V_{DD}/2$		V
Output circuit resistor R_{ref}	8.35		kΩ
Input rise and fall times	5		ns

Table 6. Capacitance(1)

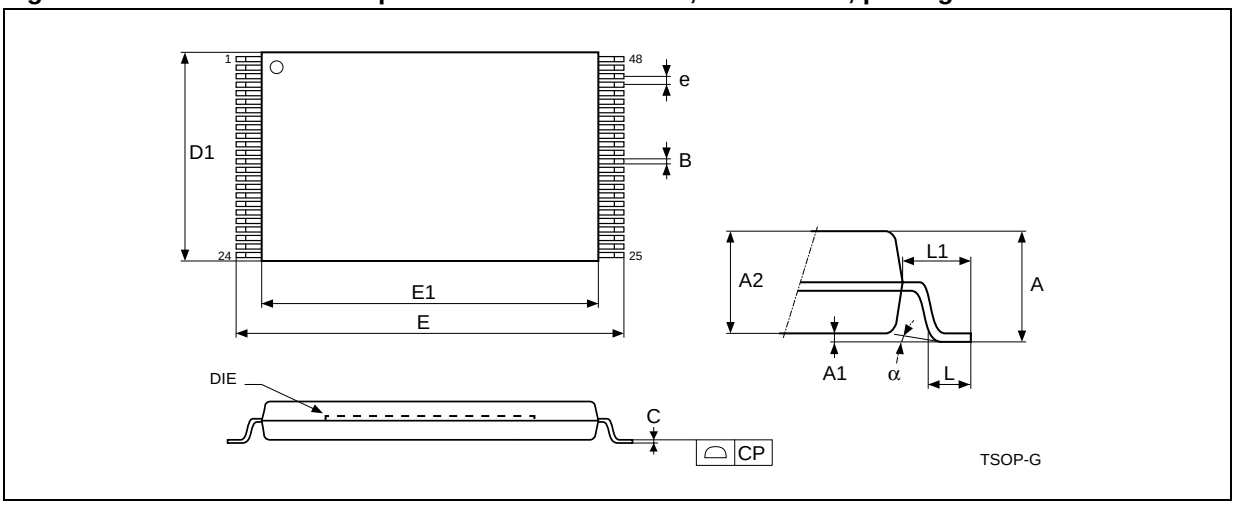
Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance	V_{IL} = 0 V		10	pF

1. T_A = 25 °C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.

6 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages, which are lead-free. In compliance with JEDEC standard JESD97 the category of second level interconnect is marked on the package and on the inner box label. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 4. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline



1. Drawing is not to scale.

Table 7. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.08			0.003
D1	12.00	11.90	12.10	0.472	0.468	0.476
E	20.00	19.80	20.20	0.787	0.779	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	
L	0.60	0.50	0.70	0.024	0.020	0.028
L1	0.80			0.031		
a	3°	0°	5°	3°	0°	5°

7 Ordering information

Table 8. Ordering information scheme

Example: NAND16G W 3 B 4 D N 6 E

Device type

NAND flash memory

Density

16G = 16 Gbits

Operating voltage

W = V_{DD} = 2.7 to 3.6 V

Bus width

3 = x8

Family identifier

B = 2112-byte page

Device options

4 = Chip Enable ‘don't care’ enabled with 2 Chip Enable and 2 Ready/Busy signals

Product version

D = first version

Package

N = TSOP48 12 x 20 mm

Temperature range

6 = –40 to 85 °C

Option

E = ECOPACK® package, standard packing

F = ECOPACK® package, tape and reel packing

Note: Devices are shipped from the factory with the memory content bits, in valid blocks, erased to ‘1’. For further information on any aspect of this device, please contact your nearest Numonyx sales office.

8 Revision history

Table 9. Document revision history

Date	Revision	Changes
06-Jun-2008	1	Initial release.
27-Jun-2008	2	Changed datasheet's name and modified the reference to the 4-Gbit/8-Gbit datasheet in *Section 1: Description* and *Section 2.1: Bad blocks*.

Please Read Carefully: