

PH955L

N-channel TrenchMOS™ logic level FET

Rev. 01 — 1 March 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Very low on-state resistance

1.3 Applications

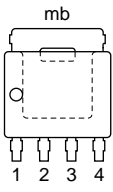
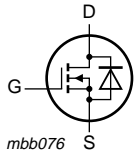
- DC-to-DC converters
- Motors, lamps and solenoids
- General purpose power switching
- Portable appliances

1.4 Quick reference data

- $V_{DS} \leq 55$ V
- $I_D \leq 62.5$ A
- $R_{DS(on)} \leq 8.3$ m Ω
- $Q_{gd} = 16.4$ nC (typ)

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
mb	mounting base; connected to drain (D)		

SOT669 (LFPACK)

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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PH955L	LFAK	plastic single-ended surface mounted package; 4 leads	SOT669

4. Limiting values

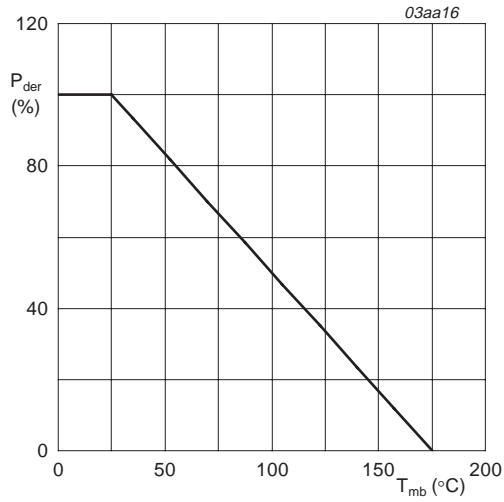
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2 and Figure 3	-	62.5	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2	-	43.7	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	187	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	156	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 44\text{ A}$; $t_p = 0.1\text{ ms}$; $V_{DD} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; starting at $T_j = 25\text{ °C}$	-	195	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 4.4\text{ A}$; $t_p = 0.1\text{ ms}$; $V_{DD} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$	[1] - [2]	2	mJ

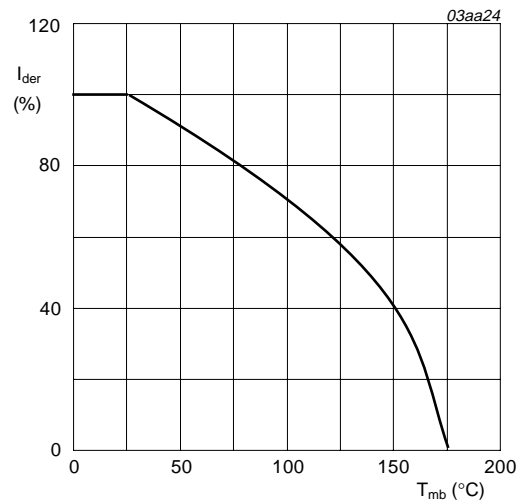
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



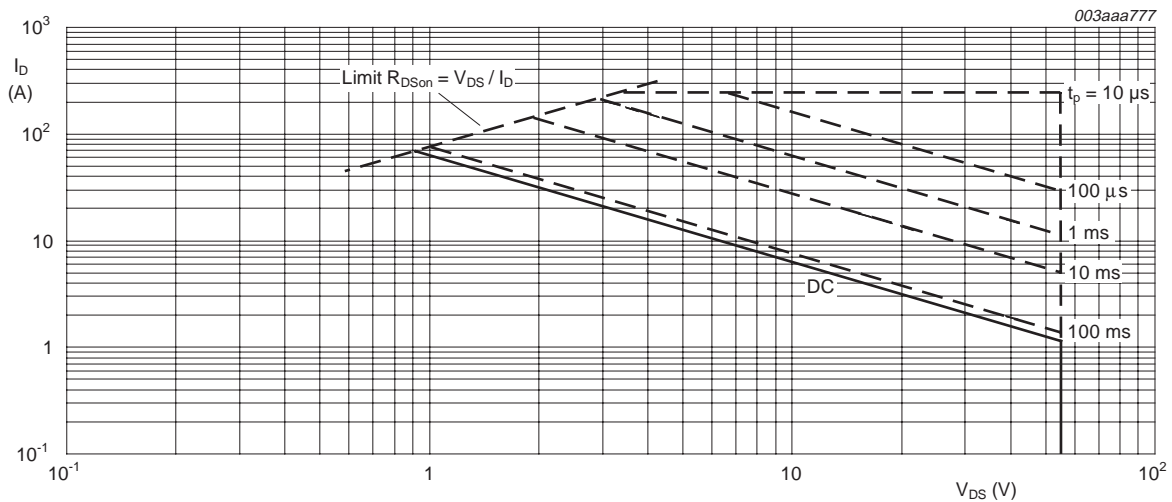
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^\circ C$; I_{DM} is single pulse; $V_{GS} = 10 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

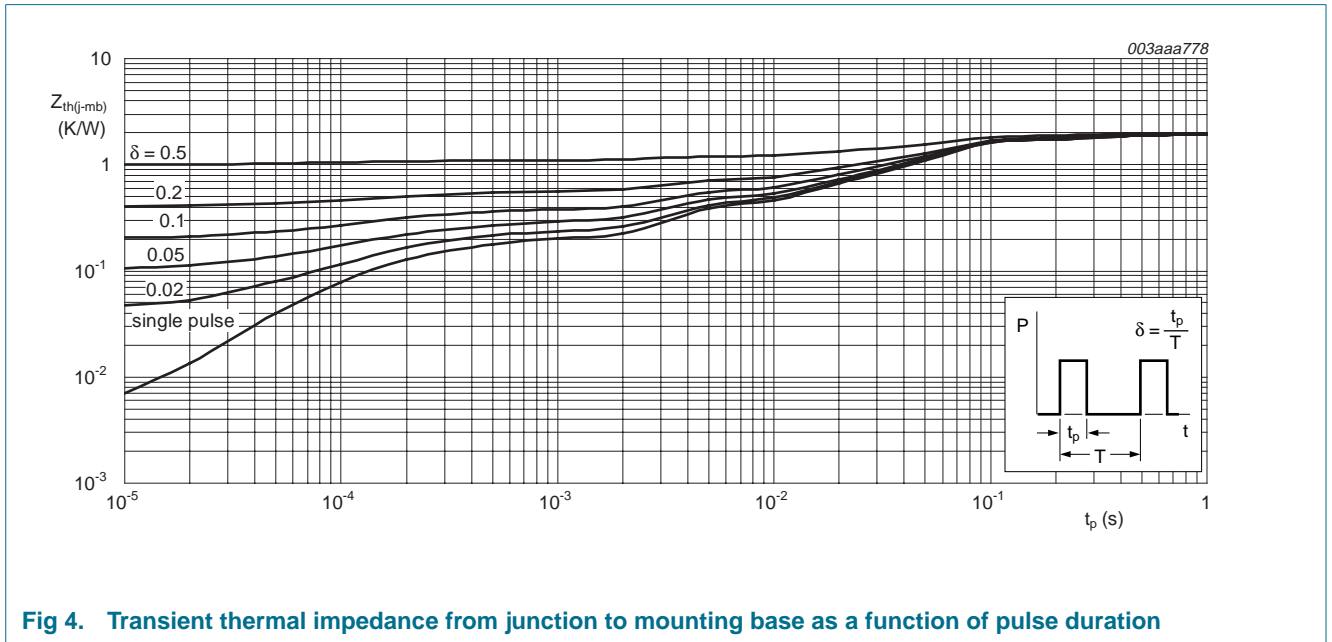
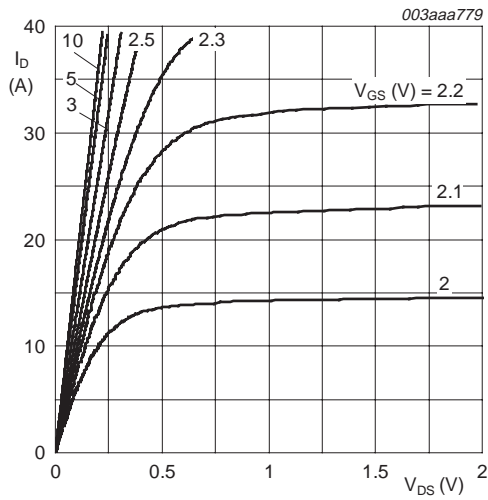


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

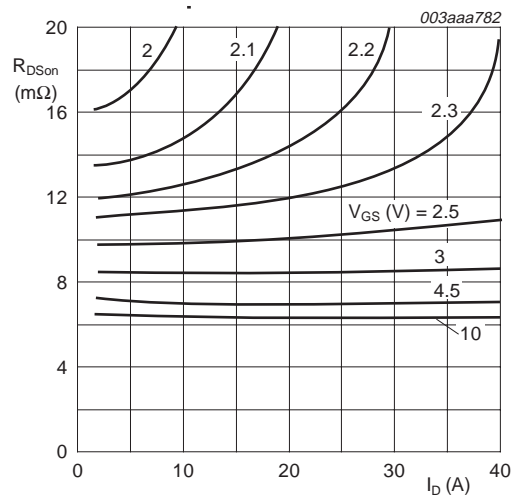
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C T _j = -55 °C	55 50	- -	- -	V V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10 T _j = 25 °C T _j = 150 °C T _j = -55 °C	1 0.5 -	1.5 - -	2 - 2.3	V V V
I _{DSS}	drain-source leakage current	V _{DS} = 55 V; V _{GS} = 0 V T _j = 25 °C T _j = 150 °C	- - -	0.02 - -	1 500	μA μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A T _j = 25 °C; Figure 6 T _j = 150 °C; Figure 8 V _{GS} = 4.5 V; I _D = 25 A	- - -	6.2 - 7.1	8.3 16 9.9	mΩ mΩ mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 25 A; V _{DD} = 44 V; V _{GS} = 5 V; Figure 11 and Figure 12	-	42	-	nC
Q _{gs}	gate-source charge		-	5.7	-	nC
Q _{gs1}	pre-V _{GS(th)} gate-source charge		-	4.3	-	nC
Q _{gs2}	post-V _{GS(th)} gate-source charge		-	1.4	-	nC
Q _{gd}	gate-drain (Miller) charge		-	16.4	-	nC
V _{plat}	plateau voltage		-	2	-	V
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 14	-	2 836	-	pF
C _{oss}	output capacitance		-	441	-	pF
C _{rss}	reverse transfer capacitance		-	210	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 25 V; R _L = 1 Ω; V _{GS} = 5 V; R _G = 4.7 Ω	-	18	-	ns
t _r	rise time		-	71	-	ns
t _{d(off)}	turn-off delay time		-	105	-	ns
t _f	fall time		-	25	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 13	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _R = 30 V	-	62	-	ns
Q _r	recovered charge		-	48	-	nC



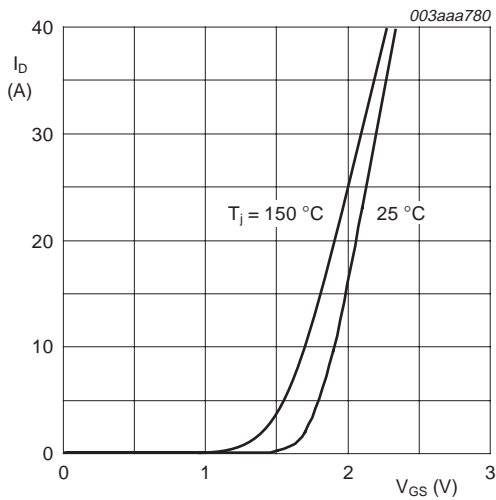
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



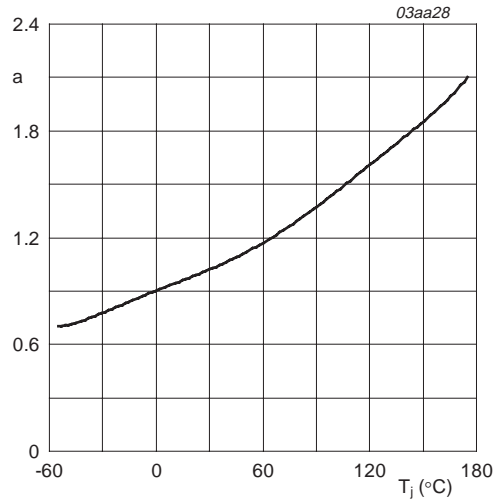
$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



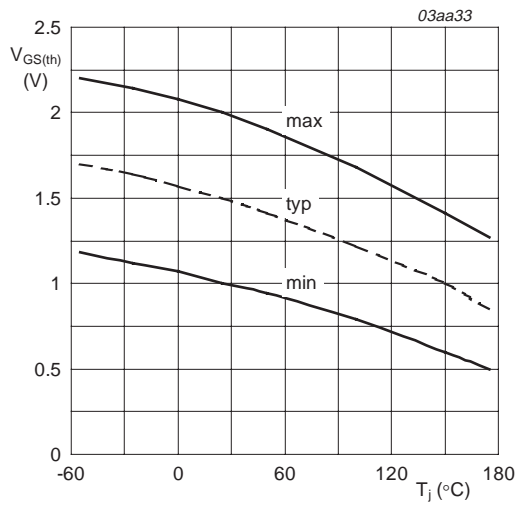
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



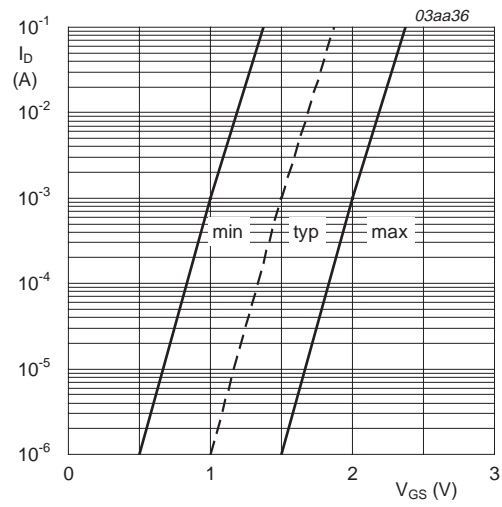
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



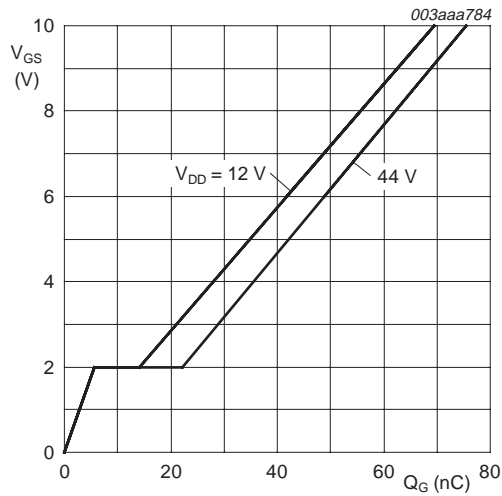
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}; V_{DD} = 12 \text{ V and } 44 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

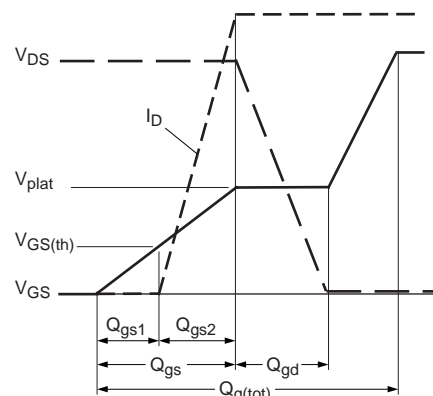
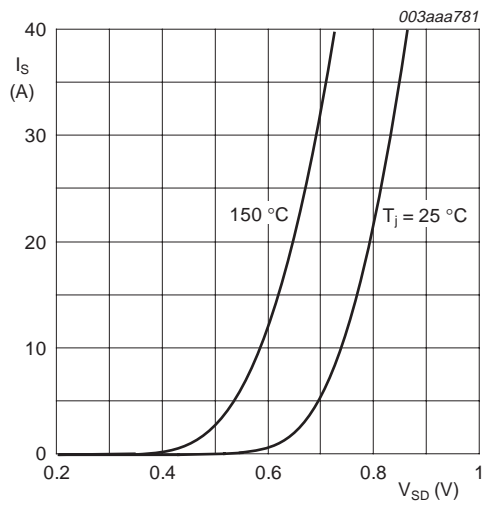
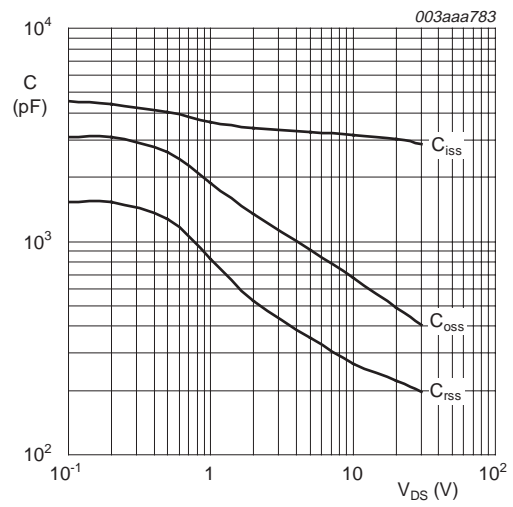


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

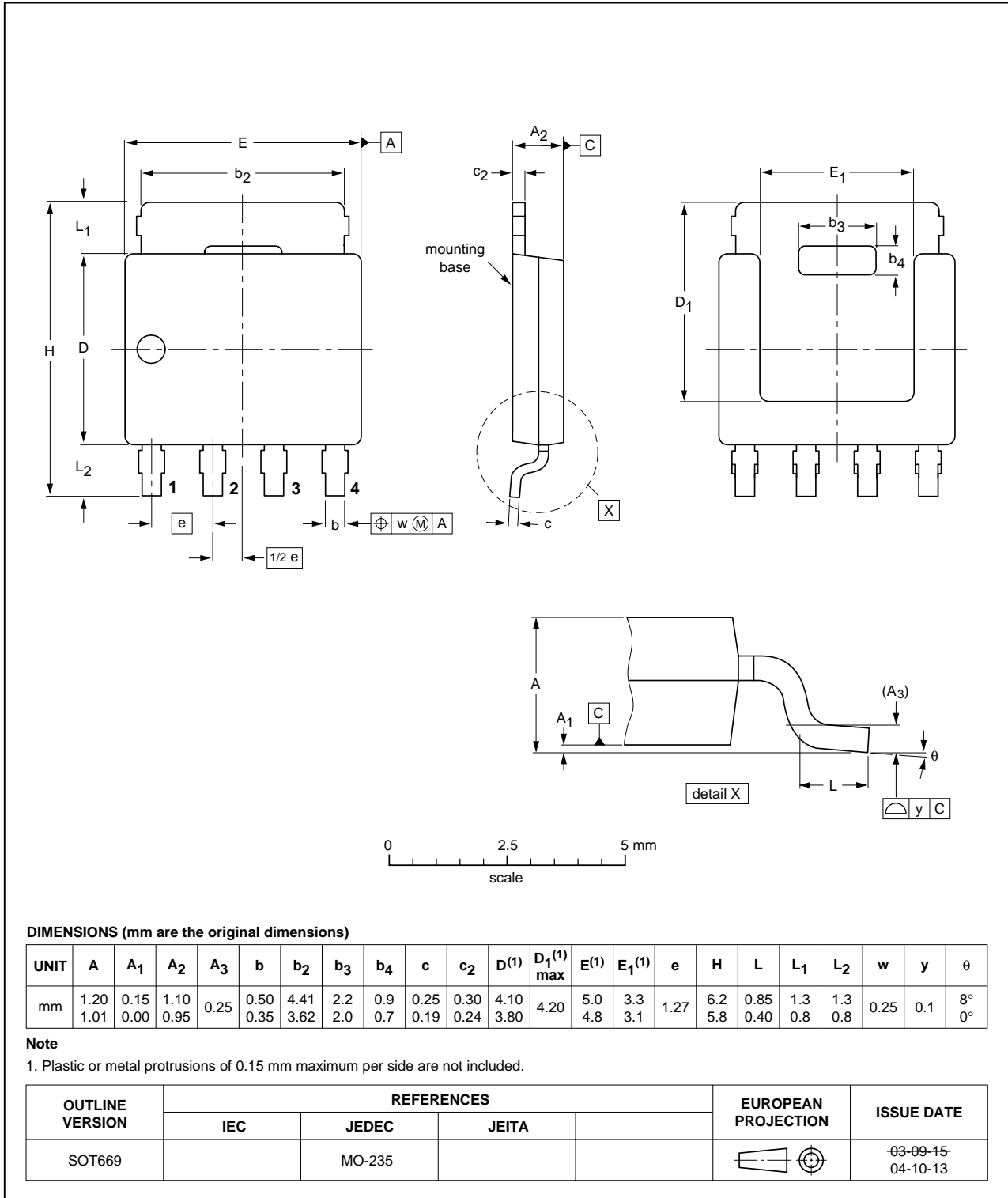


Fig 15. Package outline SOT669 (LPAK)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH955L_1	20050301	Product data sheet	-	9397 750 14557	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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