PHK18NQ03LT

N-channel TrenchMOS logic level FET

Rev. 01 — 18 December 2006 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Optimized for use in DC-to-DC converters
- Logic level compatible
- Very low switching and conduction losses

1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers

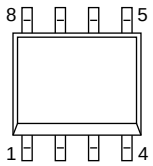
1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $R_{DSon} \leq 8.9$ mΩ
- $I_D \leq 20.3$ A
- $Q_{GD} = 2.5$ nC (typ)

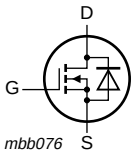
2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
5, 6, 7, 8	drain (D)		



SOT96-1 (SO8)



3. Ordering information

Table 2. Ordering information

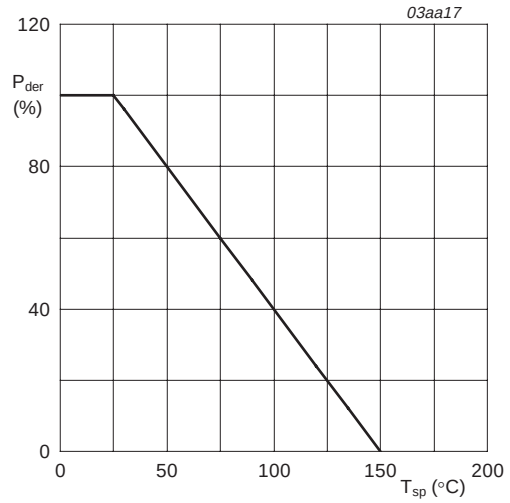
Type number	Package		
	Name	Description	Version
PHK18NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 3. Limiting values

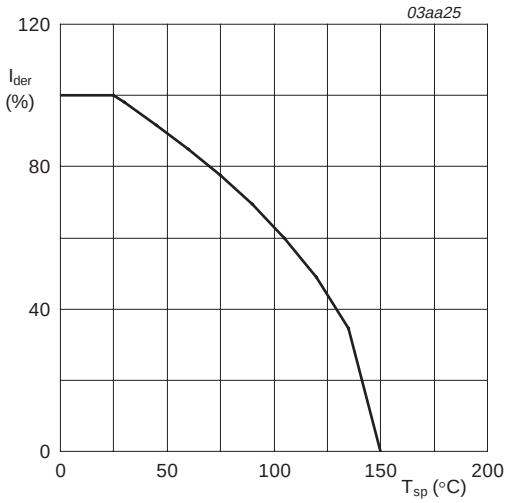
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		-	±20	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3	-	20.3	A
		T_{sp} = 100 °C; V_{GS} = 10 V; see Figure 2	-	12.1	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	80	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 1	-	6.25	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current	T_{sp} = 25 °C	-	5.2	A
I_{SM}	peak source current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	20.8	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 31.5 A; t_p = 0.07 ms; V_{DS} ≤ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	-	50	mJ



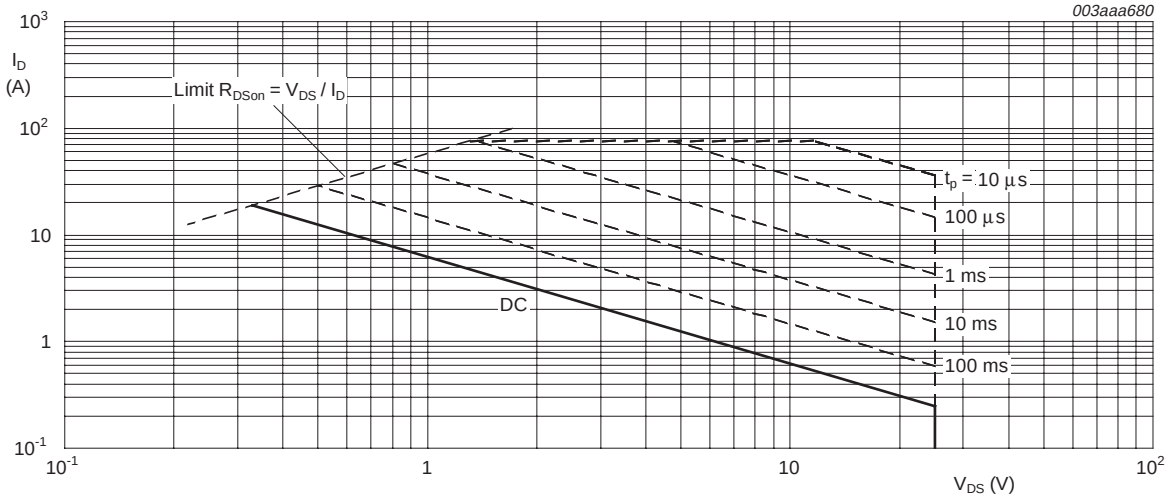
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	20	K/W

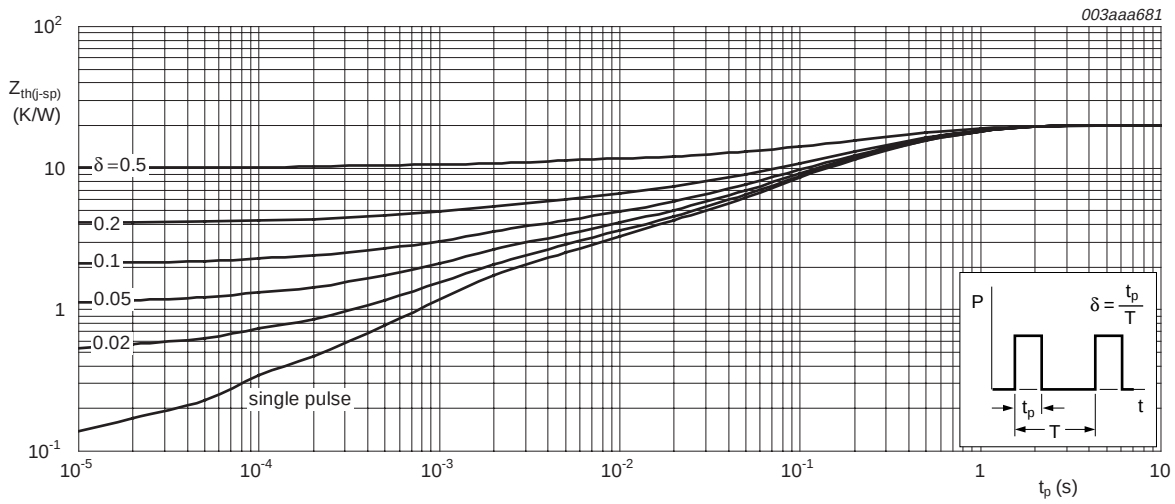


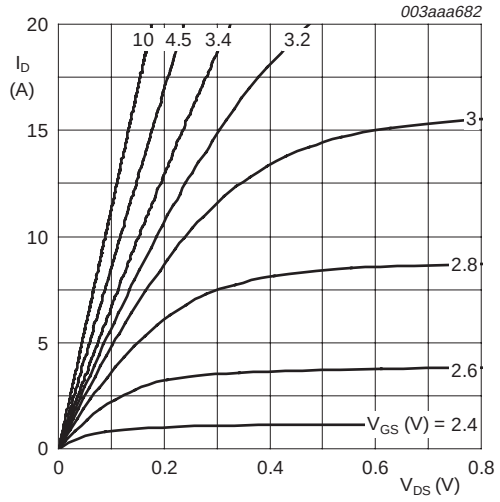
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5. Characteristics

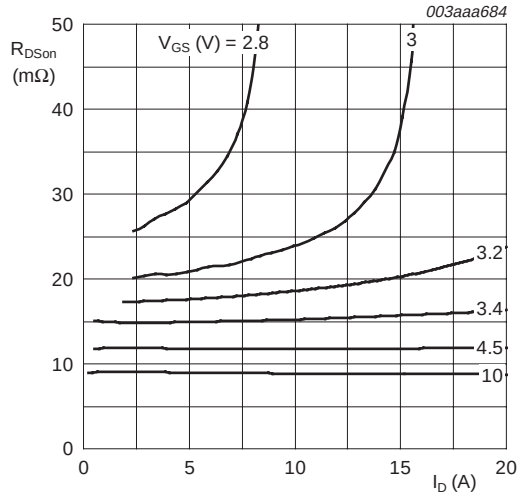
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	1.3	1.7	2.15	V
		T_j = 150 °C	0.8	-	-	V
		T_j = –55 °C	-	-	2.6	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = ±16 V; V_{DS} = 0 V	-	-	100	nA
R_G	gate resistance	f = 1 MHz; $V_{GSS(AC)}$ = 150 mV	-	1.6	-	Ω
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; see Figure 6 and 8				
		T_j = 25 °C	-	7.1	8.9	mΩ
		T_j = 150 °C	-	12.1	15.1	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; see Figure 6 and 8	-	10.1	12.5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 11 and 12	-	10.6	-	nC
Q_{GS}	gate-source charge		-	4.85	-	nC
Q_{GS1}	pre-$V_{GS(th)}$ gate-source charge		-	2.4	-	nC
Q_{GS2}	post-$V_{GS(th)}$ gate-source charge		-	2.45	-	nC
Q_{GD}	gate-drain charge		-	2.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	3	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 12 V; f = 1 MHz; see Figure 14	-	1380	-	pF
C_{oss}	output capacitance		-	290	-	pF
C_{rss}	reverse transfer capacitance		-	135	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 0 V; f = 1 MHz	-	1590	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.8 Ω; V_{GS} = 4.5 V; R_G = 5.6 Ω	-	19	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	11	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; see Figure 13	-	0.95	1.2	V
t_{rr}	reverse recovery time	I_S = 15 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V	-	34	-	ns
Q_r	recovered charge		-	14	-	nC



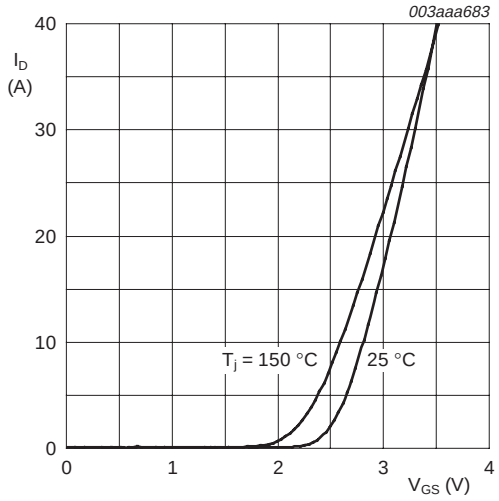
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



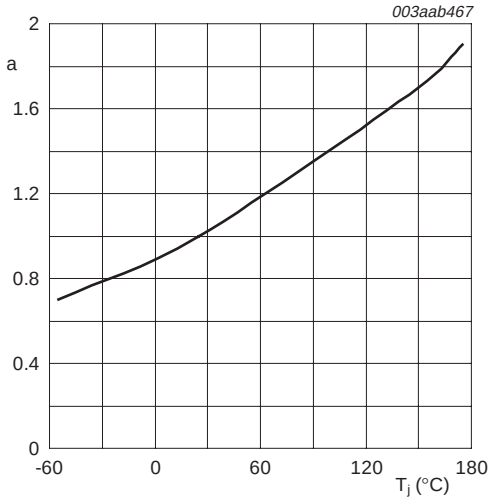
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



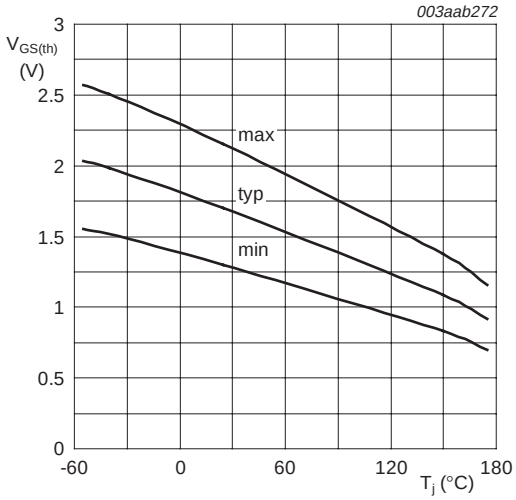
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



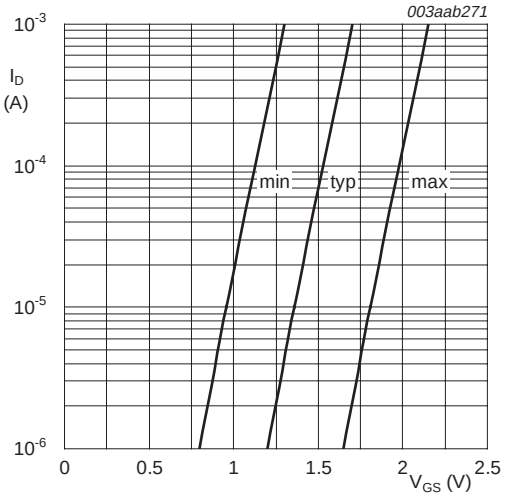
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



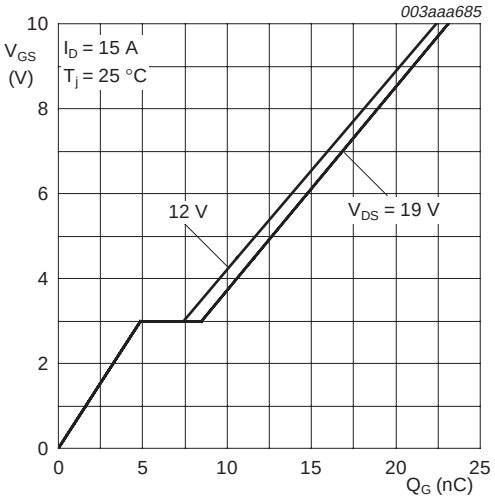
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



I_D = 15 A; V_{DS} = 12 V and 19 V

Fig 11. Gate-source voltage as a function of gate charge; typical values

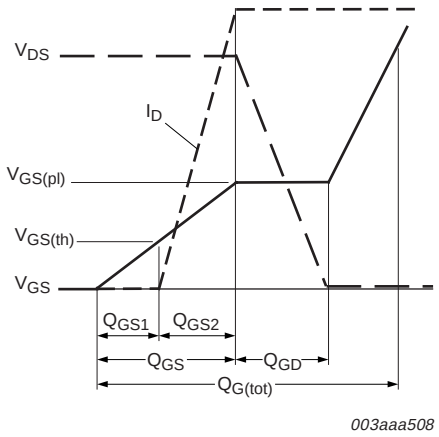
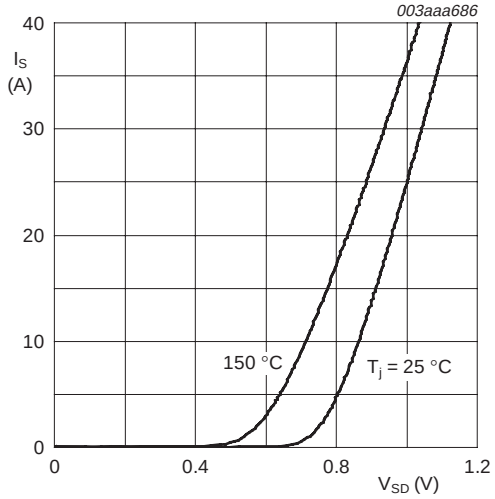
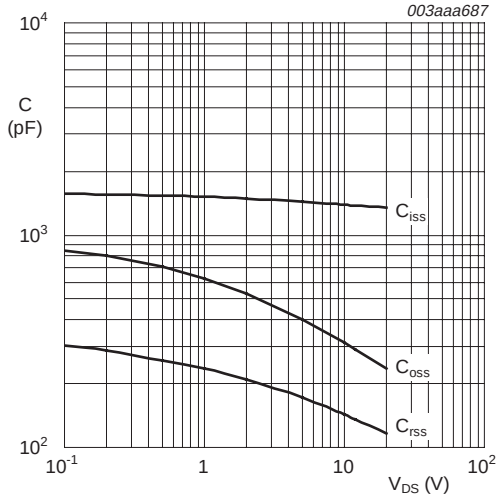


Fig 12. Gate charge waveform definitions



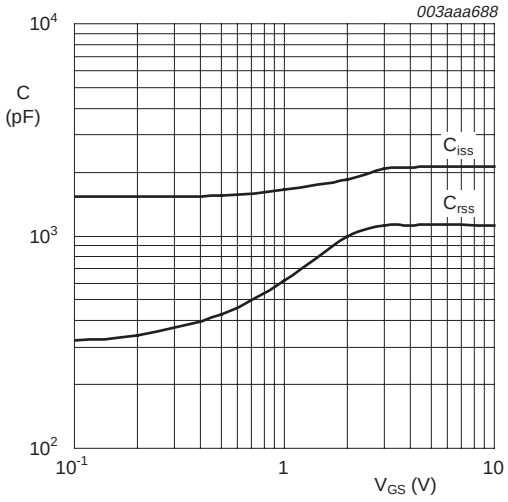
T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source current as a function of source-drain voltage; typical values



V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

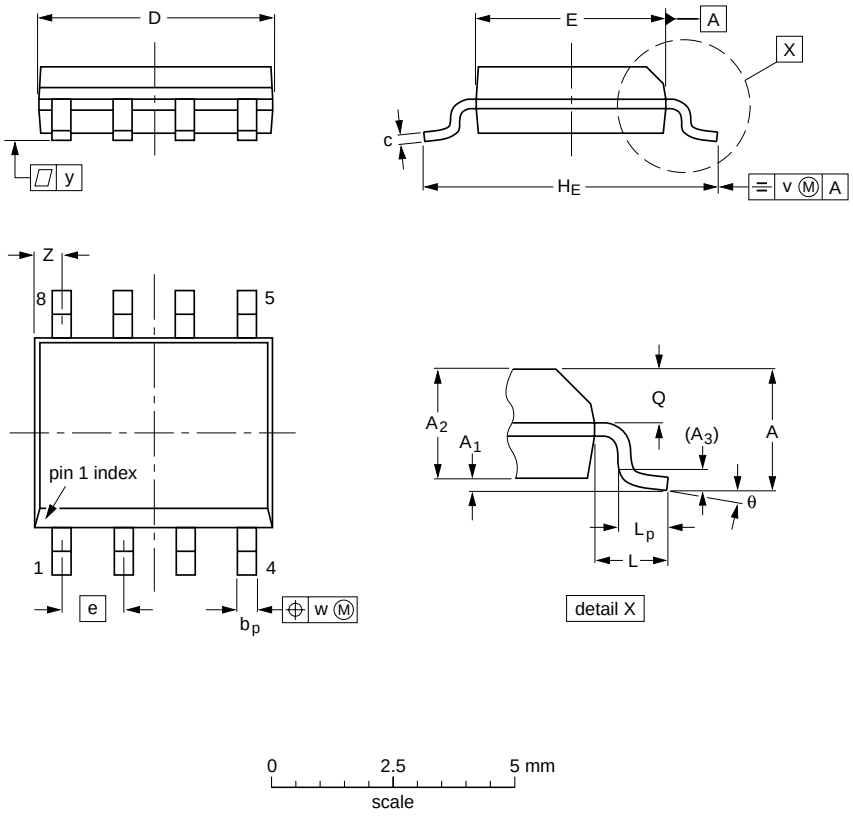


V_{GS} = 0 V; f = 1 MHz

Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK18NQ03LT_1	20061218	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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