

PHP28NQ15T

N-channel TrenchMOS standard level FET

Rev. 01 — 17 August 2005

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low body diode Q_r
- Fast switching

1.3 Applications

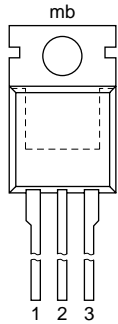
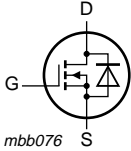
- DC-to-DC converters
- DC-to-AC inverters
- Switched-mode power supplies
- Class-D audio

1.4 Quick reference data

- $V_{DS} \leq 150$ V
- $I_D \leq 28.5$ A
- $R_{DS(on)} \leq 65$ m Ω
- $Q_{GD} = 7.5$ nC (typ)

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)		
3	source (S)		
mb	mounting base; connected to drain		

SOT78 (TO-220AB)

3. Ordering information

Table 2: Ordering information

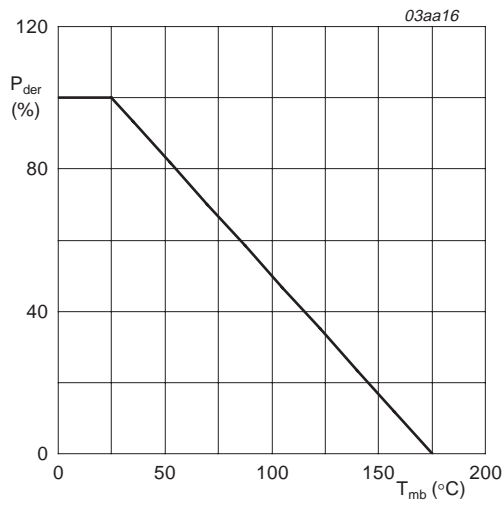
Type number	Package		Version
	Name	Description	
PHP28NQ15T	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 3: Limiting values

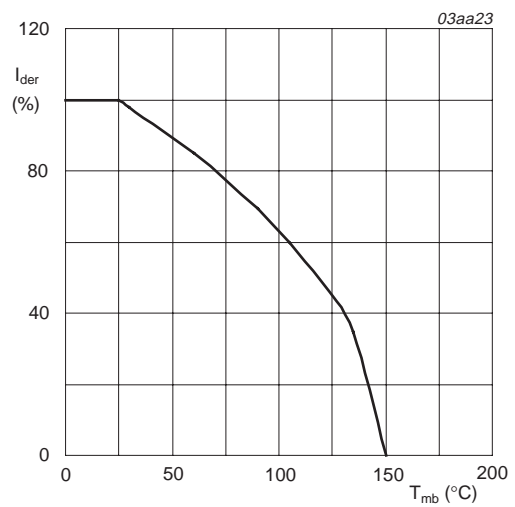
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	150	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	150	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	28.5	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	20.2	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	57.1	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	150	W
T_{stg}	storage temperature		-55	+175	$^{\circ}\text{C}$
T_j	junction temperature		-55	+175	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	28.5	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	57.1	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 9.9\text{ A}$; $t_p = 0.1\text{ ms}$; $V_{DD} \leq 150\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	100	mJ



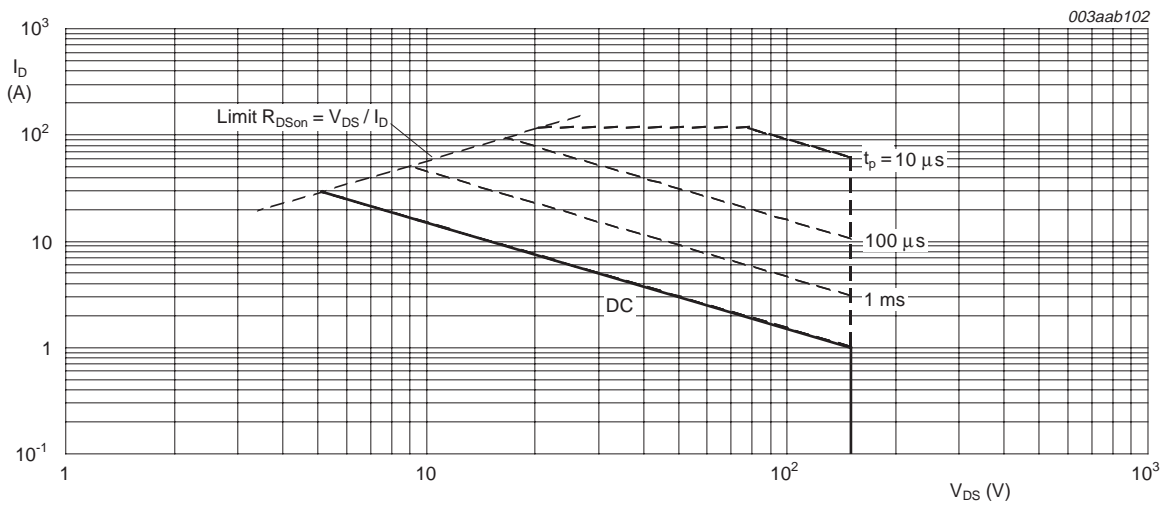
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^\circ C$; I_{DM} is single pulse; $V_{GS} = 10\text{ V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W

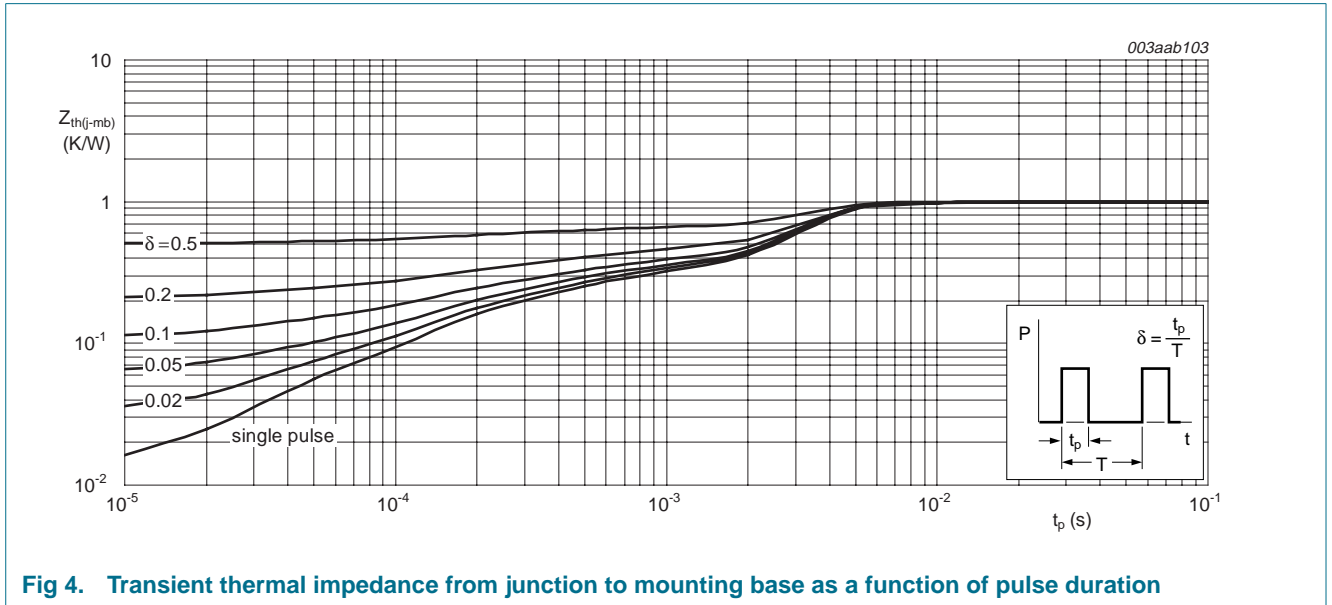
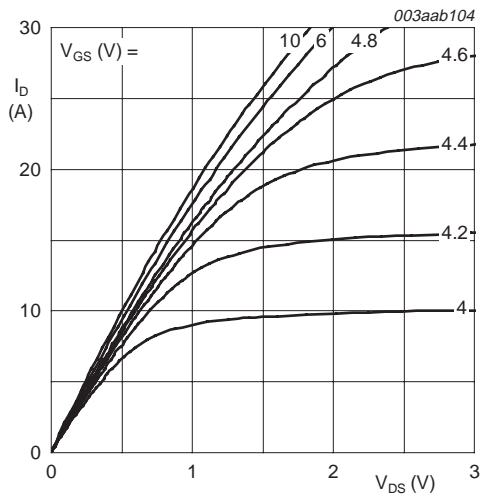


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

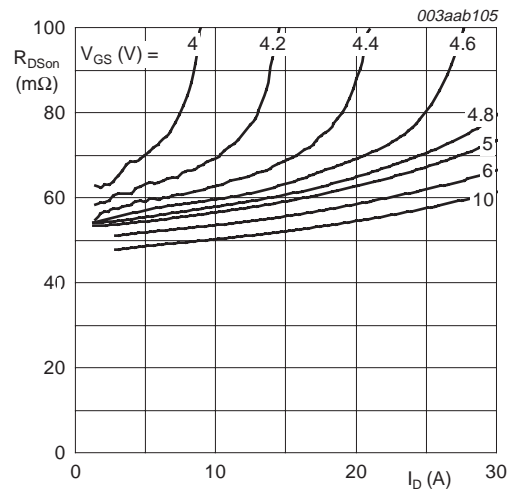
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C T _j = -55 °C	150 135	- -	- -	V V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; see Figure 9 and 10 T _j = 25 °C T _j = 175 °C T _j = -55 °C	2 1 -	3 - -	4 - 4.4	V V V
I _{DSS}	drain leakage current	V _{DS} = 120 V; V _{GS} = 0 V T _j = 25 °C T _j = 175 °C	- - -	- - -	1 500	μA μA
I _{GSS}	gate leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	10	100	nA
R _G	gate resistance	f = 1 MHz	-	1.1	-	Ω
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 18 A; see Figure 6 and 8 T _j = 25 °C T _j = 175 °C	- - -	54 145	65 175	mΩ mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 75 V; V _{GS} = 10 V; see Figure 11 and 12	-	24	-	nC
Q _{GS}	gate-source charge		-	6	-	nC
Q _{GD}	gate-drain charge		-	7.5	-	nC
V _{GS(pl)}	gate-source plateau voltage		-	5	-	V
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 30 V; f = 1 MHz; see Figure 14	-	1250	-	pF
C _{oss}	output capacitance		-	185	-	pF
C _{rss}	reverse transfer capacitance		-	55	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 75 V; R _L = 3 Ω; V _{GS} = 10 V; R _G = 5.6 Ω	-	12	-	ns
t _r	rise time		-	20	-	ns
t _{d(off)}	turn-off delay time		-	12	-	ns
t _f	fall time		-	55	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; see Figure 13	-	0.87	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	110	-	ns
Q _r	recovered charge		-	170	-	nC



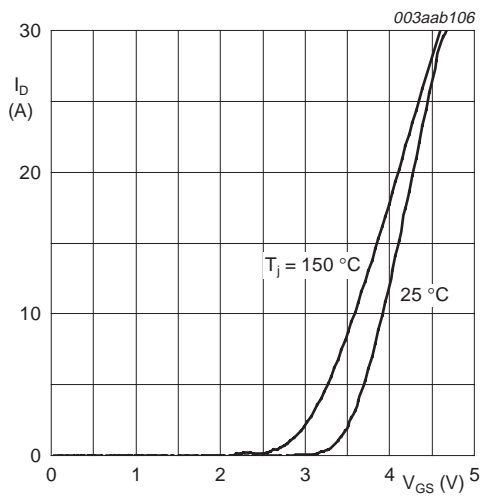
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



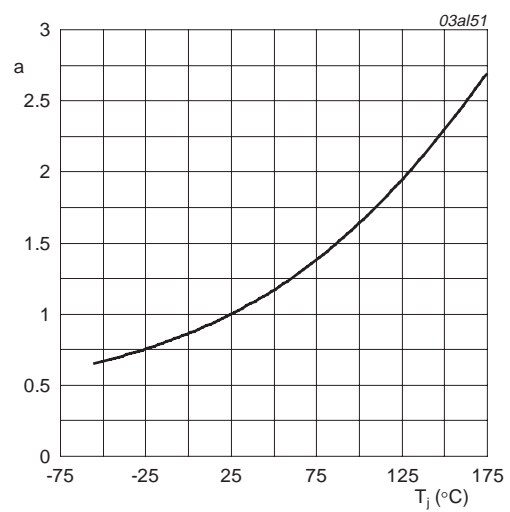
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



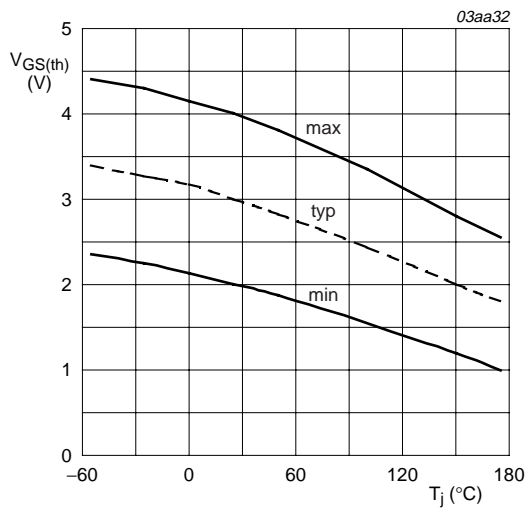
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



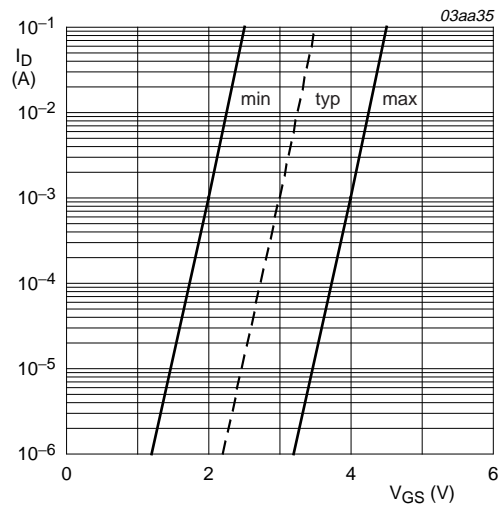
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



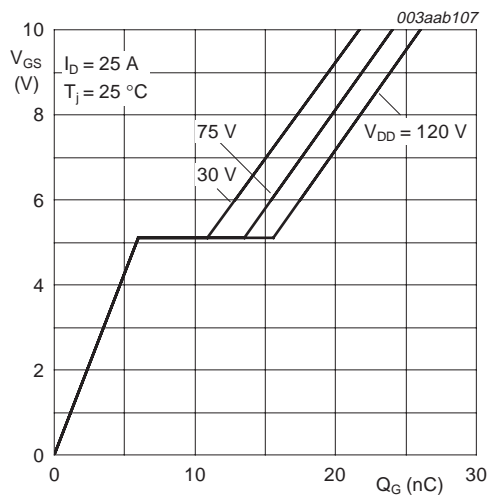
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



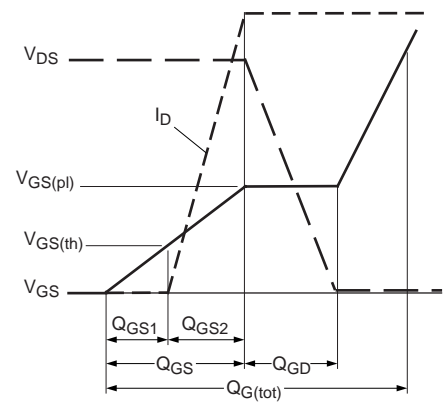
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



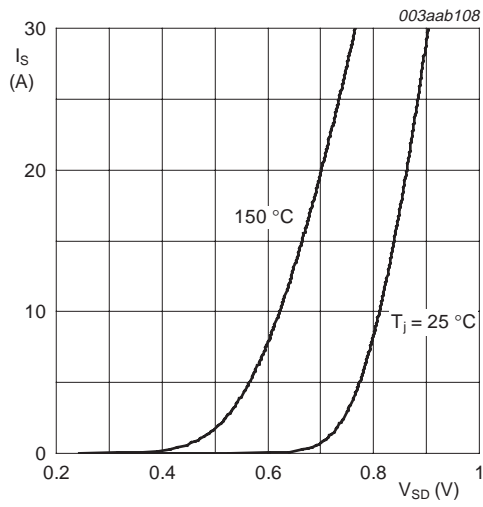
$I_D = 25 \text{ A}; V_{DS} = 30 \text{ V}, 75 \text{ V and } 120 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



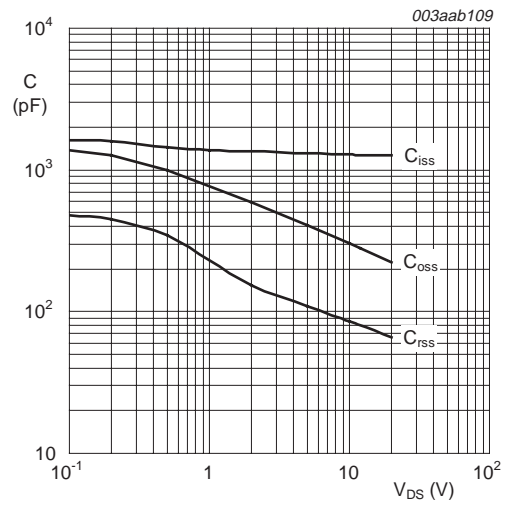
003aaa508

Fig 12. Gate charge waveform definitions



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

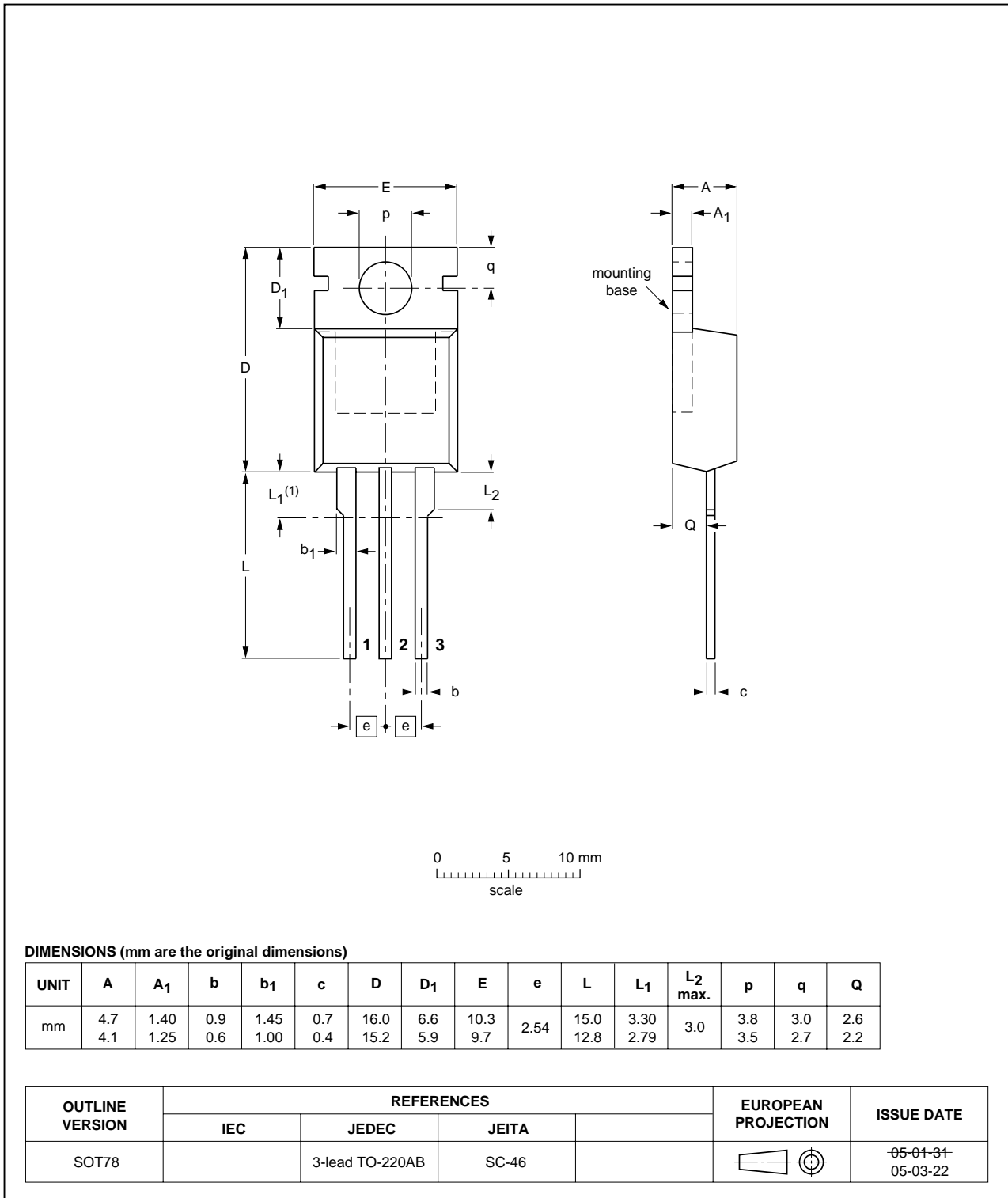


Fig 15. Package outline SOT78 (TO-220AB)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PHP28NQ15T_1	20050817	Product data sheet	-	-	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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