POWERTIP TECH. CORP.

SPECIFICATIONS

CUSTOMER	:	PTC
SAMPLE CODE (Ver.)	:	PPT9999-A003-06-Q (Ver.A)
MASS PRODUCTION CODE (Ver.)	:	PPT9999-A003-06-Q (Ver.A)
DRAWING NO. (Ver.)	:	PPT-06002-007 (Ver.A)

Customer Approved

Date:

Approved	QC Confirmed	Designer
研發 2007-6-22. 黃秋源	Q.A. DEPT. JUN 20 2007 POWERTIP TECH CORP. 王耀宗 2007.6.20	研發 95.6.13 張慶源 研發 2007-6-11. 黃俊清

☐ Approval For Specifications Only.

* This specification is subject to change without notice.

Please contact Powertip or it's representative before designing your product based on this specification.

■ Approval For Specifications and Sample.

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RECORDS OF REVISION

Date	Ver.	Description	Page	Design by
2007/05/18	0	New Sample.	—	Ackey
2007/06/11	A	Modify FPC outline.	—	Ackey

Total：22 Page

Contents

Note：For detailed information please refer to IC data sheet：Samsung --- S6E63D6

1. SPECIFICATIONS

1.1 Features

Item	Standard Value
Display Type	240 * (RGB) * 320 Dots
LCD Type	OLED
Color Mode	Full Color (262K color)
Driver Mode	Active Matrix
Screen size(inch)	2.4(Diagonal)
Interface	MPU i80-system 18-/16-9-8-Bit bus interface MPU i68-system 18-/16-9-8-Bit bus interface Serial data transfer interface RGB 18-/16-/6-bit bus interface(DOTCLK,VSYNC,HSYNC,DE,DB17-0)
Controller IC	Driver IC : Samsung --- S6E63D6
ROHS	THIS PRODUCT CONFORMS THE ROHS OF PTC Detail information please refer web side : http://www.powertip.com.tw/news/LatestNews.asp

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	42.6 (W) * 59.2 (L) * 1.65 (H)	mm

OLED panel

Item	Standard Value	Unit
Active Area	36.72 (W) * 48.96 (L)	mm

Note : For detailed information please refer to LCM drawing

1.3 Absolute Maximum ratings:

Items	Symbol	Unit	Value	Note
Power supply voltage 1	VDD3	V	-0.3~+5.0	
Power supply voltage 2	VCI	V	-0.3~+5.0	
Supply Voltage range	| VLIN2-VLIN3|	V	20	
Input Voltage range	Vin	V	-0.3~VDD+0.5	

Note:

(1)Absolute maximum rating is the limit value. When the IC is exposed operation environment beyond this range, the IC do not assure operations and may be damaged permanently, not be able to be recovered.

(2)Absolute maximum rating is guaranteed only when our company's package used.

1.4 DC Electrical Characteristics

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Driving voltage	VGH	-	3.0	-	8.0	V	
	VGL		-8.0	-	-3.0	V	
	VINT		-4.0	-	-1.0	V	
Logic Operating Voltage	RVDD	-	1.45	1.5	1.55	V	
Operating frequency	Fose	Frame frequency=60Hz Display line=320 line	1161.1	1290.2	1419.3	KHz	
1st step-up input voltage	VCI1	-	2.1	-	2.75	V	
1st step-up output voltage	VLOUT1	Without load	+4.6	-	+5.5	V	
1st step-up output efficiency	VLOUT1	$I_{\_VLOUT1\_LOAD}$=2.3mA	90	95	-	%	
2nd step-up output voltage	VLOUT2	Without load		8.1		V	
2nd step-up output efficiency	VLOUT2	$I_{\_VLOUT2\_LOAD}$=0.1mA	90	93	-	%	
3nd step-up output voltage	VLOUT3	Without load	-	-10.6	-	V	
3nd step-up output efficiency	VLOUT3	$I_{\_VLOUT3\_LOAD}$=0.1mA	90	93	-	%	
Source Output voltage deviation (channel to channel)	-	-	-	+/-TBD	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	+/-TBD	-	mV	
Source driver output Voltage range	Vso	-	0.96	-	4.2	V	

LTPS driver output voltage deviation	-	-	-	-	TBD	V	
Characteristic	**Symbol**	**CONDITION**	**MIN**	**TYP**	**MAX**	**Unit**	**Note**
Driving voltage	dVGH	Voltage deviation	-	-	TBD	V	
	dVGL		-	-	TBD	V	
Current consumption during normal operation	IVDD3	No load, Ta=25°C VCI=2.8V Frame(f)=60Hz	-	-	TBD	uA	-
	IVCI		-	-	TBD	mA	-

Characteristic	**Symbol**	**CONDITION**	**MIN**	**TYP**	**MAX**	**Unit**	**Note**
Power supply Voltage	VCI	Operating Voltage	2.5	2.8	3.3	V	
Power Supply Voltage	VDD3	I/O supply voltage	1.65	1.8	3.3	V	
Logic High level input voltage	V_{IH}		0.7*VDD3		VDD3	V	
Logic Low level input voltage	V_{IL}		0		0.3*VDD3	V	
Logic High level output voltage	V_{OH}	$I_{CUT=-1mA}$	0.8*VDD3		VDD3	V	
Logic Low level output voltage	V_{OL}	$I_{CUT=-+1mA}$	0		0.2*VDD3	V	

1.5 Electro- Optical Characteristics

Items	Symbol	Min.	Typ.	Max	Unit	Remark
Operating Luminance	L		200	-	Cd/ m^2	(1)(5)
Power Consumption	Pon	-	260	-	mW	30% Pixels on(1)
Response Time	Tres	-	-	50	US	(2)
CIEx(White)	Wx	0.26	0.30	0.34	-	(5)
CIEy(White)	Wy	0.30	0.34	0.38	-	(5)
Viewing Angle	VA	170	-			(3)
Contrast	CR	-	10000:1			(4)
Operation Lifetime	Ltop	10000			Hrs	(1)(6)
Storage lifetime	LTs	20000	-	-	Hrs	(7)

Note:

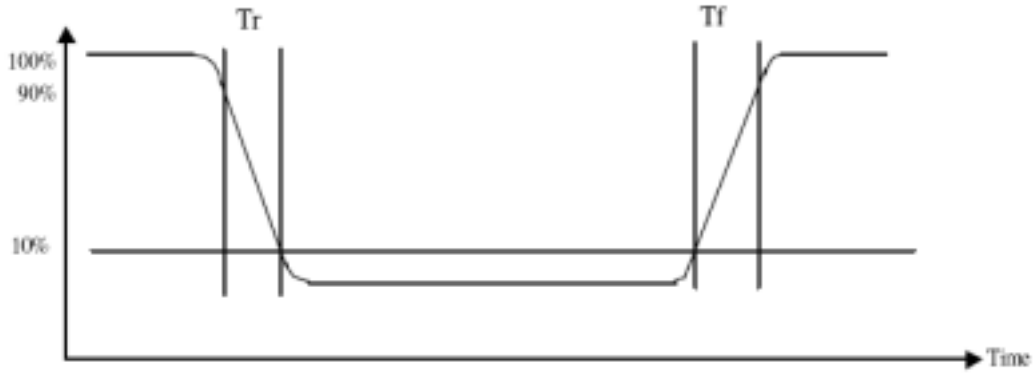
Measuring surrounding :dark room

Surrounding Temperature:25℃

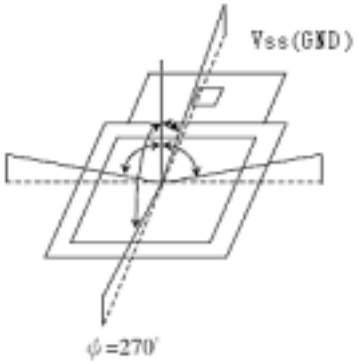
1. Test condition:

   TBD

2.response Time test condition



3.Viewing Angle test condition:



4.Contrast

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5.Optical tester: Topcon SR3

6.Full white with check board at 85Hz frame rate,1/96 duty. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.

7.The storage life time is define as 50% when the luminance has decayed to less than 50% of the minimum luminance under temperature 25°C,RH<50%.

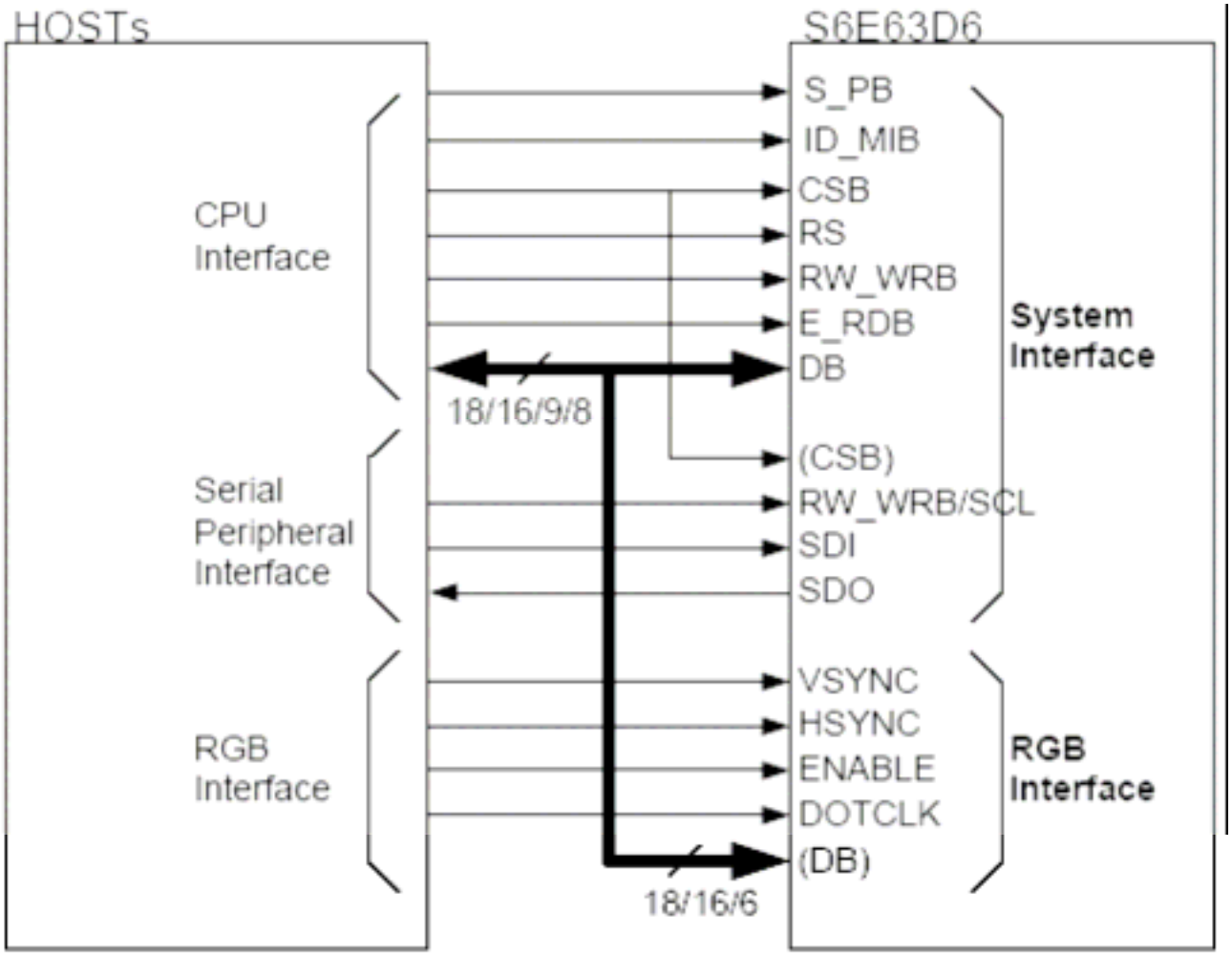
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram



2.2 Interface Pin Description

Pin No.	Symbol	Function
1	AR_VDD	Positive voltage for OLED.
2	AR_VSS	Negative voltage for OLED.
3	VCI	Power supply for analog circuit(2.5v~3.3v).
4	VCI1	A reference voltage for 1st booster.
5	GND	Ground.
6	C12M	External capacitance connect pin between C12M and C12P.
7	C12P	
8	C11M	External capacitance connect pin between C11M and C11P.
9	C11P	
10	VLOUT1	1st booster output pin.
11	C31P	External capacitance connect pin between C31M and C31P.
12	C31M	
13	C32P	External capacitance connect pin between C32M and C32P.
14	C32M	
15	VLOUT3	3st booster output pin.
16	VLOUT2	2nd booster output pin.
17	C21P	External capacitance connect pin between C21M and C21P.
18	C21M	
19	VGS	A reference level for the grayscale voltage generation circuit.
20	IOVCC	I/O power supply.
21	SPB	Select the CPU interface mode.(0=parallel interface,1=serial interface).
22	ID_MIB	Select the CPU type.(0=intel 80x-system,1= intel 68x-system).
23	DB17	Operates liked an 18-bit bi-directional data bus. 18-bits bus I/F: DB17-0
24	DB16	
25	DB15	
26	DB14	

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>27</td><td>DB13</td><td rowspan="12">BI-directional data bus.
When CPU I/F,
18-bit interface:DB 17-0
16-bit interface:DB 17-10,DB 8-1
9-bit interface:DB 8-0
8-bit interface:DB 8-1
When RGB I/F
18-bit interface:DB 17-0
18-bit interface:DB 17-0
16-bit interface:DB 17-10,DB 8-1
6-bit interface:DB 8-3

Fix unused pin to the VSS level</td></tr>
<tr><td>28</td><td>DB12</td></tr>
<tr><td>29</td><td>DB11</td></tr>
<tr><td>30</td><td>DB10</td></tr>
<tr><td>31</td><td>DB9</td></tr>
<tr><td>32</td><td>DB8</td></tr>
<tr><td>33</td><td>DB7</td></tr>
<tr><td>34</td><td>DB6</td></tr>
<tr><td>35</td><td>DB5</td></tr>
<tr><td>36</td><td>DB4</td></tr>
<tr><td>37</td><td>DB3</td></tr>
<tr><td>38</td><td>DB2</td></tr>
<tr><td>39</td><td>DB1</td></tr>
<tr><td>40</td><td>DB0</td></tr>
<tr><td>41</td><td>VSYNC</td><td>Frame-synchronizing signal.
(VSPL=0 Low active,VSPL=1 High active)
Fix this pin at VSS level if the pin is not used.</td></tr>
<tr><td>42</td><td>HSYNC</td><td>Line-synchronizing signal.
(HSPL=0 Low active,HSPL=1 High active)
Fix this pin at VSS level if the pin is not used.</td></tr>
<tr><td>43</td><td>DOTCLK</td><td>Input pin for clock signal of external interface:dot clock.
DPL=0 Display data is fetched at DOTCLK’s rising edge.
DPL=1 Display data is fetched at DOTCLK’s falling edge.
Fix this pin at VSS level if the pin is not used.</td></tr>
<tr><td>44</td><td>Enable</td><td>Data enablesignal pin for RGB interface.

<table>
<tr><th>EPL</th><th>ENABLE</th><th>GRAM write</th><th>GRAM address</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Updated</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>45</td><td>SDI</td><td>For a serial peripheral interface(SPI),input data is fetched at the rising edge of the SCL signal,Fix SDI pin at VSS level if the pin is not used.</td></tr>
<tr><td>46</td><td>SDO</td><td>For a serial peripheral interface(SPI),serves as the serial data output pin(SDO),Successive bits are output at the falling edge of the SCL signal.</td></tr>
<tr><td>47</td><td>CSB</td><td>Chip select signal input pin.
0=driver IC is selected and can be accessed.
1=driver IC is not selected and cannot be accessed.</td></tr>
<tr><td>48</td><td>RW_WRB</td><td>
<table>
<tr><td>Pin function</td><td>CPU type</td><td>Pin description</td></tr>
<tr><td>RW</td><td>68-system</td><td>Read/Write operation selection pin
0=write 1=read</td></tr>
<tr><td>WRB</td><td>80-system</td><td>Write strobe signal.(Input pin)Data is fetched at the rising edge.</td></tr>
<tr><td>SCL</td><td>SPI</td><td>The synchronous clock signal</td></tr>
</table>
</td></tr>
<tr><td>49</td><td>RS</td><td>Register select pin.
0=Index/status. 1=instruction parameter,GRAM data
Must be fixed at VDD3 level when not used.</td></tr>
<tr><td>50</td><td>E_RDB</td><td>
<table>
<tr><td>Pin Function</td><td>CPU type</td><td>Pin description</td></tr>
<tr><td>E</td><td>68-system</td><td>Read/Writeoperation enable pin</td></tr>
<tr><td>RDB</td><td>80-system</td><td>Read strobe signal.
Read out data at the low level</td></tr>
<tr><td colspan="3">When SPI mode is selected,fix this pin at VDD3 levle</td></tr>
</table>
</td></tr>
<tr><td>51</td><td>RESETB</td><td>Reset pin initializes the IC when low.Should be reset after power-on.</td></tr>
<tr><td>52</td><td>MVDD</td><td>Internal power for RAM.Connect a capacitance to gnd.</td></tr>
<tr><td>53</td><td>VREG1OUT</td><td>A reference level for the grayscale voltage.</td></tr>
<tr><td>54</td><td>VCI</td><td>Power supply for analog circuit(2.5v~3.3v).</td></tr>
<tr><td>55</td><td>VGH</td><td>The positive voltage used in the gate driver.</td></tr>
</table>

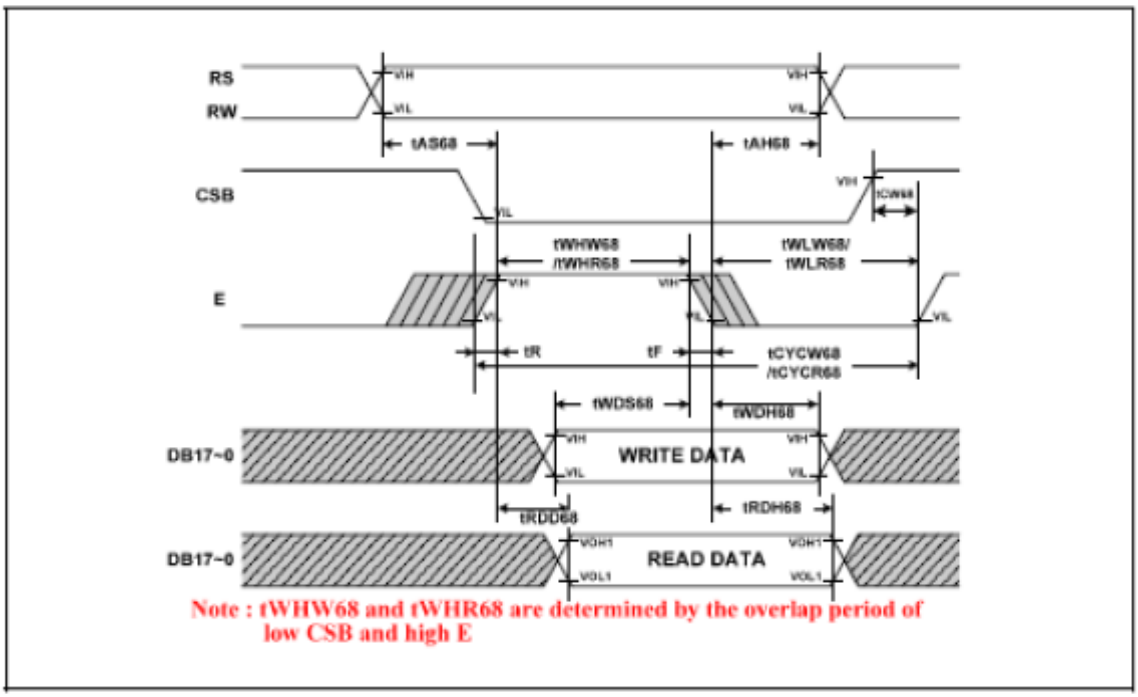
Pin No.	Symbol	Function
56	VGL	The negative voltage used in the gate driver.
57	GND	Ground.
58	TP1	For touch screen.
59	TP2	For touch screen.
60	TP3	For touch screen.
61	TP4	For touch screen.

2.3 Timing Characteristics

CPU Interface M68

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW68	85	-	ns
	Read	tCYCR68	500	-	
Pulse rise / fall time		tR, tF	-	15	
Pulse width low	Write	tWHW68	27.5	-	
	Read	tWHR68	250	-	
Pulse width high	Write	tWLW68	27.5	-	
	Read	tWLR68	250	-	
RS,RW to CSB, E setup time		tAS68	10	-	
RS,RW to CSB, E hold time		tAH68	2	-	
CSB to E time		tCW68	15	-	
Write data setup time		tWDS68	40	-	
Write data hold time		tWDH68	15	-	
Read data delay time		tRDD68	-	200	
Read data hold time		tRDH68	5	-	

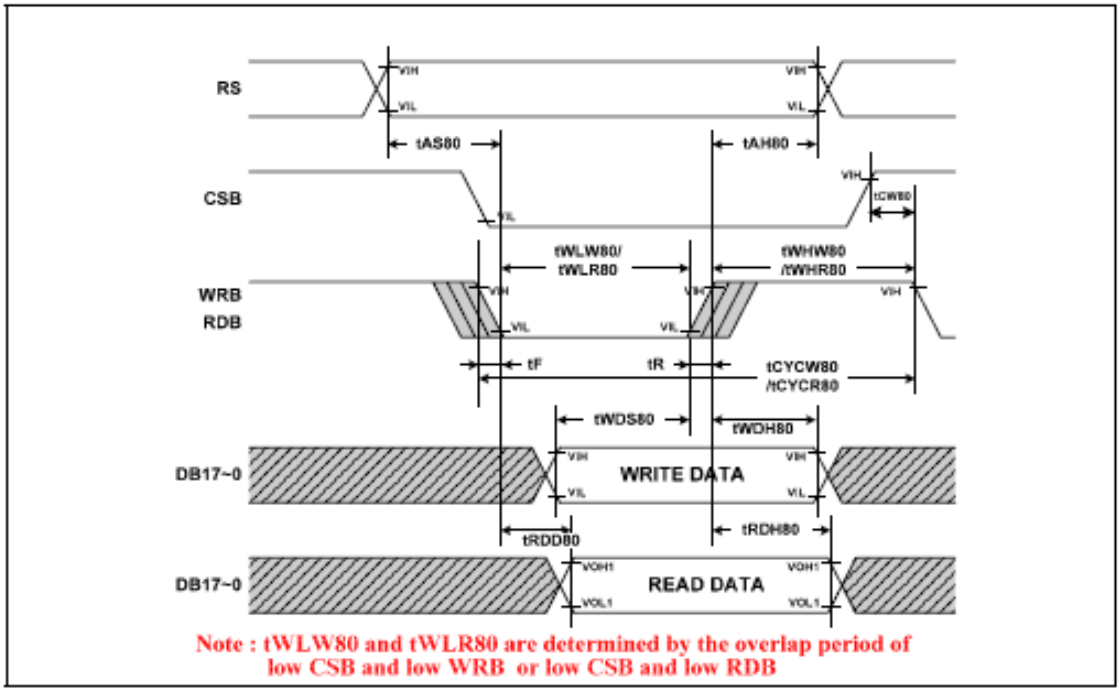


Note : tWHW68 and tWHR68 are determined by the overlap period of low CSB and high E

CPU Interface M80

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW80	85	-	ns
	Read	tCYCR80	500	-	
Pulse rise / fall time		tR, tF	-	15	
Pulse width low	Write	tWLW80	27.5	-	
	Read	tWLR80	250	-	
Pulse width high	Write	tWHW80	27.5	-	
	Read	tWHR80	250	-	
RS to CSB, WRB(RDB) setup time		tAS80	10	-	
RS to CSB, WRB(RDB) hold time		tAH80	2	-	
CSB to WRB(RDB) time		tCW80	15	-	
Write data setup time		tWDS80	40	-	
Write data hold time		tWDH80	15	-	
Read data delay time		tRDD80	-	200	
Read data hold time		tRDH80	5	-	

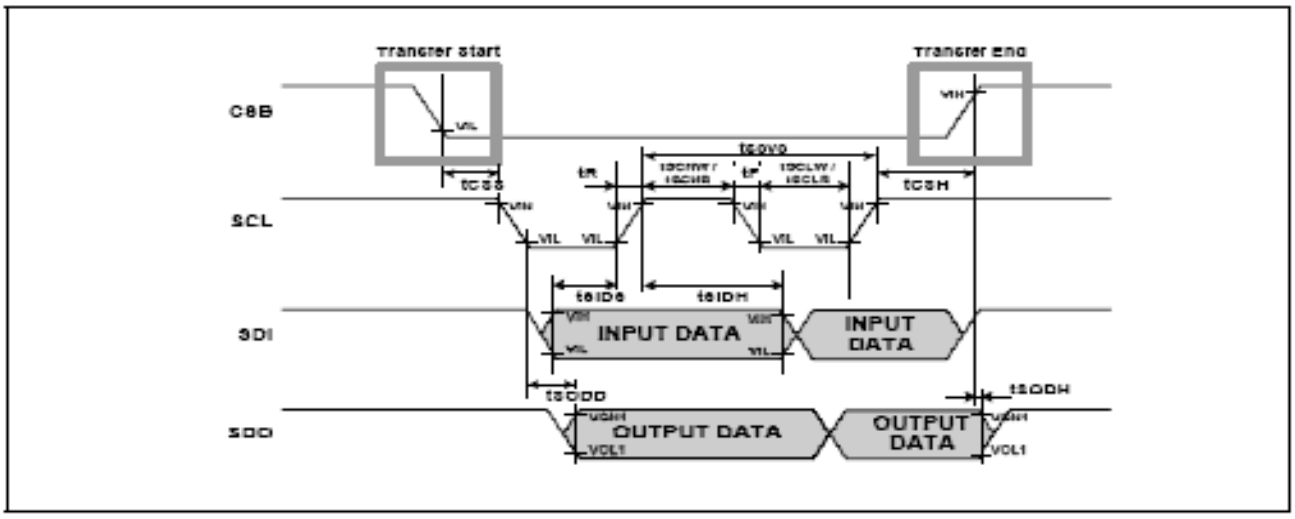


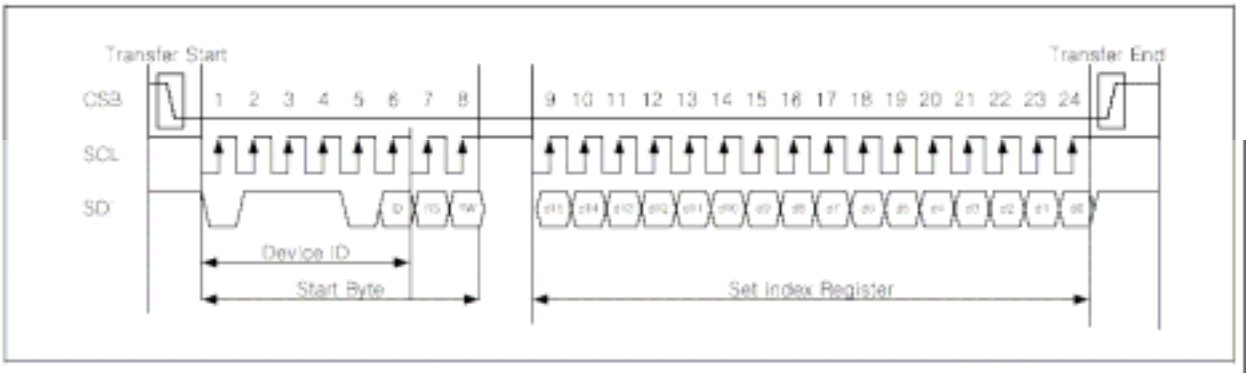
Note : tWLW80 and tWLR80 are determined by the overlap period of low CSB and low WRB or low CSB and low RDB

SPI

Table66: Clock Synchronized Serial Write Mode Characteristics
(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscyc	130	-	ns
Serial clock read cycle time	tscyc	250	-	ns
Serial clock rise / fall time	tR, tF	-	15	ns
Pulse width high for write	tSCHW	50	-	ns
Pulse width high for read	tSCHR	110	-	ns
Pulse width low for write	tSCLW	50	-	ns
Pulse width low for read	tSCLR	110	-	ns
Chip Select setup time	tCSS	20	-	ns
Chip Select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns



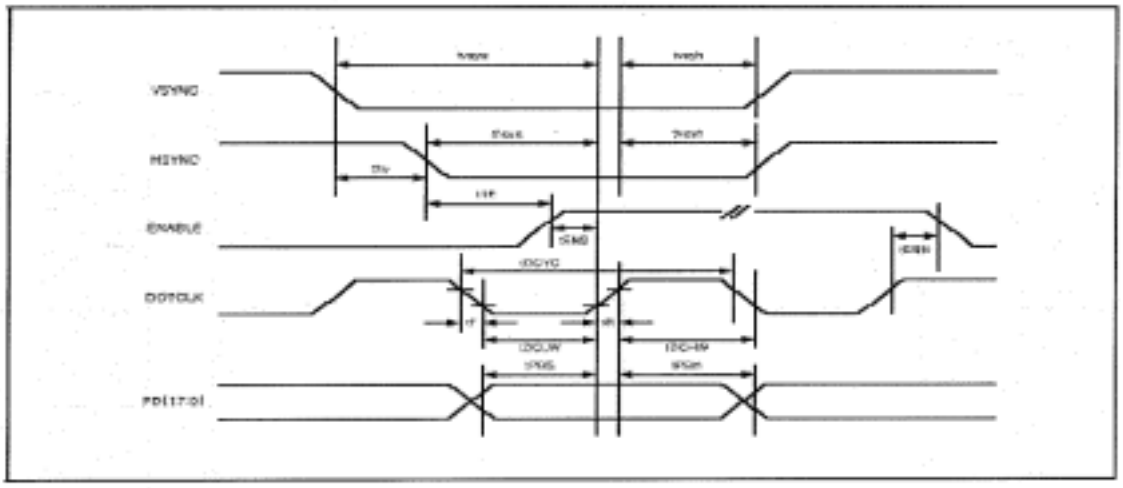


RGB Interface

(VDD = 1.6V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

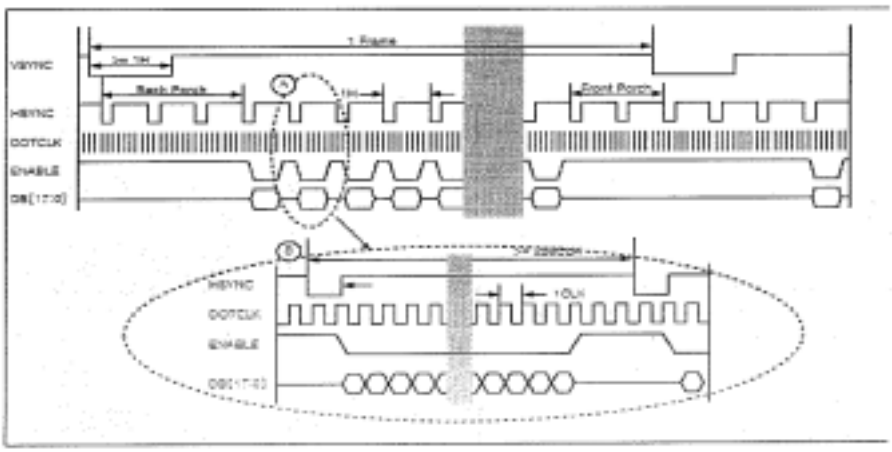
Characteristic	Symbol	18/16bit RGB interface		6bit RGB interface		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	100	-	100	-	ns
DOTCLK rise / fall time	tR, tF	-	15	-	15	
DOTCLK Pulse width high	tDCHW	40	-	40	-	
DOTCLK Pulse width low	tDCLW	40	-	40	-	
Vertical Sync Setup Time	tvsys	30	-	30	-	
Vertical Sync Hold Time	tvsyh	30	-	30	-	
Horizontal Sync Setup Time	thsys	30		30		
Horizontal Sync Hold Time	thsyh	30		30		
ENABLE setup time	tENS	30	-	30	-	
ENABLE hold time	tENH	20	-	20	-	
PD data setup time	tPDS	30	-	30	-	
PD data hold time	tPDH	20	-	20	-	
HSYNC-ENABLE Time	tHE	1	HBP	1	HBP	tDCYC
VSYNC-HSYNC Time	thv	1	175	1	527	

Note : HBP is Horizontal Back-porch.



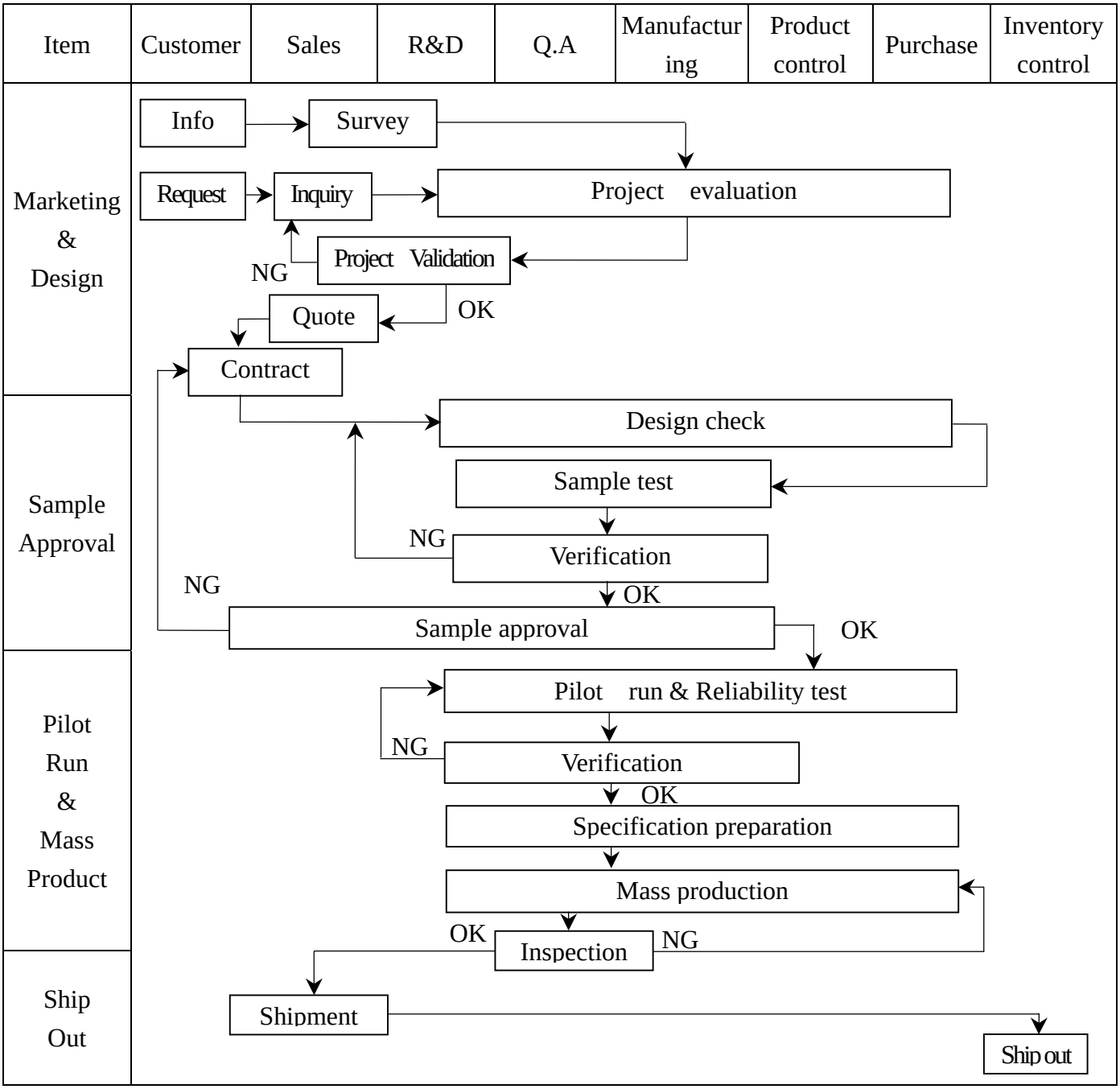
(When VSPL=0, HSPL=0, DPL=0, EPL=1)

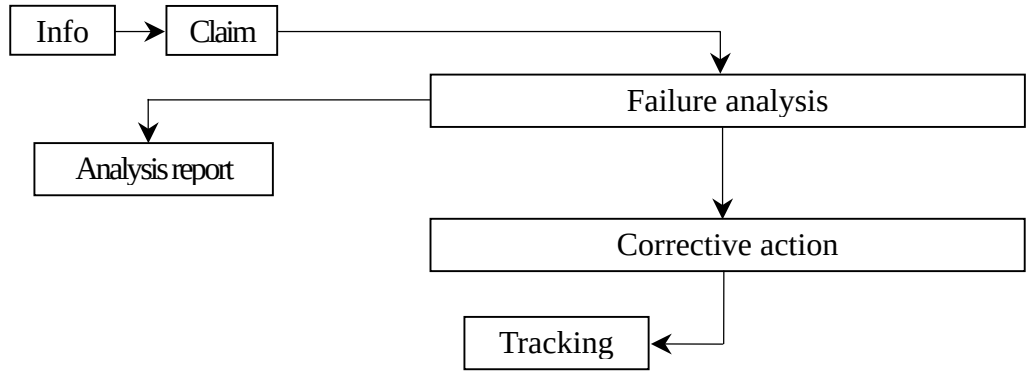
Timing Diagram



3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufacturing	Product control	Purchase	Inventory control
Sales Service								
Q.A Activity	1. ISO 9001 Maintenance Activities 2. Process improvement proposal 3. Equipment calibration 4. Education And Training Activities 5. Standardization Management							

4. RELIABILITY TEST

4.1 Reliability Test Condition

No.	Items	Specification
1	High Temp.Storage	85°C,240hrs
2	Low Temp.Storage	-40°C,240hrs
3	High Temp.Operation	70°C,240hrs
4	Low Temp.Operation	-20°C,240hrs
5	High Temp/Humidity Storage	85°C,85%RH,240hrs
6	High Temp/Humidity Operation	65°C,90%RH,240hrs
7	Thermal shock	-40°C~85°C (-40°C /30min:transit /3min;85°C /30min;transit /3min)1 cycle:66min,100 cycles
8	Peel strength	>500g/cm(Speed~50mm/min)
9	Vibration	Frequency:5~50HZ,0.5G
		Scan rate:1 oct/min
		Time:2hrs/axis
		Test axis:X,Y,Z
10	Drop	Hight:120cm
		Sequence:1angle、3edges and 6 faces
		Cycles:1
11	ESD	Air discharge model,+/-8kV,10 times

Evaluation Criteria
_No damage to glass or encapsulation
_No drastic change to display
_Pixel/Line defects:no increased
_Luminance:Within+/-50% of initial value
_Uniformity:(Max-Min)/Min<15%
_Current consumption:within +/-50%of initial value

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.

5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

5.2.1 Avoid any strong mechanical shock which can break the glass.

5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.

5.2.3 Do not remove the panel or frame from the module.

5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully, do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)

5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.

5.2.6 Do not touch the display area with bare hands , this will stain the display area.

5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

5.2.8 To control temperature and time of soldering is 320 ± 10°C and 3-5 sec.

5.2.9 To avoid liquid (include organic solvent) stained on LCM

5.3 STORAGE

5.3.1 Store the panel or module in a dark place where the temperature is 25°C ± 5°C and the humidity is below 65% RH.

5.3.2 Do not place the module near organics solvents or corrosive gases.

5.3.3 Do not crush , shake , or jolt the module.

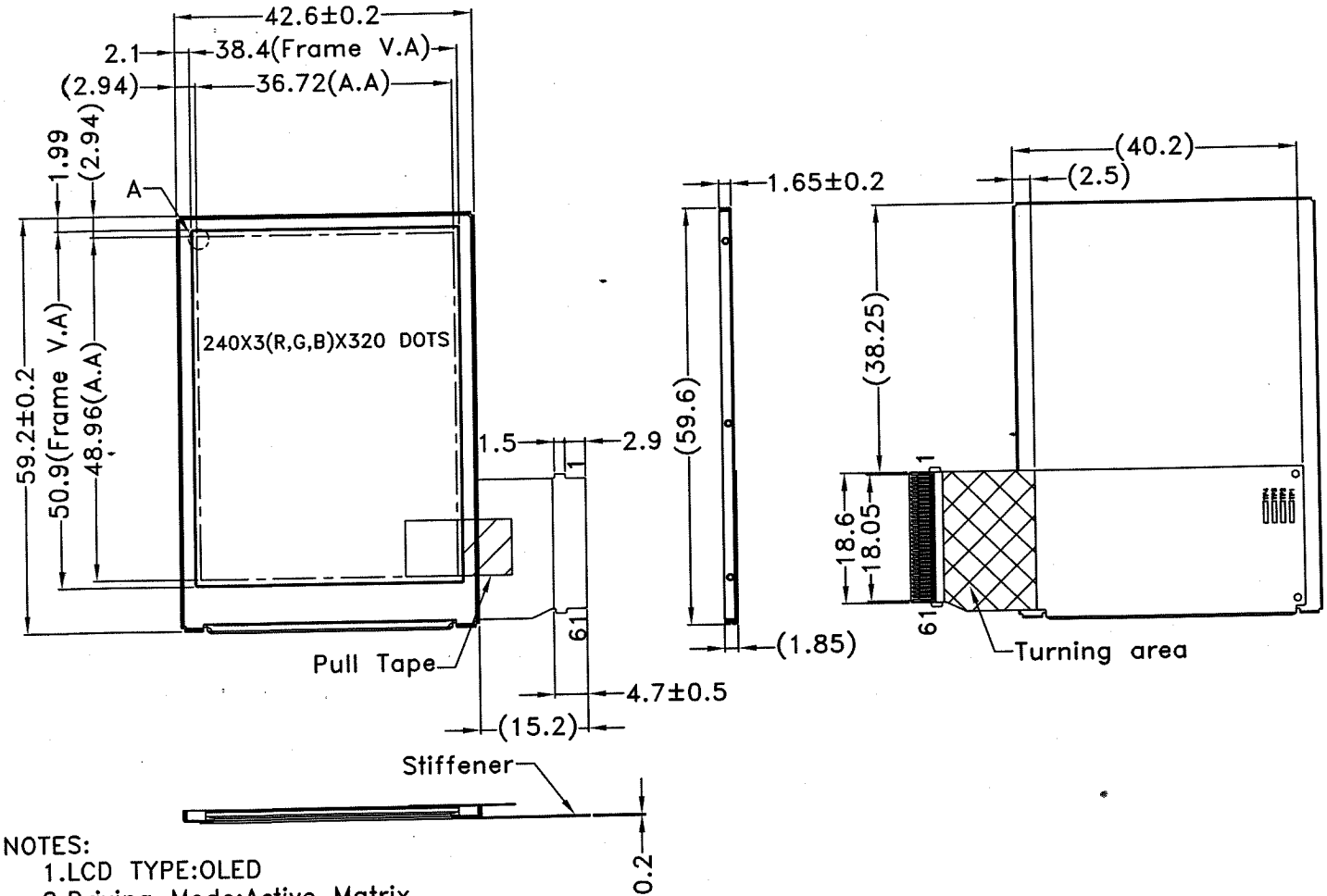
5.4 TERMS OF WARRANTY

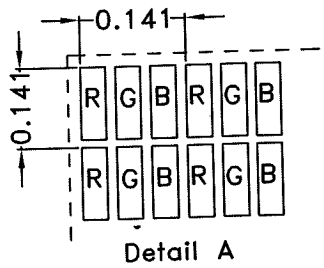
Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.

6. PACKING Specification

* See Appendix





1	AR_VDD	22	ID_MIB	42	HSYNC
2	AR_VSS	23	DB17	43	DOTCLK
3	VCI	24	DB16	44	ENABLE
4	VCI1	25	DB15	45	SDI
5	GND	26	DB14	46	SDO
6	C12M	27	DB13	47	CSB
7	C12P	28	DB12	48	RW_WRB
8	C11M	29	DB11	49	RS
9	C11P	30	DB10	50	E_RDB
10	VLOUT1	31	DB9	51	RESETB
11	C31P	32	DB8	52	MVDD
12	C31M	33	DB7	53	VREG1OUT
13	C32P	34	DB6	54	VCI
14	C32M	35	DB5	55	VGH
15	VLOUT3	36	DB4	56	VGL
16	VLOUT2	37	DB3	57	GND
17	C21P	38	DB2	58	TP1
18	C21M	39	DB1	59	TP2
19	VGS	40	DB0	60	TP3
20	IOVCC	41	VSYNC	61	TP4
21	SPB				

NOTES:
1. LCD TYPE:OLED
2. Driving Mode:Active Matrix
3. Color Mode:Full Color(262K color)
4. Top: −20~70°C Tst:−40~85°C
5. The tolerance unless classified ±0.3mm
6. Diagonal Size:2.4"(Inch)
7. Driver IC:S6E63D6,COG Assembly
8. Connector : HIROSE FH23-61S-0.3SHW(05)

REV	DESCRIPTION	DATE
A	Modify FPC outline	JUN/11/07'

久正光電股份有限公司
POWERTIP TECHNOLOGY CORPORATION

					APPROVED	CHECKER	DRAWN
SCALE:1/1	UNIT:mm	PAGE:1/1			研發 2007-6-22 黃秋源	研發 2007-6-11 李美倫	研發 96.6.11 黃茹珮
圖面名稱	PPT9999-A003-06-Q						
圖面編號	PPT-06002-007	EDI	A				

黃俊清

2-060-01-01

LCM Model	PPT9999-A003-06-Q
版次Ver.A	

LCM包裝規格書
LCM Packaging Specifications

Approve	Check	Contact
研發 2007-6-22. 黃秋源	研發 2007-6-11. 李美倫	研發 96.6.11 黃茹珮

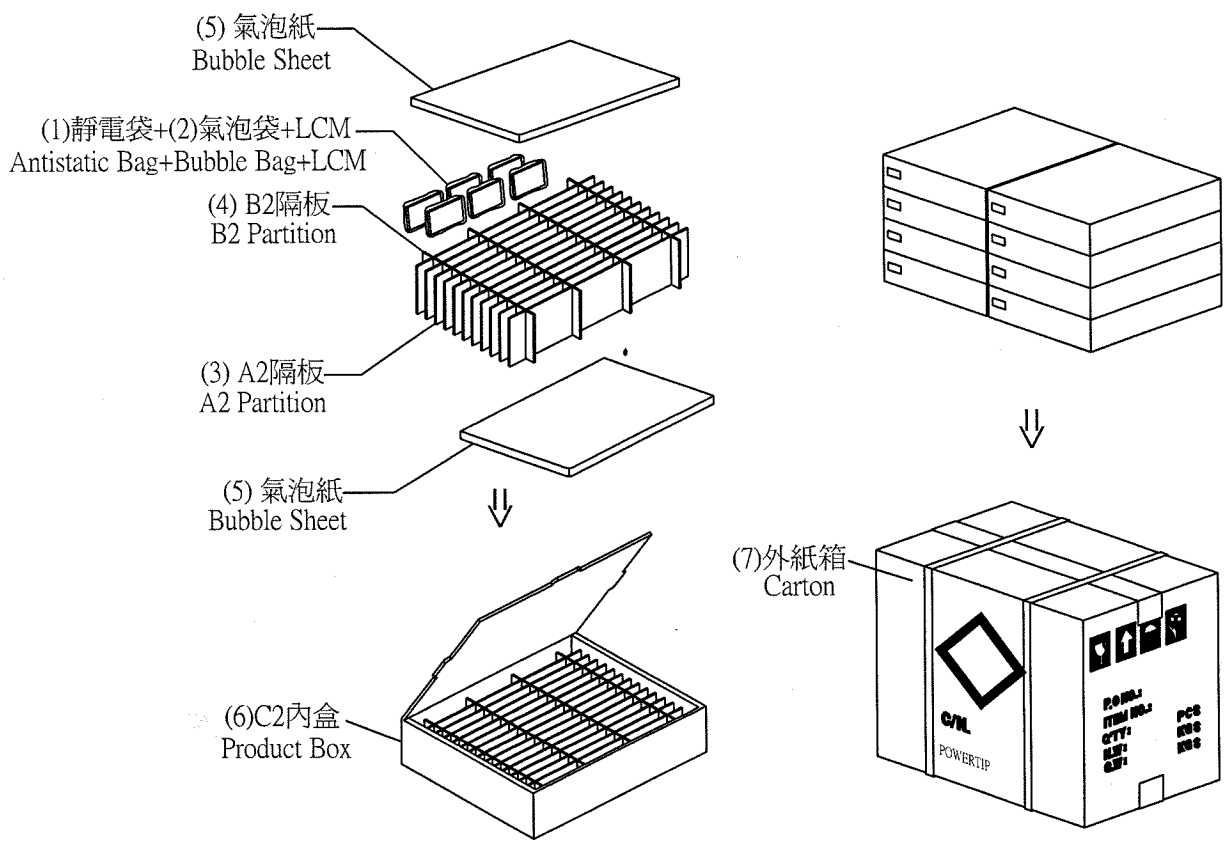
1.包裝材料規格表 (Packaging Material) : (per carton)

No.	Item	Model	Dimensions (mm)	Quantity
1	成品 (LCM)	PPT9999-A003-06-Q	50.0 X 68.0	288
2	靜電袋(1)Antistatic Bag	BAG100100ARABA	100 X 100	288
3	氣泡袋(2)Bubble Bag	BAG100080BWABA	1000 X 80	288
4	A2隔板(3)A2 Partition	BX29300070BMBA	293 X 70 X 2.5	88
5	B2隔板(4)B2 Partition	BX24500070BLBA	245 X 70 X 2.5	32
6	氣泡紙(5)Bubble Sheet	BAG280240BWABA	280 X 240	16
7	C2內盒(6)Product Box	BX31025580AABA	310 X 255 X 80	8
8	外紙箱(7)Carton	BX52732536CCBA	527 X 325 X 360	1
9				

2.單箱數量規格表 (Packaging Specifications and Quantity) :

(1)Quantity Of Spacer : A2隔板 X 11 , B2隔板 X 4

(2)Total LCM quantity in carton : quantity per box 36 x no of boxes 8 = 288



特 記 事 項 (REMARK)

1. Label Specifications :

MODEL:
LOT NO:
QUANTITY:
CHECK:

POWERTIP TECH. CORP.