R1LV0816ABG -5SI, 7SI

8Mb Advanced LPSRAM (512k word x 16bit)

REJ03C0393-0100
Rev.1.00
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Description

The R1LV0816ABG is a family of low voltage 8-Mbit static RAMs organized as 524,288-words by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1LV0816ABG is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The R1LV0816ABG is packaged in a 48balls fine pitch ball grid array [f-BGA / 7.5 mm×8.5mm with the ball-pitch of 0.75mm and 6x8 array]. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

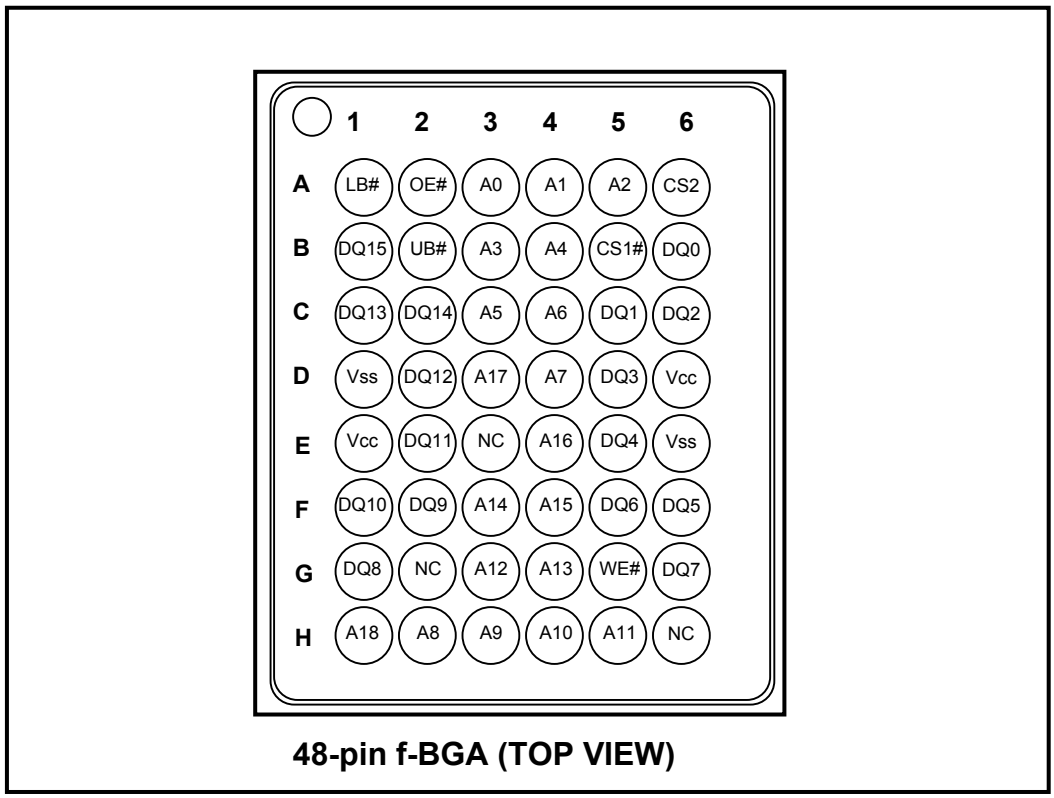
Features

- Single 2.4-3.6V power supply
- Small stand-by current: 1.2µA (Vcc=3.0V, typ.)
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Operation temperature: -40 ~ +85°C

Ordering information

Type No.	Power supply	Access time	Temperature Range	Package
R1LV0816ABG-5SI	2.7V to 3.6V	55 ns	-40 ~ +85°C	48-ball fBGA with 0.75mm ball pitch PTBG0048HB-A(48FHH)
	2.4V to 2.7V	70 ns		
R1LV0816ABG-7SI	2.4V to 3.6V	70 ns		

Pin Arrangement

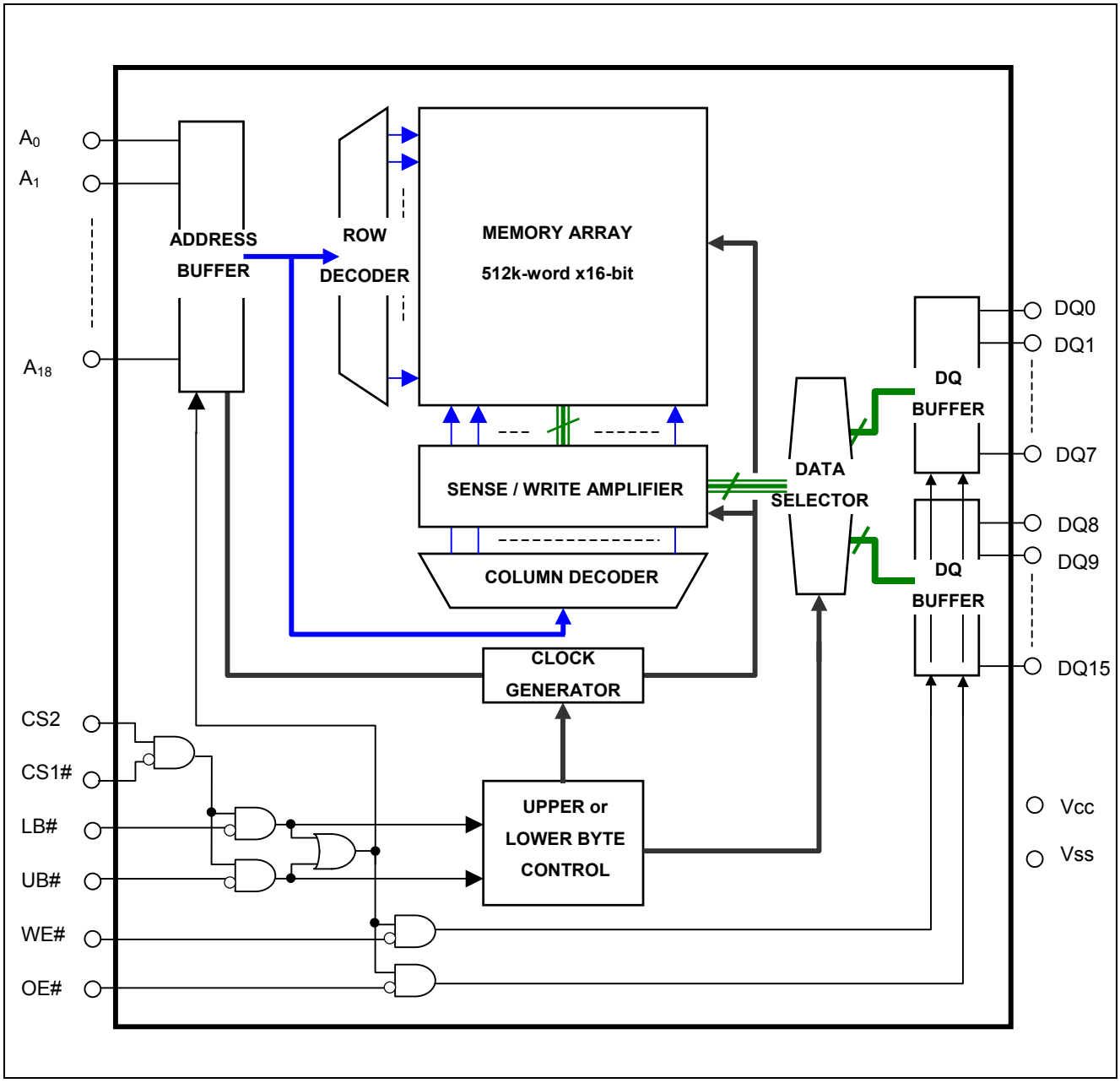


48-pin f-BGA (TOP VIEW)

Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A18	Address input
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
LB#	Lower byte enable
UB#	Upper byte enable
NC	Non connection

Block Diagram



Operation Table

CS1#	CS2	LB#	UB#	WE#	OE#	DQ0~7	DQ8~15	Operation
H	X	X	X	X	X	High-Z	High-Z	Stand-by
X	L	X	X	X	X	High-Z	High-Z	Stand-by
X	X	H	H	X	X	High-Z	High-Z	Stand-by
L	H	L	H	L	X	Din	High-Z	Write in lower byte
L	H	L	H	H	L	Dout	High-Z	Read in lower byte
L	H	L	H	H	H	High-Z	High-Z	Output disable
L	H	H	L	L	X	High-Z	Din	Write in upper byte
L	H	H	L	H	L	High-Z	Dout	Read in upper byte
L	H	H	L	H	H	High-Z	High-Z	Output disable
L	H	L	L	L	X	Din	Din	Word write
L	H	L	L	H	L	Dout	Dout	Word read
L	H	L	L	H	H	High-Z	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Terminal voltage on any pin relative to Vss	V_T	-0.5[*1] to Vcc+0.3[*2]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. -3.0V in case of AC (Pulse width ≤30ns)
2. Maximum voltage is +4.6V

Recommend Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	Vcc	2.4	3.0	3.6	V	-	
	Vss	0	0	0	V	-	
Input high voltage	V_{IH}	2.0	-	Vcc+0.2	V	Vcc=2.4V to 2.7V	
		2.2	-	Vcc+0.2	V	Vcc=2.7V to 3.6V	
Input low voltage	V_{IL}	-0.2	-	0.4	V	Vcc=2.4V to 2.7V	1
		-0.2	-	0.6	V	Vcc=2.7V to 3.6V	1
Ambient temperature range	Ta	-40	-	+85	°C	-	

Note 1. -3.0V in case of AC (Pulse width ≤30ns)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	$\lvert I_{LI} \rvert$	-	-	1	µA	Vin = Vss to Vcc	
Output leakage current	$\lvert I_{LO} \rvert$	-	-	1	µA	CS1# =V_{IH} or CS2 =V_{IL} or OE# =V_{IH} or WE# =V_{IL} or LB# = UB# =V_{IH}, VI/O =Vss to Vcc	
Average operating current	I_{CC1}	-	20*1	35	mA	Min. cycle, duty =100%, II/O = 0mA CS1# =V_{IL}, CS2 =V_{IH}, Others = V_{IH}/V_{IL}	
	I_{CC2}	-	2*1	5	mA	Cycle =1□s, duty =100%, II/O = 0mA CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V	
Standby current	I_{SB}	-	0.1*1	0.3	mA	CS2 =V_{IL}	
Standby current	I_{SB1}	-	1.2*1	4	µA	~+25°C	Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		-	3*2	6	µA	~+40°C	
		-	-	15	µA	~+70°C	
		-	-	20	µA	~+85°C	
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -1mA Vcc≥2.7V	
	V_{OH2}	2.0	-	-	V	I_{OH} = -0.1mA	
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA Vcc≥2.7V	
	V_{OL2}	-	-	0.4	V	I_{OL} = 0.1mA	

Note 1.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+25°C), and not 100% tested.
2.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+40°C), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

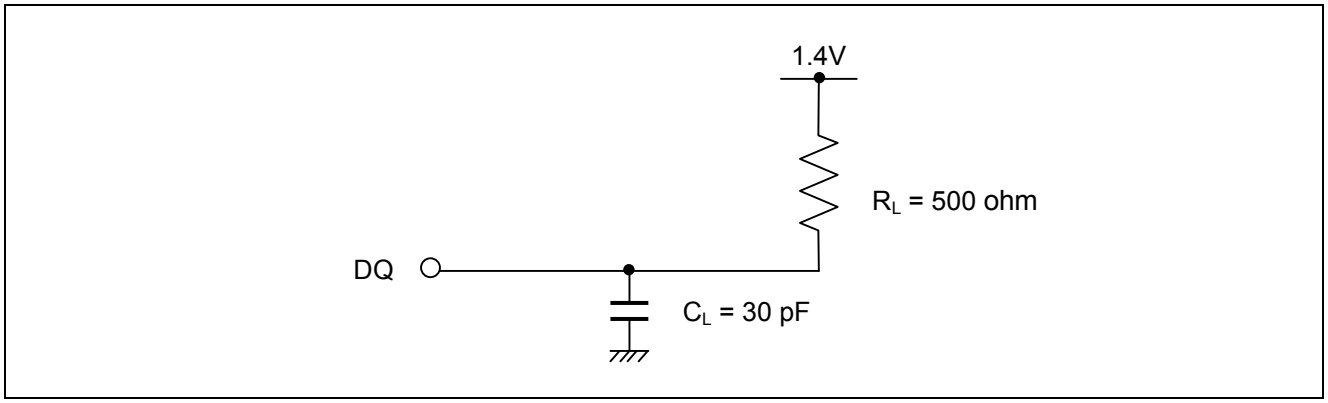
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	10	pF	Vin =0V	1
Input / output capacitance	$C_{I/O}$	-	-	10	pF	$V_{I/O}$ =0V	1

Note 1.Typical parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.4V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels: VIL = 0.4V, VIH = 2.4V (Vcc = 2.7V ~ 3.6 V)
  VIL = 0.4V, VIH = 2.2V (Vcc = 2.4V ~ 2.7 V)
- Input rise and fall times: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read cycle

Parameter	Symbol	R1LV0816ABG-5SI (Note 0)		R1LV0816ABG-7SI		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	55	-	70	-	ns	
Address access time	t_{AA}	-	55	-	70	ns	
Chip select access time	t_{ACS1}	-	55	-	70	ns	
	t_{ACS2}	-	55	-	70	ns	
Output enable to output valid	t_{OE}	-	30	-	35	ns	
Output hold from address change	t_{OH}	10	-	10	-	ns	
LB#, UB# access time	t_{BA}	-	55	-	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	-	10	-	ns	2,3
	t_{CLZ2}	10	-	10	-	ns	2,3
LB#, UB# enable to low-Z	t_{BLZ}	5	-	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1,2,3
	t_{CHZ2}	0	20	0	25	ns	1,2,3
LB#, UB# disable to high-Z	t_{BHZ}	0	20	0	25	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2,3

Write Cycle

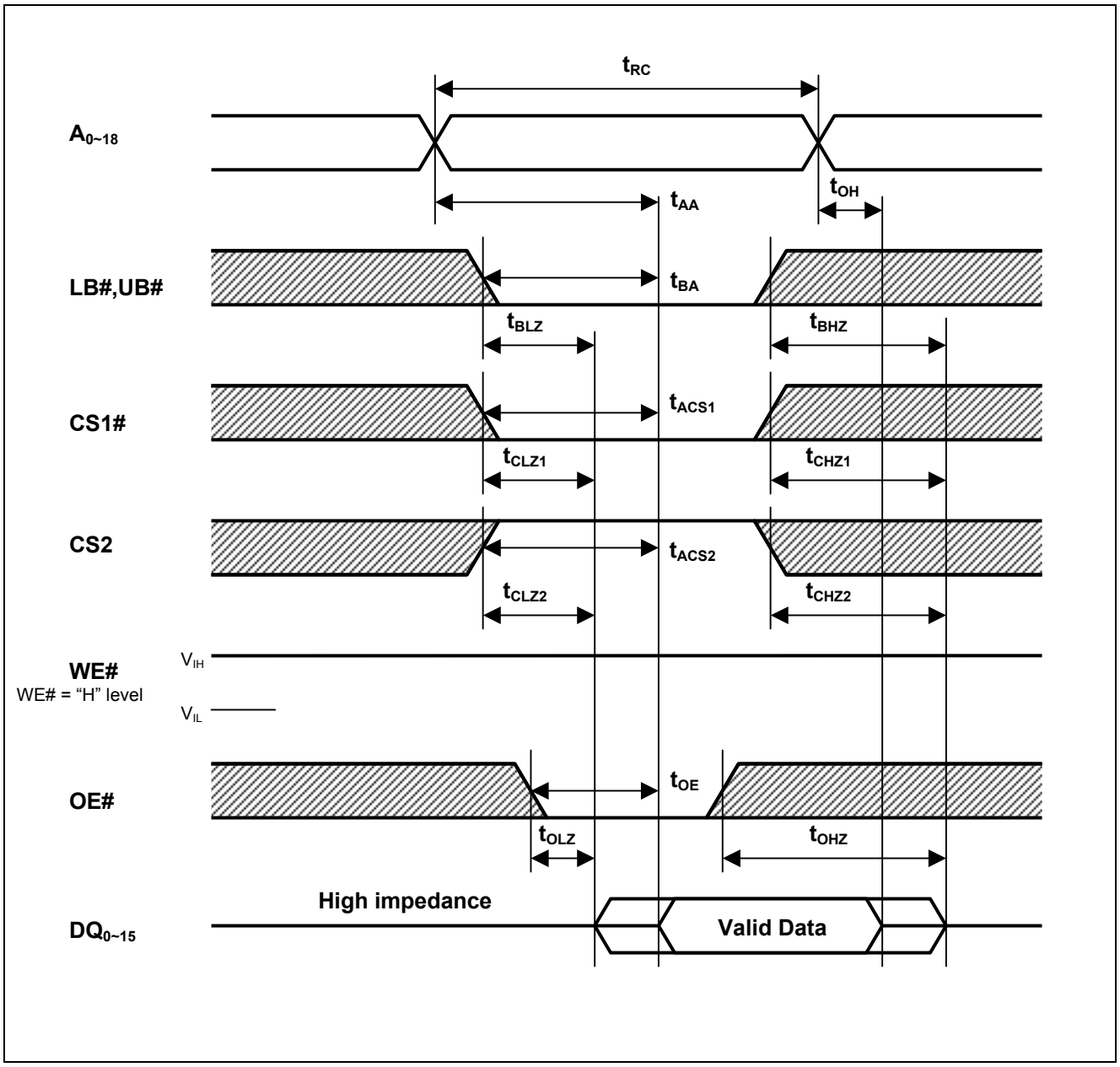
Parameter	Symbol	R1LV0816ABG-5SI (Note 0)		R1LV0816ABG-7SI		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	55	-	70	-	ns	
Address valid to end of write	t_{AW}	50	-	65	-	ns	
Chip select to end of write	t_{CW}	50	-	65	-	ns	5
Write pulse width	t_{WP}	40	-	55	-	ns	4
LB#, UB# valid to end of write	t_{BW}	50	-	65	-	ns	
Address setup time	t_{AS}	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	35	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	ns	
Output enable from end of write	t_{OW}	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1,2

Note 0. If Vcc is 2.4-2.7V, parameters of R1LV0816ABG-7SI (70ns) are applied.

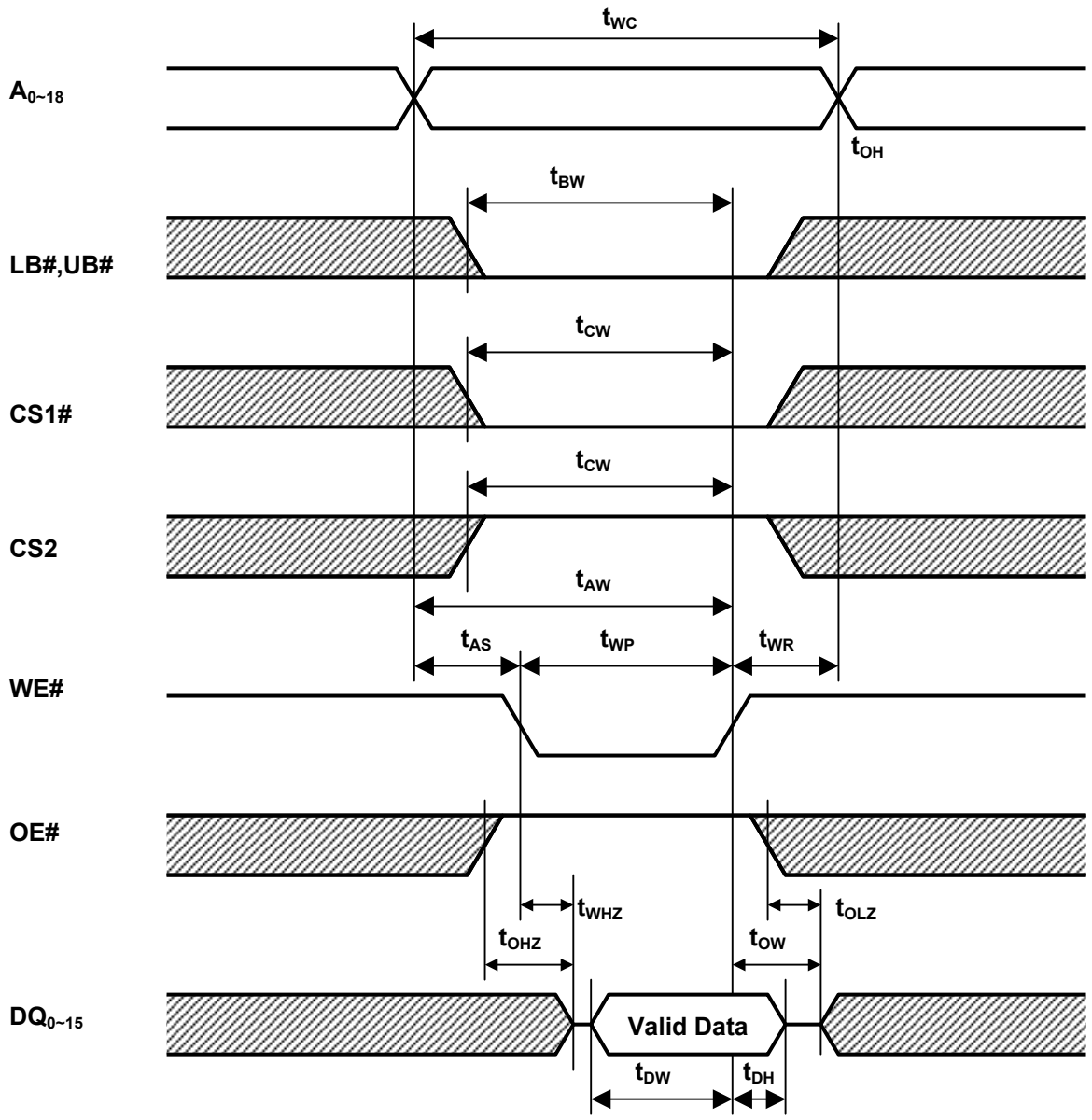
1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. Typical parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or low UB#.
   A write begins at the latest transitions among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low.
   A write ends at the earliest transitions among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle

Timing Waveforms

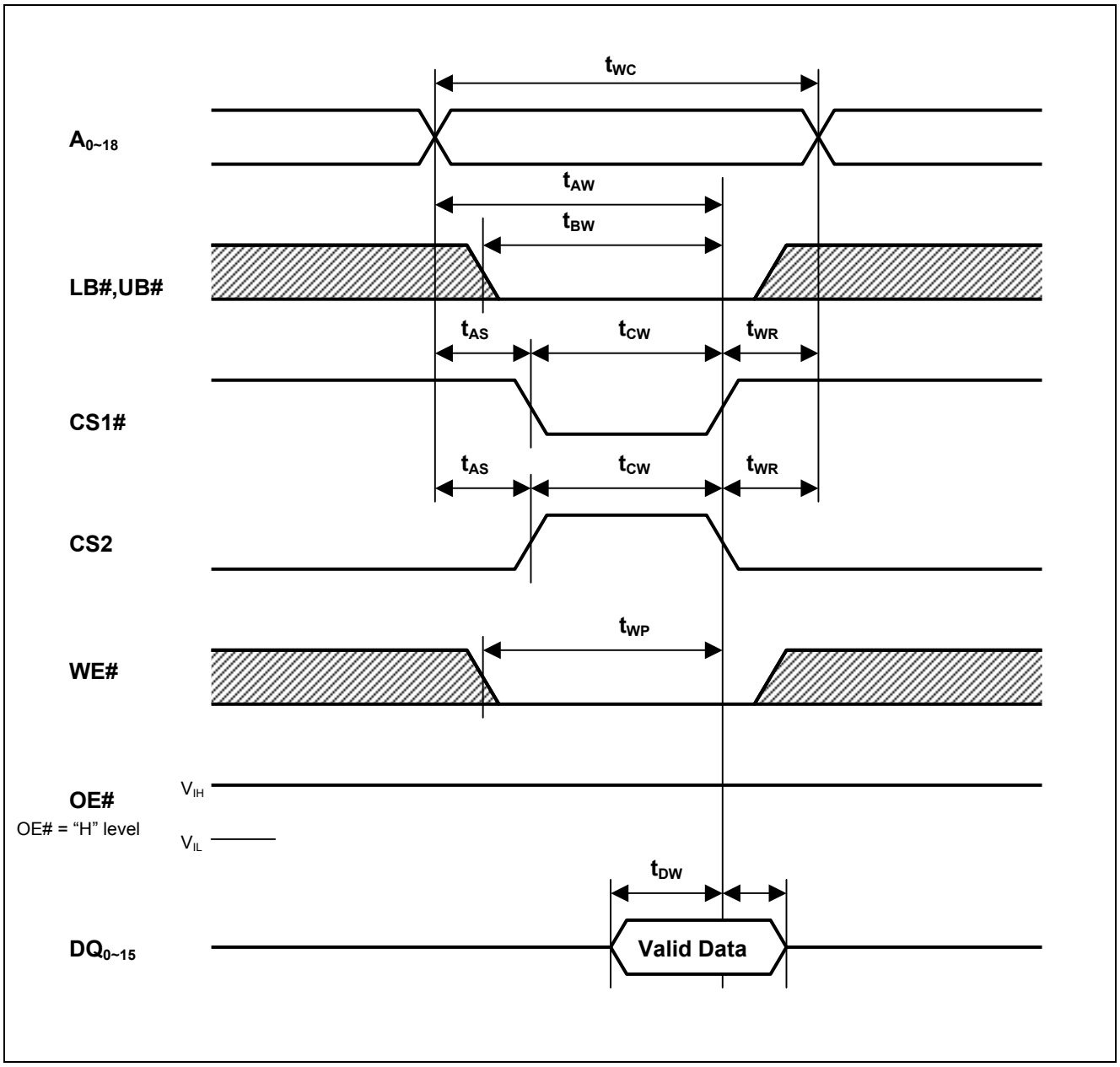
Read Cycle



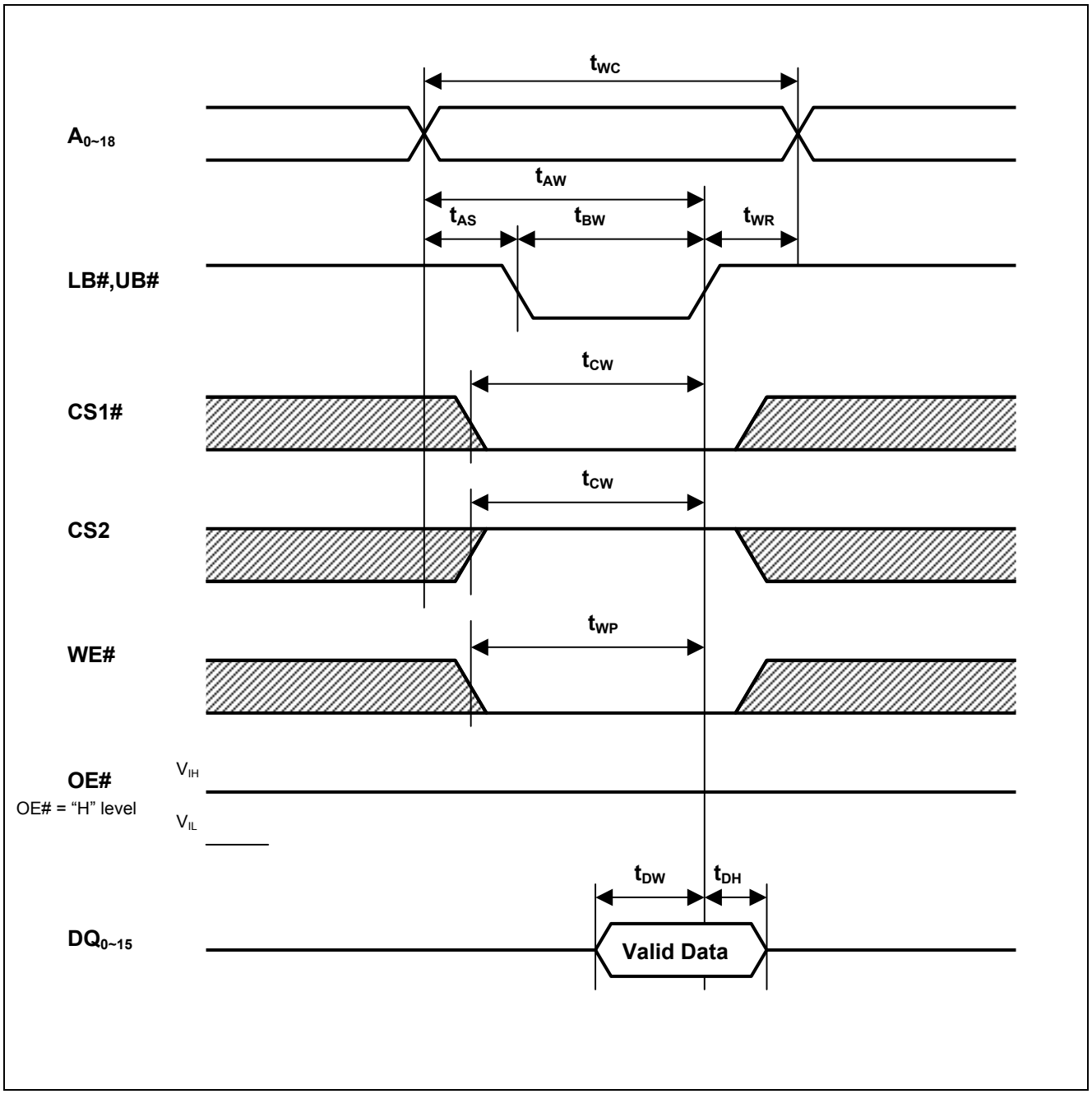
Write Cycle (1) (WE# CLOCK)



Write Cycle (2)　(CS1#, CS2 CLOCK)



Write Cycle (3) (LB#, UB# CLOCK)



Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[*3]	
V_{CC} for data retention	V_{DR}	1.5	-	3.6	V	Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V	
Data retention current	I_{CCDR}	-	1.2[*1]	4	µA	~+25°C	Vcc=3.0V, Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		-	3[*2]	6	µA	~+40°C	
		-	-	15	µA	~+70°C	
		-	-	20	µA	~+85°C	
Chip select to data retention time	t_{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t_R	5	-	-	ms		

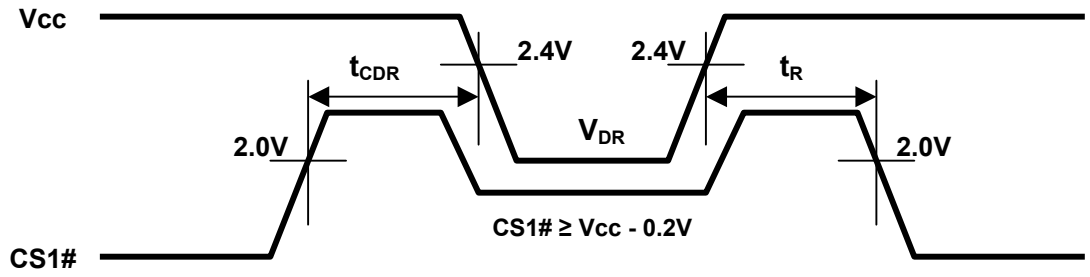
Note 1.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+25°C), and not 100% tested.

2.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+40°C), and not 100% tested.

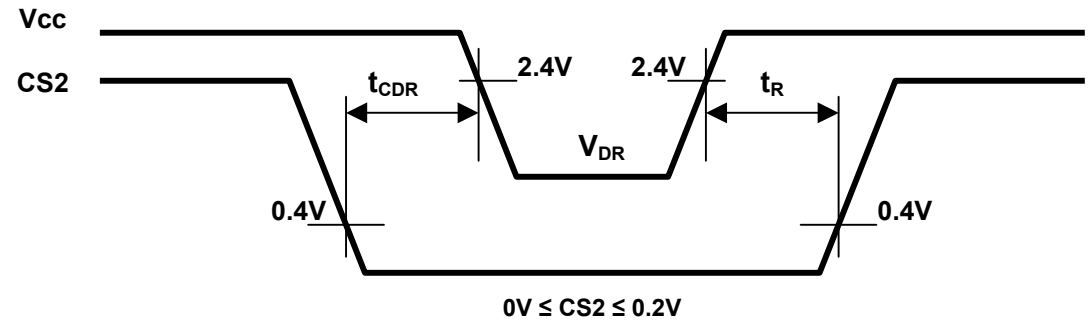
3.CS2 controls address buffer, WE# buffer, CS1# Buffer, OE# buffer, LB#, UB# buffer and Din buffer.
If CS2 controls data retention mode, Vin levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V .
The other inputs levels (address, WE#, OE#, CS1#, LB#, UB#, DQ) can be in the high impedance state.

Data Retention Timing Waveforms

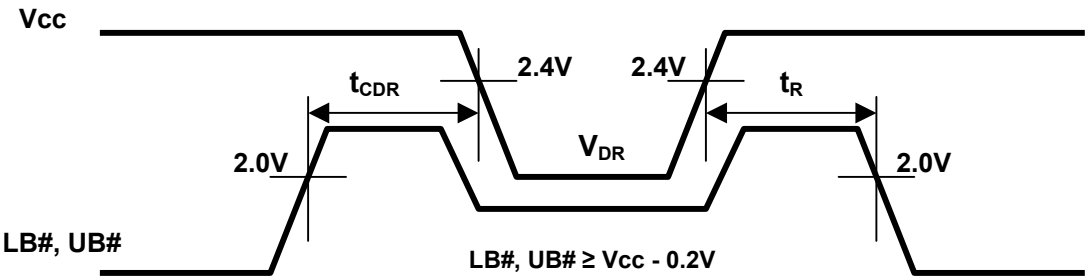
(1) CS1# controlled



(2) CS2 controlled



(3) LB#, UB# controlled



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