



STP80NF10FP

N-channel 100V - 0.012Ω - 38A - TO-220FP
Low gate charge STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D ⁽¹⁾
STP80NF10FP	100V	<0.015Ω	38A

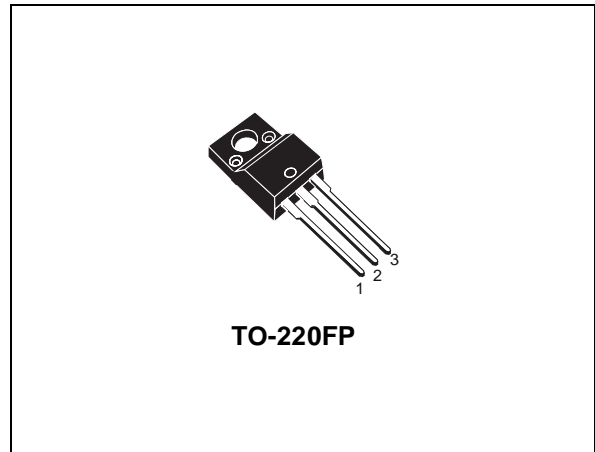
- Exceptional dv/dt capability
- 100% Avalanche tested
- Application oriented characterization

Description

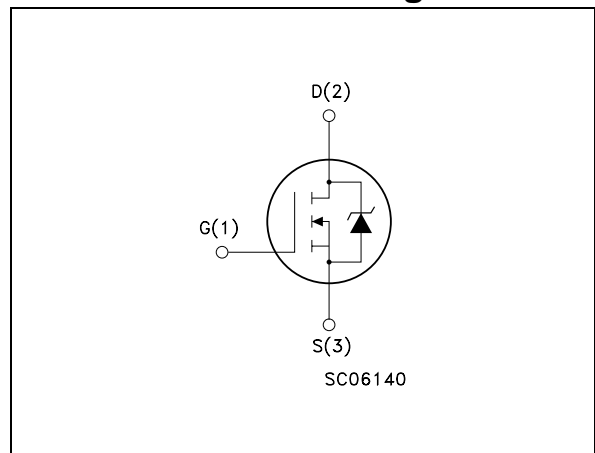
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP80NF10FP	P80NF10FP	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	38	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	27	A
$I_{DM}^{(2)}$	Drain current (pulsed)	152	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	45	W
	Derating factor	0.3	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	9	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	350	mJ
V_{ISO}	Insulation withstand voltage (DC)	2500	V
T_{stg} T_j	Storage temperature Operating junction temperature	-55 to 175	$^\circ\text{C}$

1. Limited by Package
2. Pulse width limited by safe operating area
3. $I_{SD} < 80\text{A}$, $di/dt < 300\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$
4. Starting $T_j = 25^\circ\text{C}$, $I_D = 80\text{A}$, $V_{DD} = 50\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case Max	3.33	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 40A$		0.012	0.015	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25V, I_D = 40 A$		80		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		4300 600 230		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80V, I_D = 80A,$ $V_{GS} = 10V$		140 23 51	189	nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50V, I_D = 40A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 14)		40		ns
t_r	Rise time			145		ns
$t_{d(off)}$	Turn-off-delay time			134		ns
t_f	Fall time			115		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				152	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 80A, V_{DD} = 50V$ $di/dt = 100A/\mu s, T_j = 150^\circ C$		155		ns
Q_{rr}	Reverse recovery charge			850		nC
I_{RRM}	Reverse recovery current			11		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

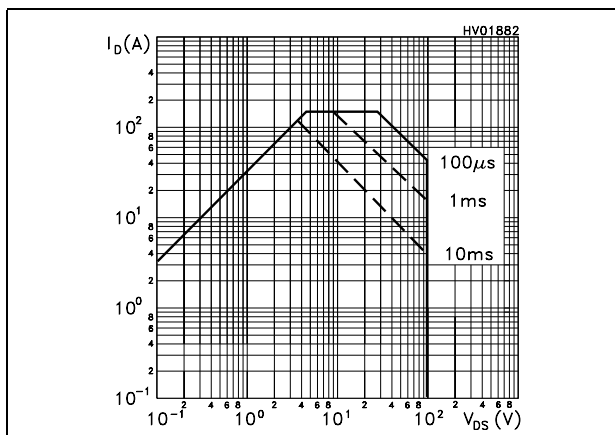


Figure 2. Thermal impedance

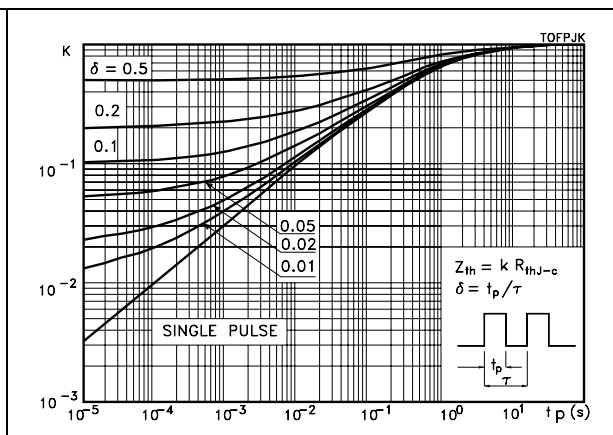


Figure 3. Output characteristics

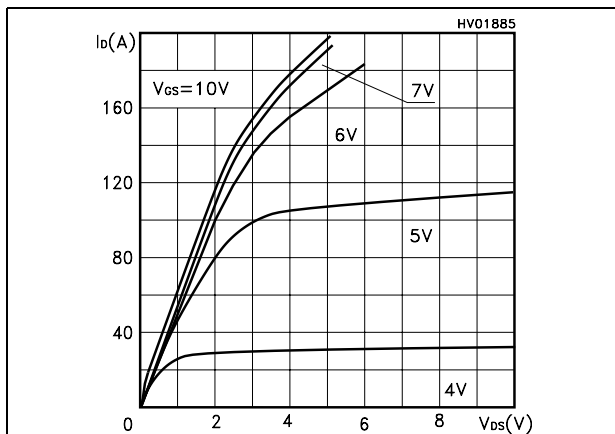


Figure 4. Transfer characteristics

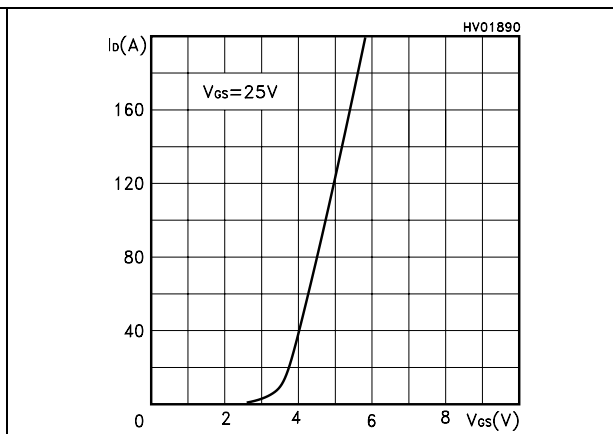


Figure 5. Transconductance

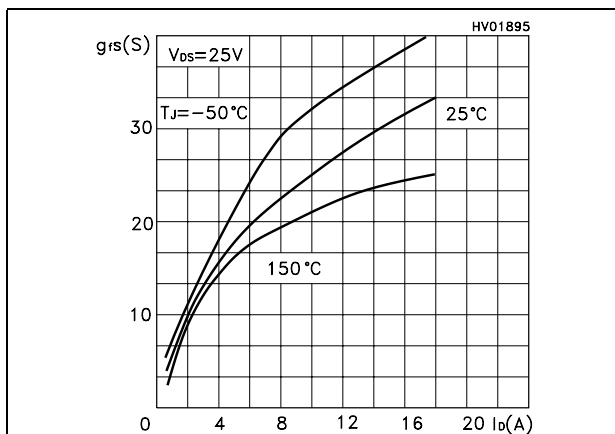


Figure 6. Static drain-source on resistance

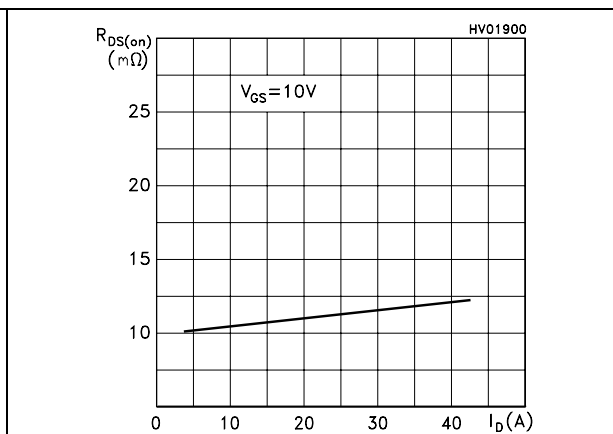


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

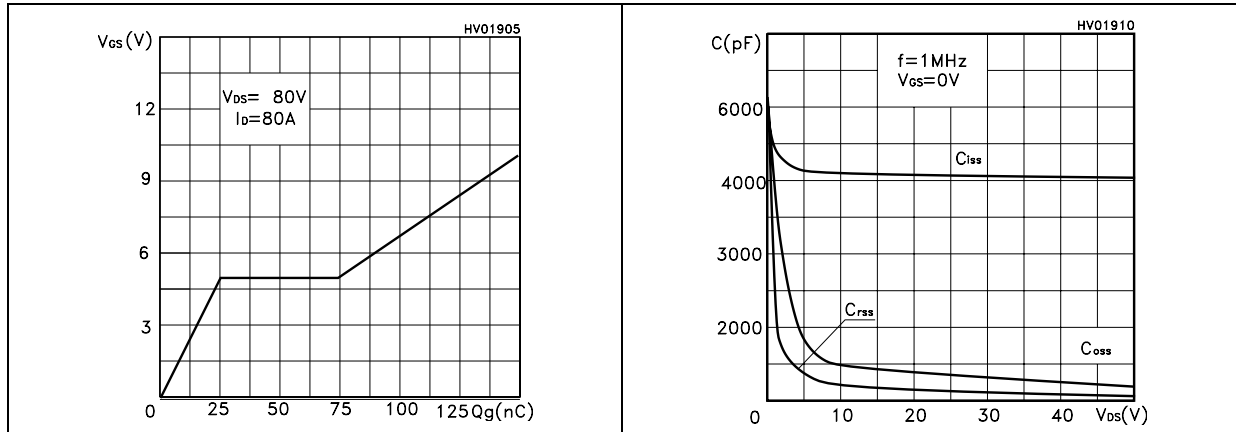


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

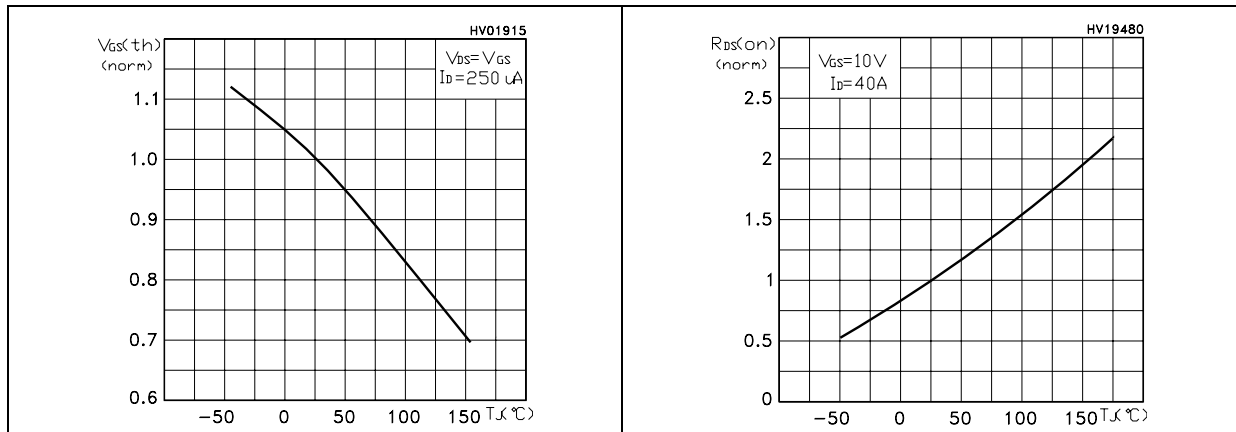
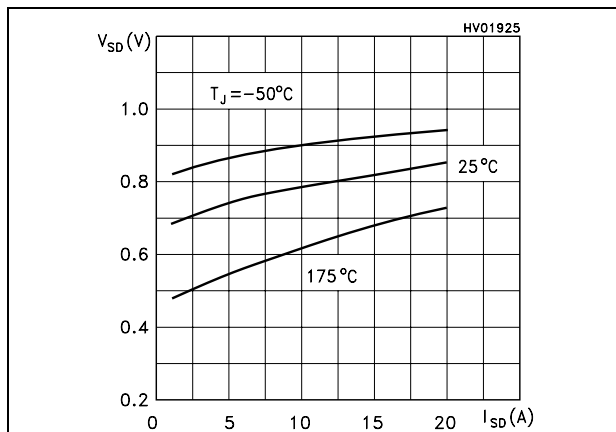


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

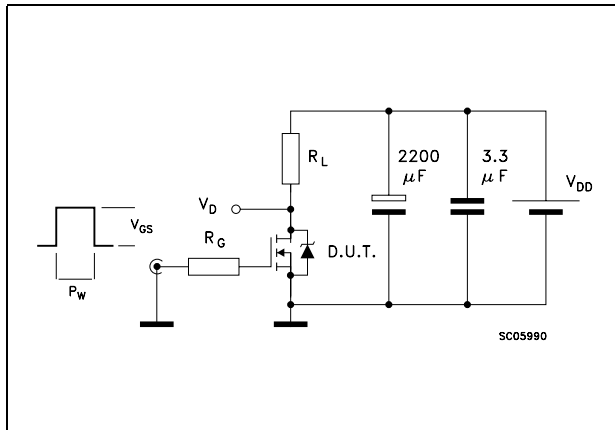


Figure 13. Gate charge test circuit

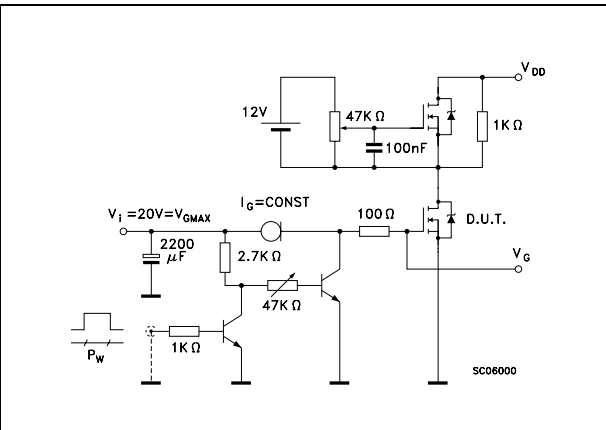


Figure 14. Test circuit for inductive load switching and diode recovery times

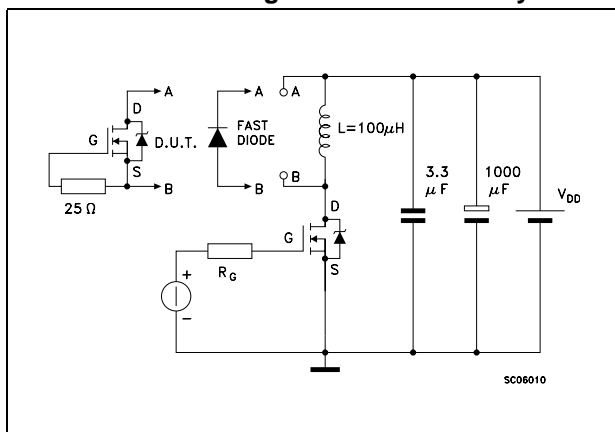


Figure 15. Unclamped inductive load test circuit

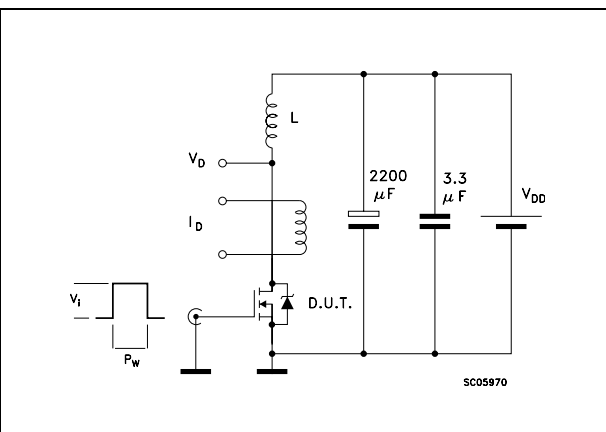


Figure 16. Unclamped inductive waveform

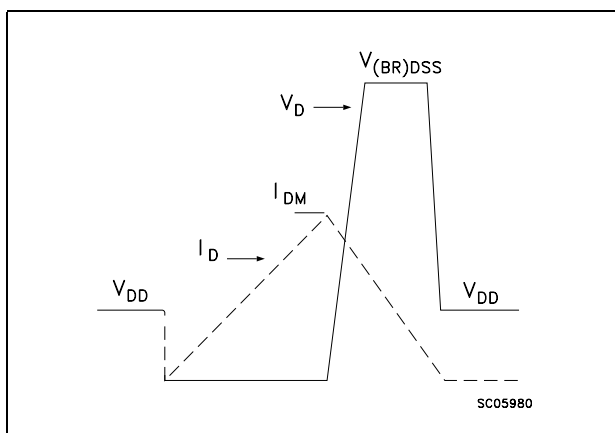
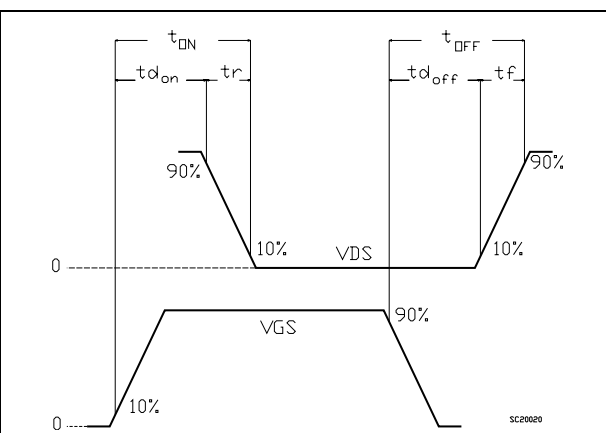


Figure 17. Switching time waveform

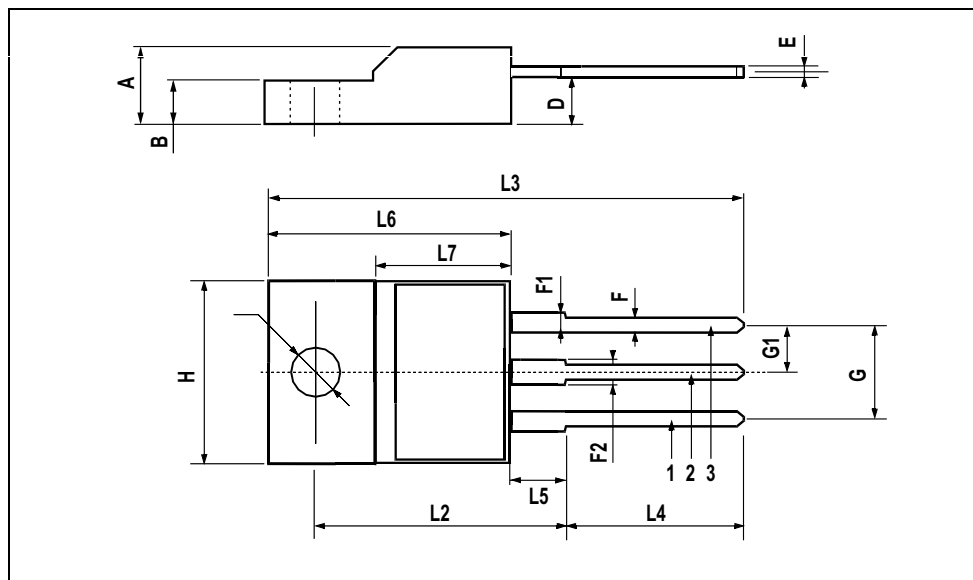


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



5 Revision history

Table 7. Revision history

Date	Revision	Changes
11-Apr-2006	1	First Release

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