



STS15N4LLF3

N-channel 40V - 0.0042Ω - 15A - SO-8
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STS15N4LLF3	40V	<0.005Ω	15A

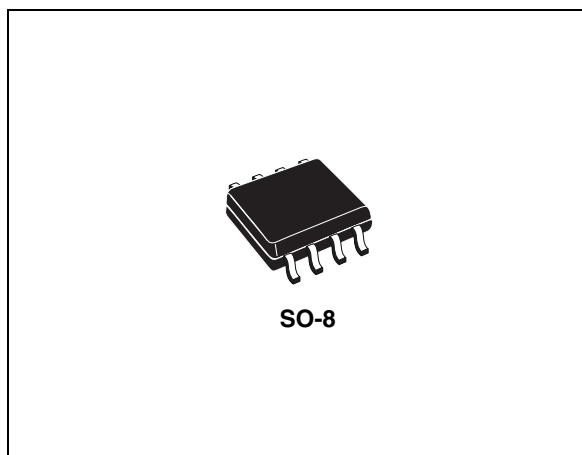
- Optimal R_{DS(on)} × Q_g trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced

Description

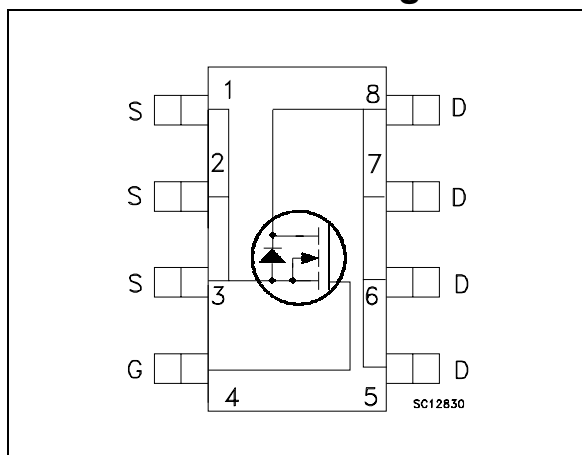
This N-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronic unique “Single Feature Size™” strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STS15N4LLF3	15N4LL-	SO-8	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	40	V
V_{GS}	Gate-source voltage	± 16	V
$V_{GS}^{(1)}$	Gate- source voltage	± 18	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	15	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	9.3	A
$I_{DM}^{(2)}$	Drain current (pulsed)	60	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.7	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	2	J

1. Guaranteed for test time $\leq 15\text{ms}$
2. Pulse width limited by $T_{j\text{max}}$
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 7.5\text{A}$, $V_{DD} = 25\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{\text{thj-pcb}}^{(1)}$	Thermal resistance junction-pcb max	47	$^\circ\text{C/W}$
T_l	Maximum lead temperature for soldering	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

1. When mounted of FR-4 board with 1 inch² pad, 2oz of Cu and $t < 10\text{sec}$

2 Electrical characteristics

($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating} @ 125^\circ\text{C}$			10 100	μA μA
I_{GSS}	Gate body leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 7.5\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 7.5\text{A}$		0.0042 0.005	0.005 0.007	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		2530 574 29		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20\text{V}$, $I_D = 15\text{A}$ $V_{GS} = 4.5\text{V}$ (see Figure 13)		21.5 6.9 8.2	28	nC nC nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20mV open drain	1	3	5	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 20\text{V}$, $I_D = 7.5\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 15)		17 25		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 20\text{V}$, $I_D = 7.5\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 15)		62 9		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 15A, V_{DD} = 30V,$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ (see Figure 14)		43		ns
Q_{rr}	Reverse recovery charge			64		nC
I_{RRM}	Reverse recovery current			3		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

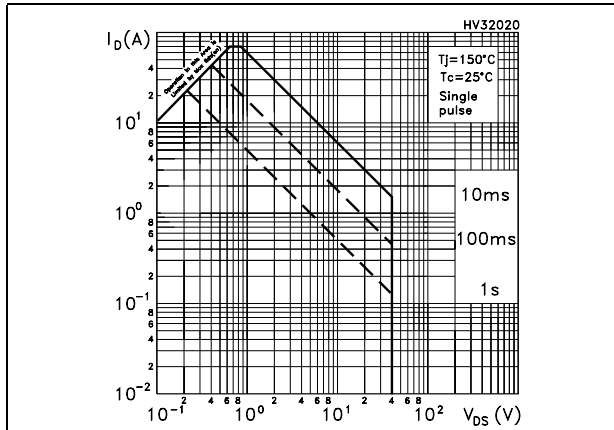


Figure 2. Thermal impedance

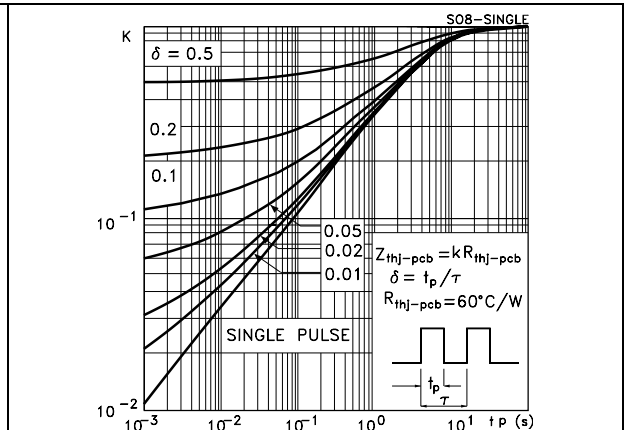


Figure 3. Output characteristics

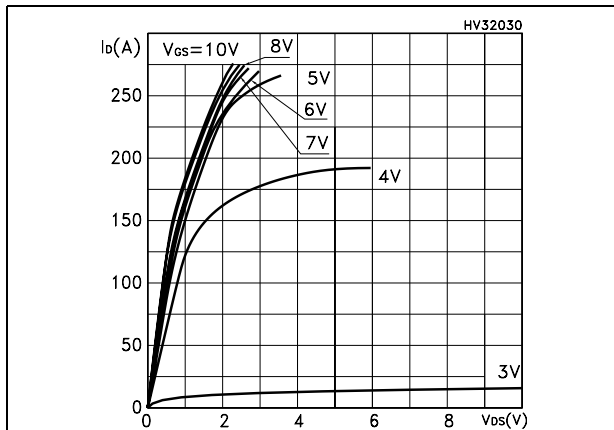


Figure 4. Transfer characteristics

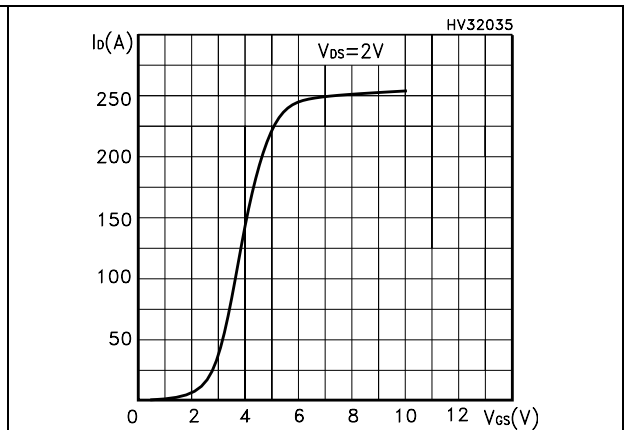


Figure 5. Normalized B_{VDSS} vs temperature

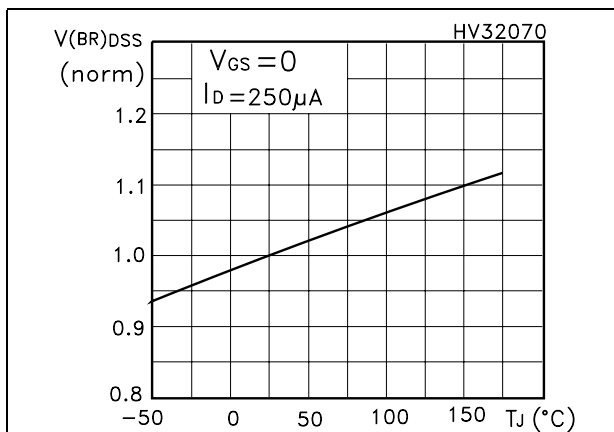


Figure 6. Static drain-source on resistance

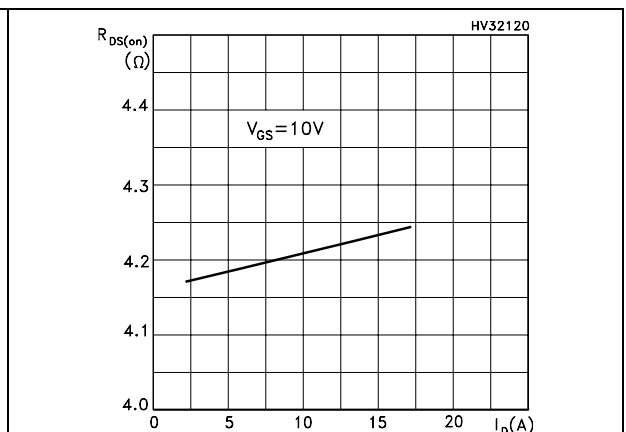


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

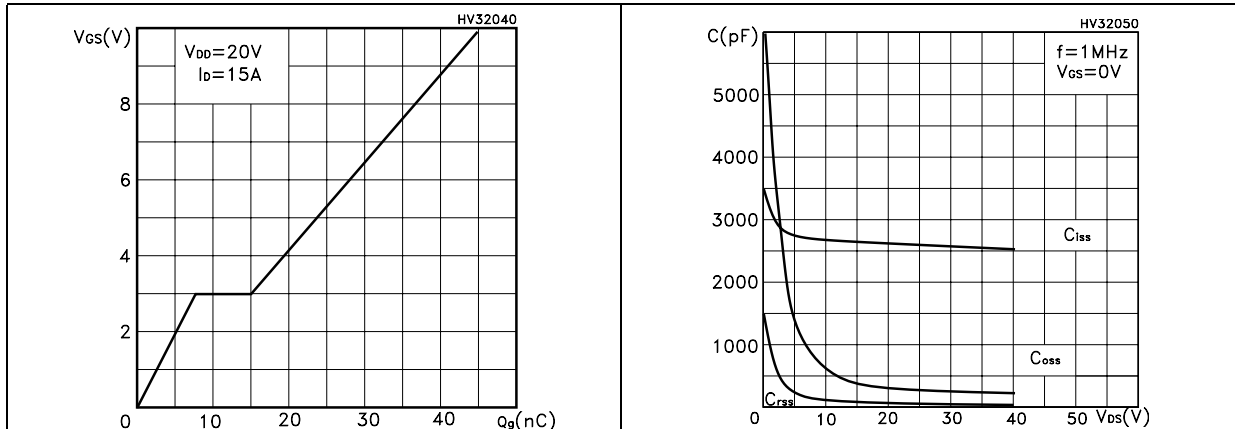


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

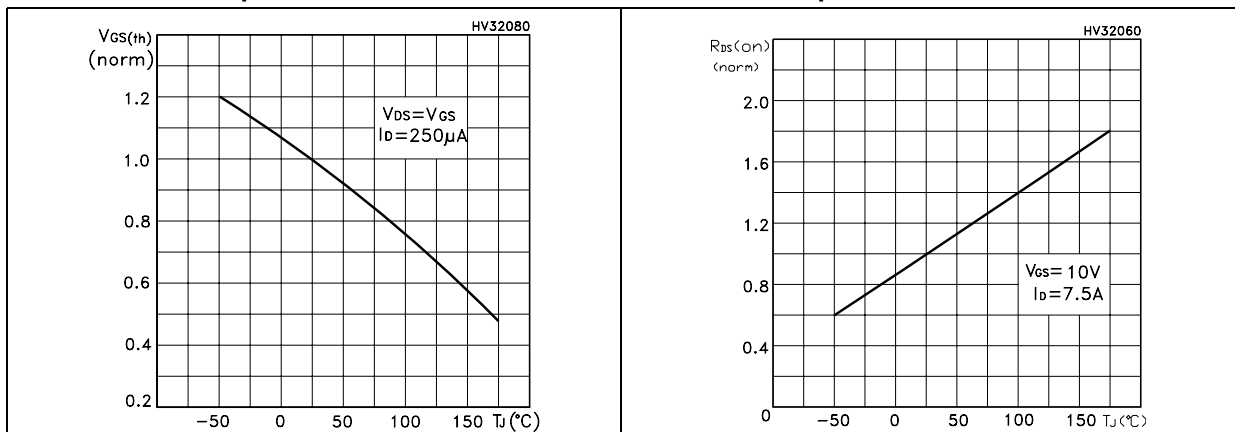
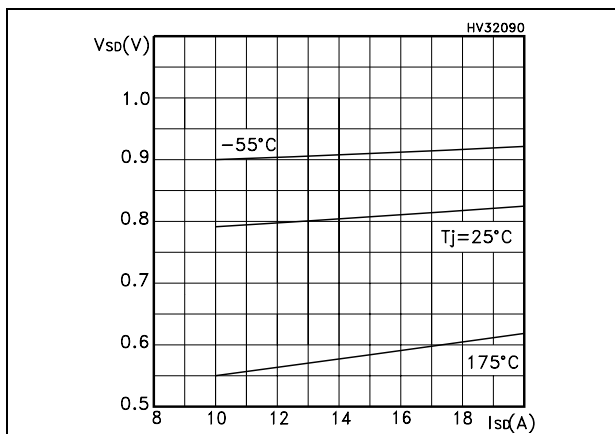


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit



Figure 14. Test circuit for inductive load switching and diode recovery times



Figure 15. Unclamped Inductive load test circuit



Figure 16. Unclamped inductive waveform



Figure 17. Switching time waveform

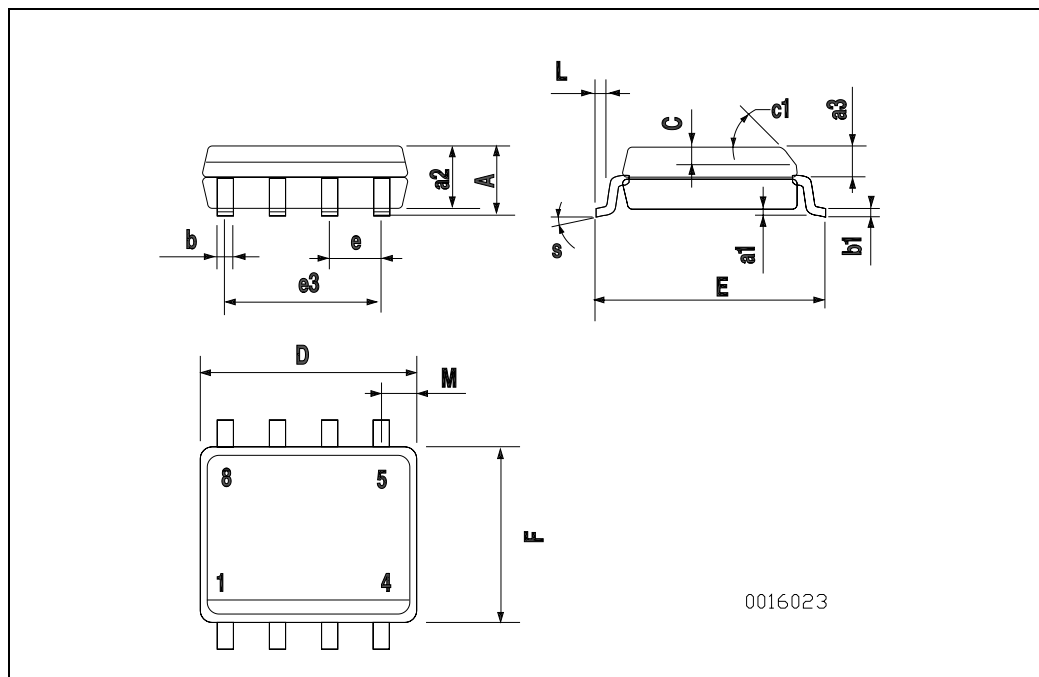


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Jun-2006	1	First release
22-Nov-2006	2	Corrected part number

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