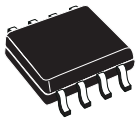
STS4C3F30L

N-channel 30V - 0.044Ω - 5A - SO-8
STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS4C3F30L (n-ch)	30V	<0.055Ω	5A
STS4C3F30L (p-ch)	30V	<0.165Ω	3A

- Low threshold drive
- Standard outline for easy automated surface mount assembly

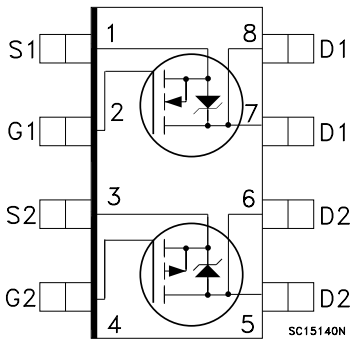


SO-8

Description

This application specific MOSFET is the second generation of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STS4C3F30L	S4C3F30L	SO-8	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
V_{DS}	Drain-source voltage (V_{GS} = 0)	30		V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	30		V
V_{GS}	Gate- source voltage	± 16		V
I_D	Drain current (continuos) at T_C = 25°C S.O.	5	2.7	A
I_D	Drain current (continuos) at T_C = 100°C S.O.	3.2	1.7	A
I_{DM} (1)	Drain current (pulsed)	20	11	A
P_{TOT}	Total dissipation at T_C = 25°C D.O. Total dissipation at T_C = 25°C S.O.	1.6 2		W W
T_{stg}	Storage temperature	-60 to 150		W/°C
T_j	Max. operating junction temperature	150		°C

1. Pulse width limited by safe operating area

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case S.O.	62.5	°C/W
	Thermal resistance junction-case D.O.	78.0	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test condictions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} = 0	n-ch p-ch	30 30			V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125°C	n-ch p-ch			1 1	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V	n-ch p-ch			±100 ±100	nA nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	n-ch p-ch	1 1	1.6 1.6	2.5 2.5	V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 2A V_{GS} = 10V, I_D = 1.5A V_{GS} = 4.5V, I_D = 2A V_{GS} = 4.5V, I_D = 1.5A	n-ch p-ch n-ch p-ch		0.044 0.145 0.051 0.160	0.055 0.165 0.065 0.20	Ω Ω Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test condictions		Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} >$I_{D(on)}$x$R_{DS(on)max}$, I_D=3.5A V_{DS} >$I_{D(on)}$x$R_{DS(on)max}$, I_D=2A	n-ch p-ch		6 4		S S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	n-ch p-ch		220 420		pF pF
C_{oss}	Output capacitance		n-ch p-ch		115 95		pF pF
C_{rss}	Reverse transfer capacitance		n-ch p-ch		23 30		pF pF
Q_g	Total gate charge	**N-channel** V_{DD} = 24V, I_D = 5 A V_{GS} = 10V	n-ch p-ch		9.5 4.8	2 7	nC nC
Q_{gs}	Gate-source charge	**P-channel** V_{DD} =15V, I_D = 3 A V_{GS} = 4.5V	n-ch p-ch		2.25 1.7		nC nC
Q_{gd}	Gate-drain charge	(see Figure 24)	n-ch p-ch		1.7 2		nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Switching times

Symbol	Parameter	Test condictions		Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	**N-channel**	n-ch		13		ns
		V_{DD} = 15V, I_D = 2.5 A	p-ch		15		ns
t_r	Rise time	R_G = 4.7Ω, V_{GS} = 10V	n-ch		27		ns
		P-channel	p-ch		37		ns
$t_{d(off)}$	Turn-off-delay time	V_{DD} = 15V, I_D = 1.5 A	n-ch		10		ns
		R_G = 4.7Ω, V_{GS} = 4.5V	p-ch		90		ns
t_f	Fall time	(see Figure 26)	n-ch		3		ns
			p-ch		23		ns

Table 6. Source drain diode

Symbol	Parameter	Test condictions		Min	Typ.	Max	Unit
I_{SD}	Source-drain current		n-ch			5	A
			p-ch			3	A
I_{SDM} (1)	Source-drain current (pulsed)		n-ch			20	A
			p-ch			12	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0	n-ch			1.2	V
			p-ch			1.2	V
t_{rr}	Reverse recovery time	**N-channel**	n-ch		28		ns
		I_{SD} = 3.5A, di/dt=100A/µs	p-ch		35		ns
		V_{DD} = 15V, T_j = 150°C					
Q_{rr}	Reverse recovery charge	**P-channel**	n-ch		18		nC
		I_{SD} = 3A, di/dt=100 A/µs	p-ch		25		nC
I_{RRM}	Reverse recovery current	V_{DD} = 15V, T_j = 150°C	n-ch		1.3		A
		(see Figure 28)	p-ch		1.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area n-ch

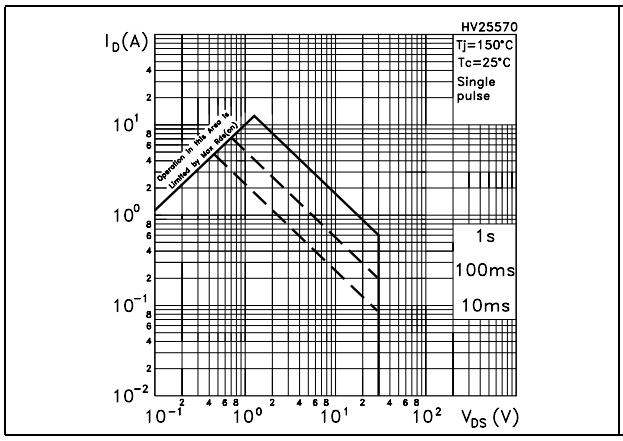


Figure 2. Thermal impedance n-ch

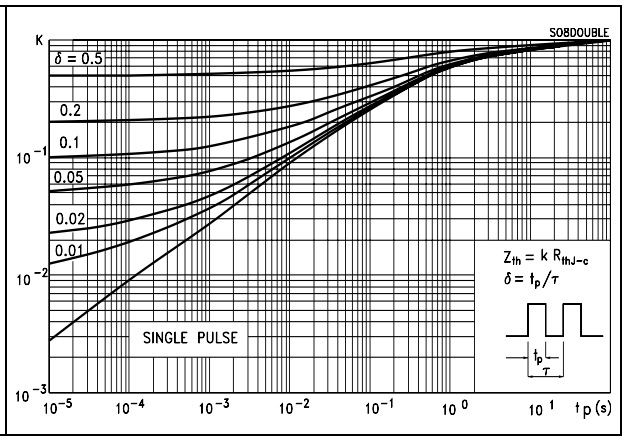


Figure 3. Output characterisics n-ch

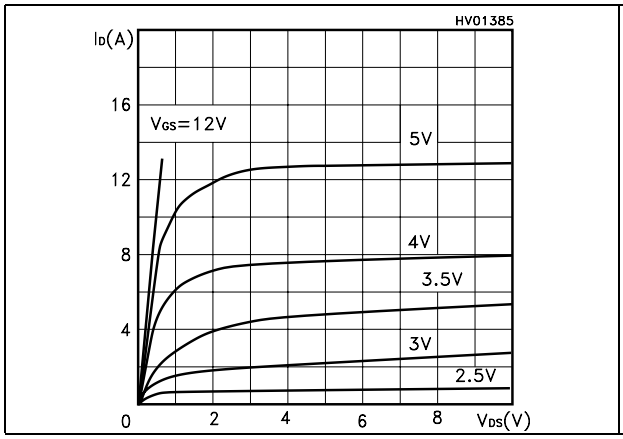


Figure 4. Transfer characteristics n-ch

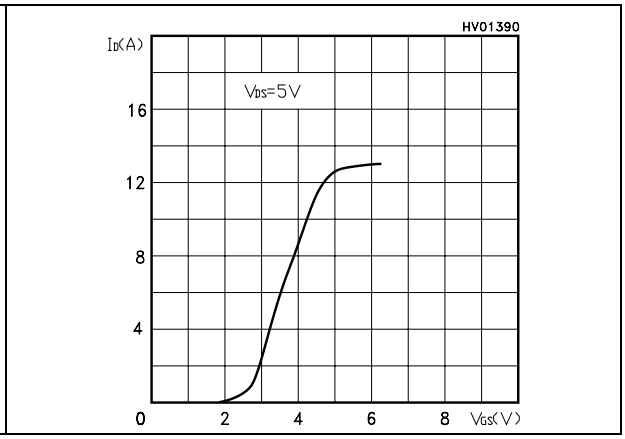


Figure 5. Transconductance n-ch

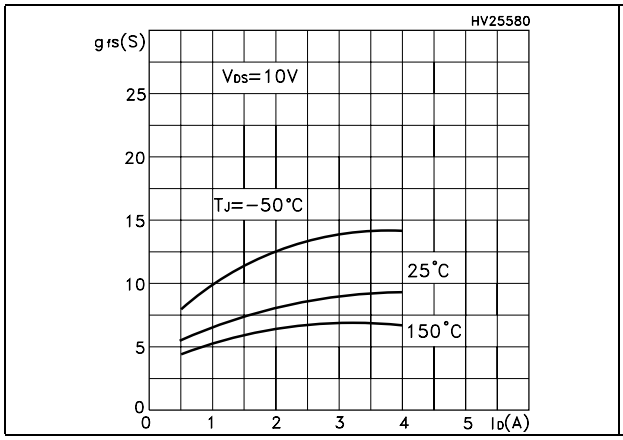


Figure 6. Static drain-source on resistance n-ch

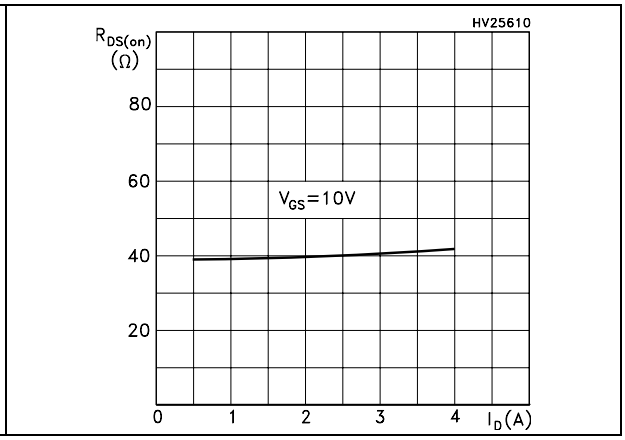


Figure 7. Gate charge vs gate-source voltage n-ch

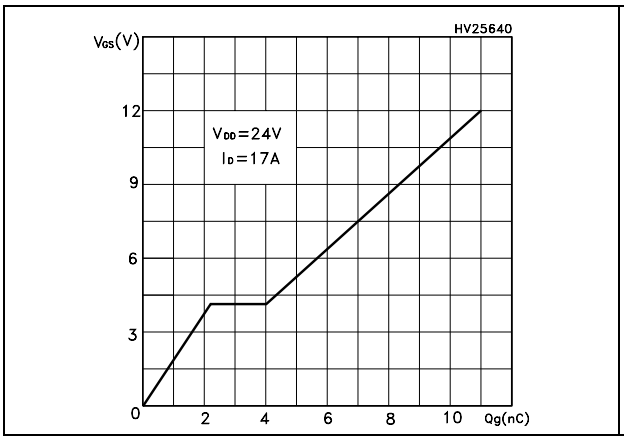


Figure 8. Capacitance variations n-ch

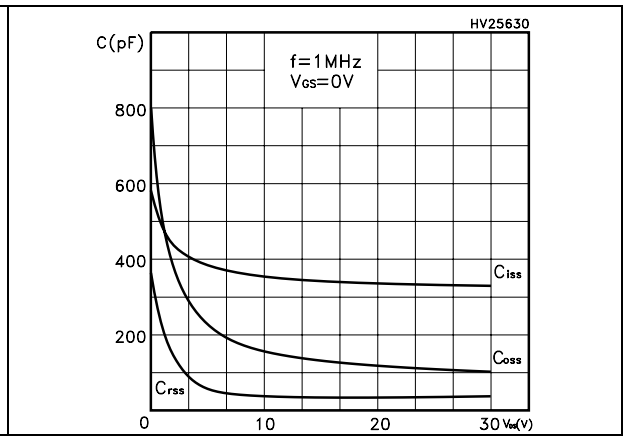


Figure 9. Normalized gate threshold voltage vs temperature n-ch

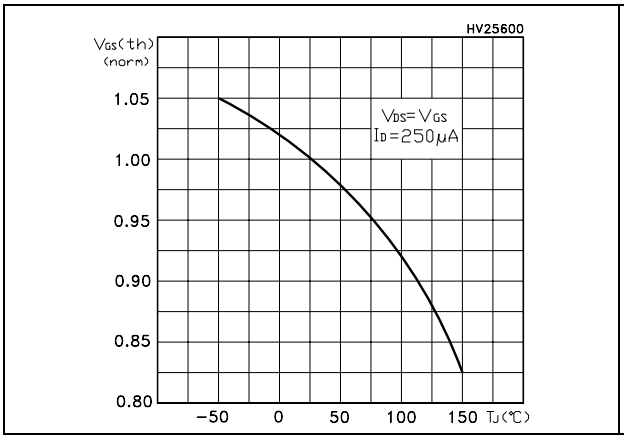


Figure 10. Normalized on resistance vs temperature n-ch

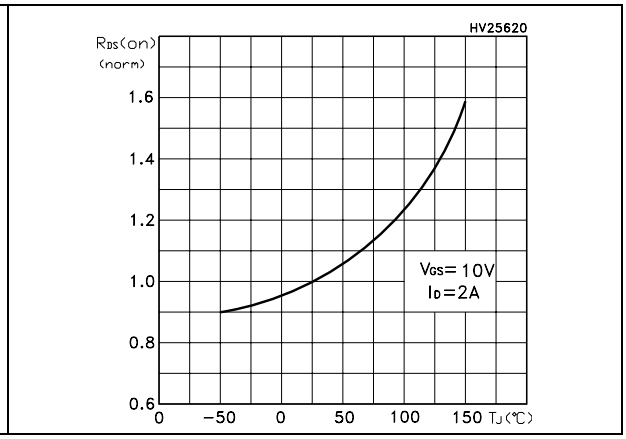


Figure 11. Source-drain diode forward characteristics n-ch

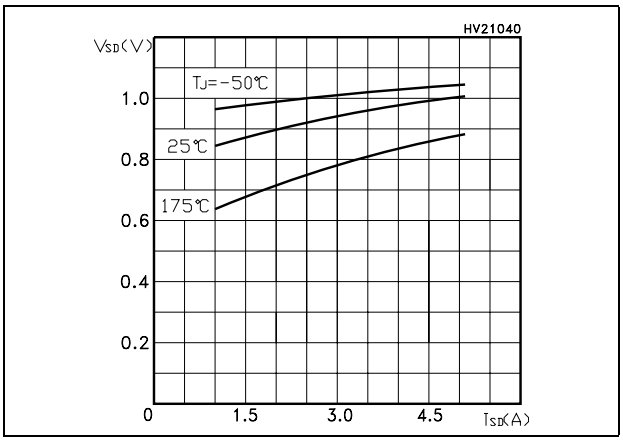


Figure 12. Safe operating area p-ch

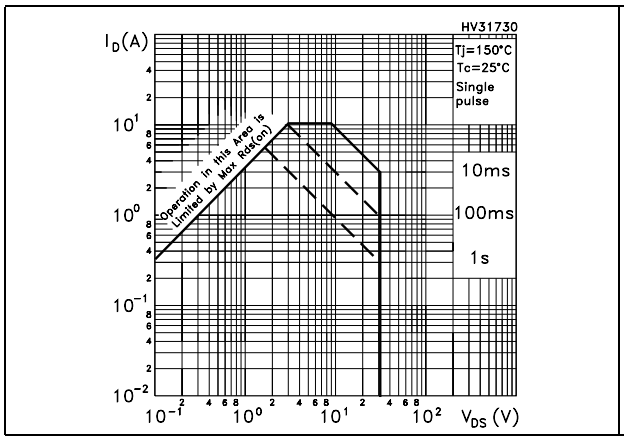


Figure 13. Thermal impedance p-ch

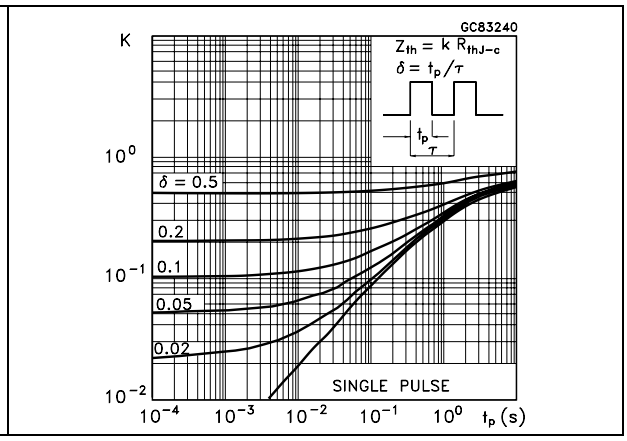


Figure 14. Output characterisics p-ch

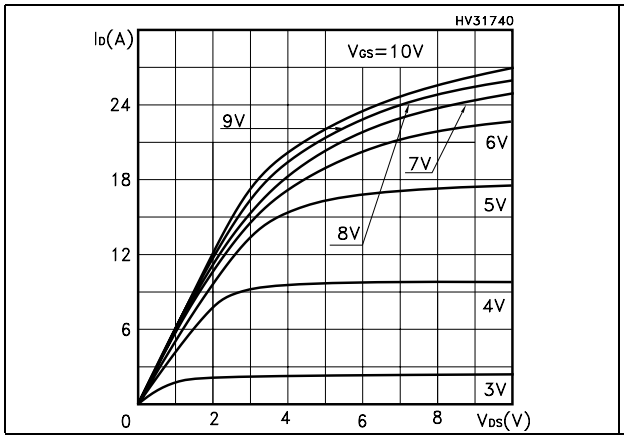


Figure 15. Transfer characteristicsp-ch

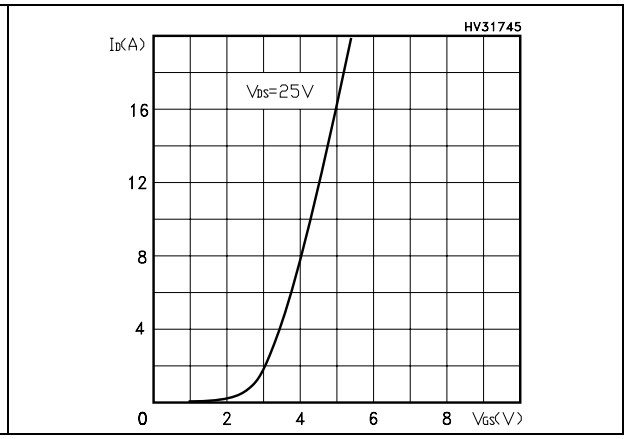


Figure 16. Transconductance p-ch

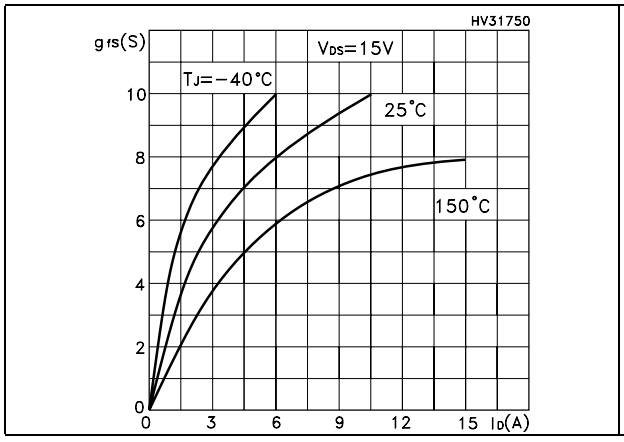


Figure 17. Static drain-source on resistance p-ch

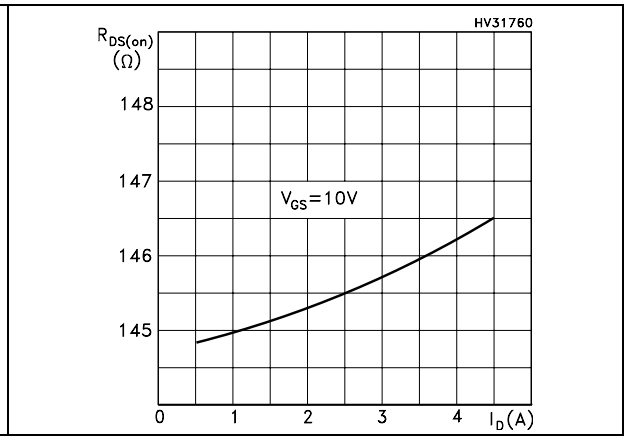


Figure 18. Gate charge vs gate-source voltage p-ch

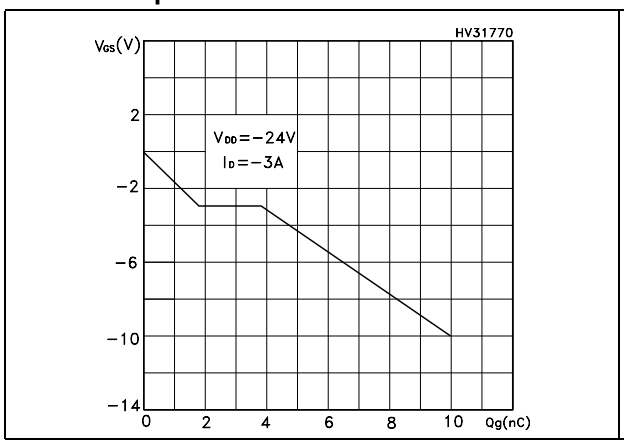


Figure 19. Capacitance variations p-ch

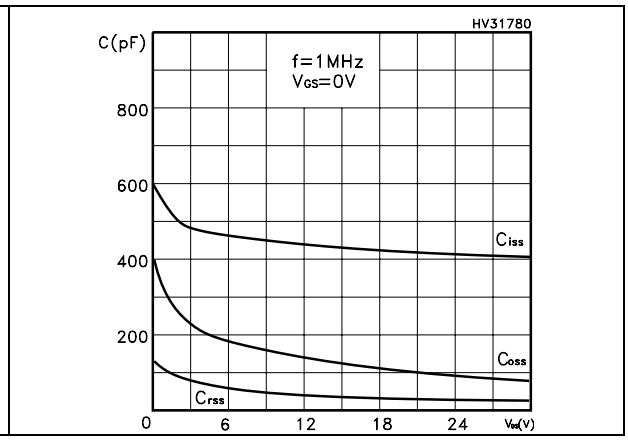


Figure 20. Normalized gate threshold voltage vs temperature p-ch

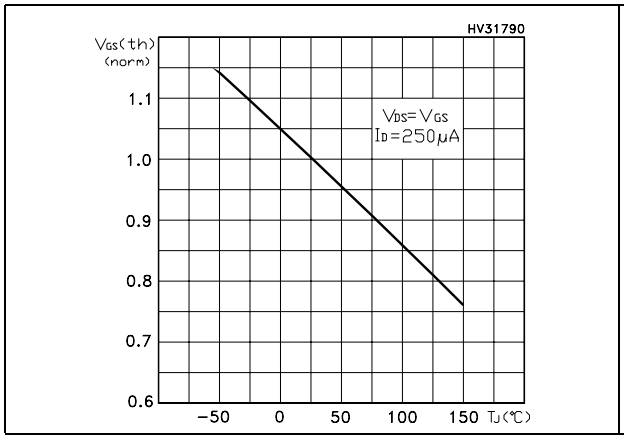


Figure 21. Normalized on resistance vs temperature p-ch

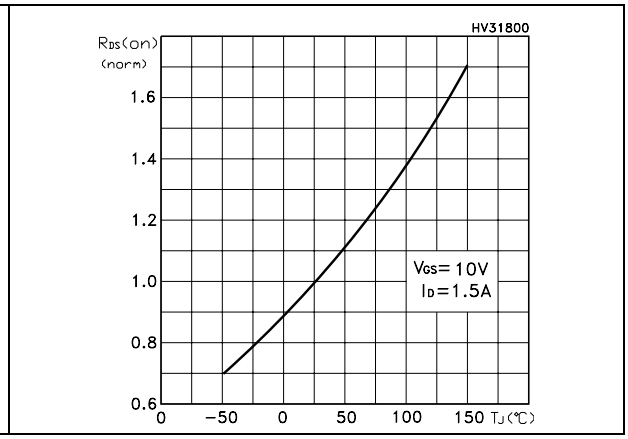
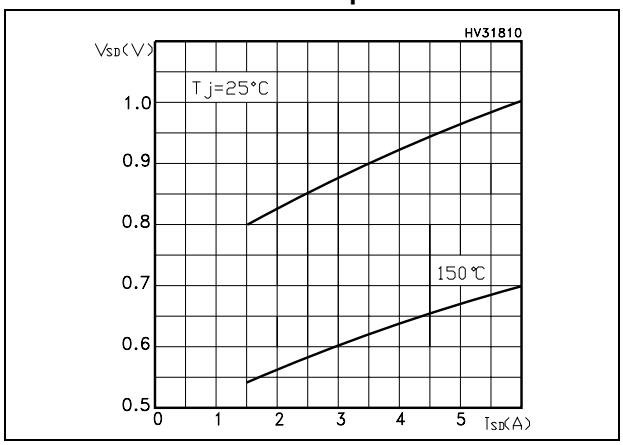


Figure 22. Source-drain diode forward characteristics p-ch



3 Test circuit

Figure 23. Switching times test circuit for resistive load

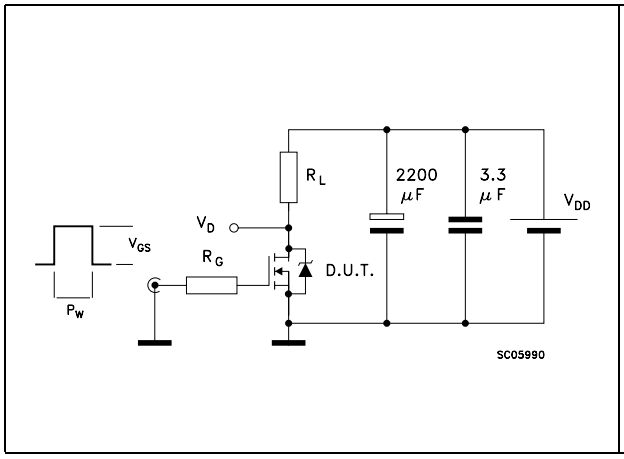


Figure 24. Gate charge test circuit

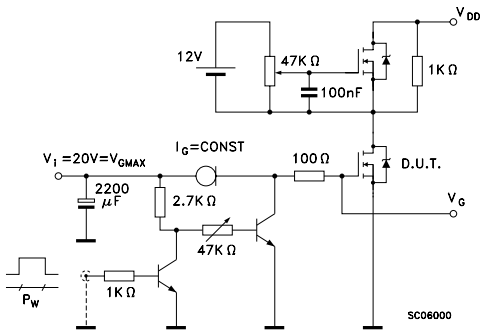


Figure 25. Test circuit for inductive load switching and diode recovery times

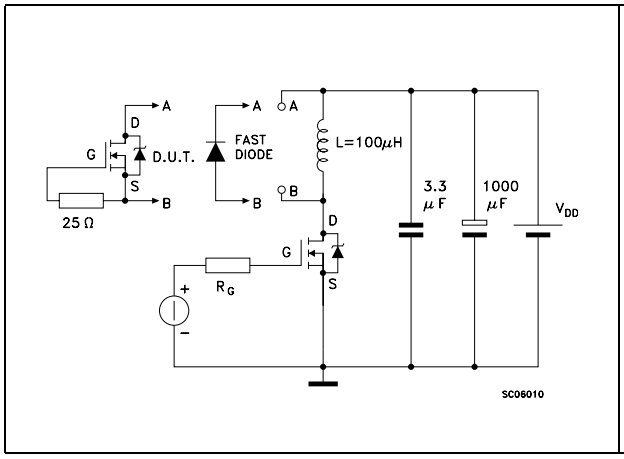


Figure 26. Unclamped Inductive load test circuit

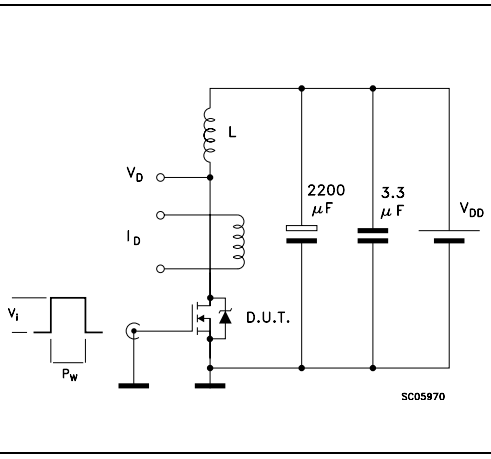


Figure 27. Unclamped inductive waveform

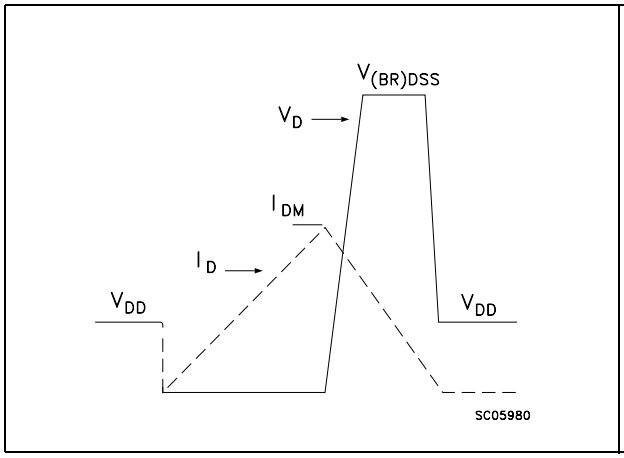
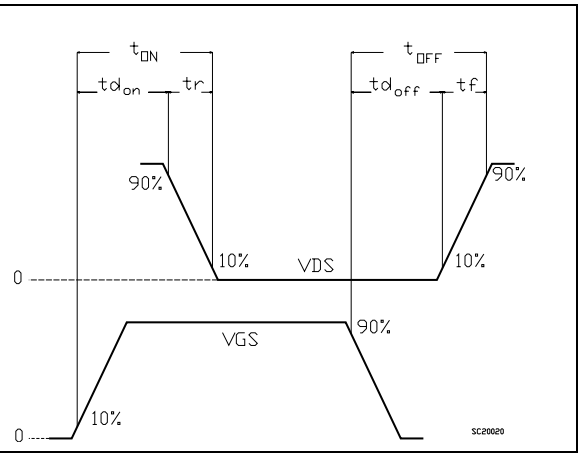


Figure 28. Switching time waveform

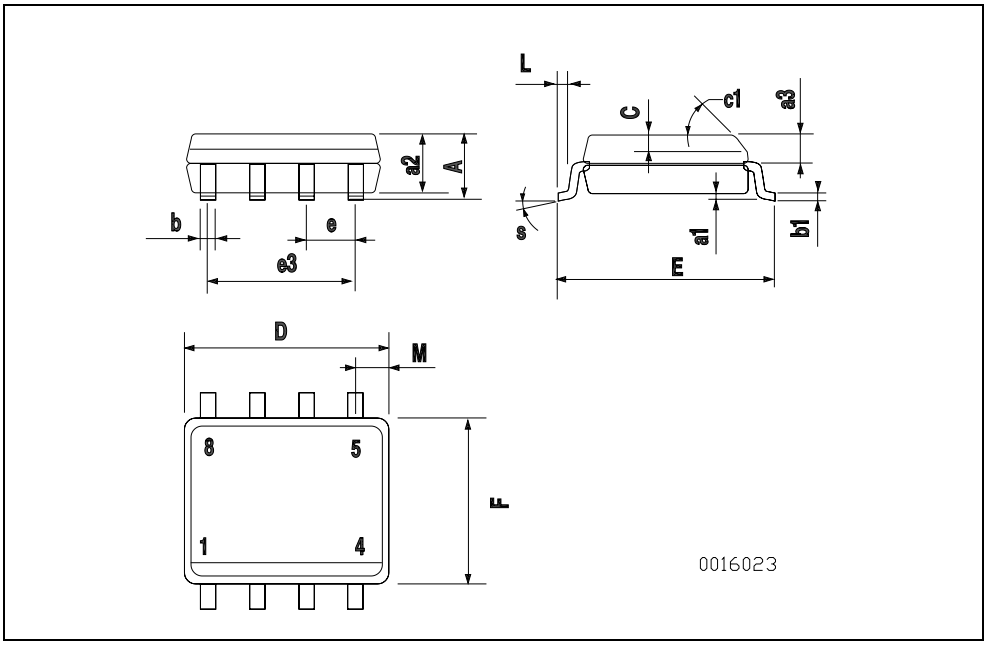


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
12-May-2006	1	First release

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