

### STS9NH3LL

# N-channel 30 V - 0.018 $\Omega$ - 9 A - SO-8 low gate charge STripFET<sup>TM</sup> III Power MOSFET

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STS9NH3LL	30 V	$0.022~\Omega$	9 A

- Optimal R<sub>DS(on)</sub> x Qg trade-off @ 4.5 V
- Conduction losses reduced
- Switching losses reduced

#### **Application**

Switching applications

#### **Description**

This application specific Power MOSFET is the third generation of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

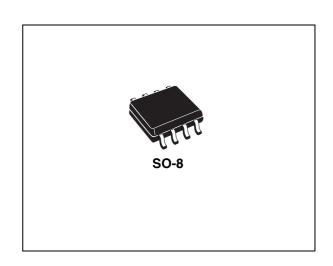


Figure 1. Internal schematic diagram

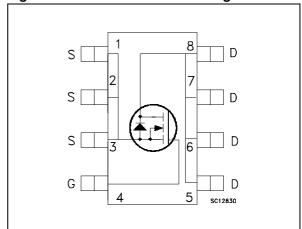


Table 1. Device summary

Order code	de Marking Package		Packaging
STS9NH3LL	S9NH3LL	SO-8	Tape & reel

Contents STS9NH3LL

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STS9NH3LL Electrical ratings

### 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	30	V
V <sub>GS</sub>	Gate-source voltage	±16	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	9	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	6	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	36	Α
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	2.5	W
E <sub>AS</sub> (2)	Single pulse avalanche energy	100	mJ
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150	°C

<sup>1.</sup> Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-amb</sub> <sup>(1)</sup>	Thermal resistance junction-ambient max	50	°C/W

<sup>1.</sup> When mounted on 1 inch² FR-4 board, 2oz Cu (t < 10 sec.)

<sup>2.</sup> Starting  $T_J = 25$  °C,  $I_D = 6$  A.

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### 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

Table 4. On/off states

Symbol Parameter		Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating @ 125 °C			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±16 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			V
R <sub>DS(on)</sub>	Static drain-source on resistance	$V_{GS}$ = 10 V, $I_{D}$ = 4.5 A $V_{GS}$ = 4.5 V, $I_{D}$ = 4.5 A		0.018 0.020	0.022 0.025	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (1)	Forward transconductance	$V_{DS} = 10 \text{ V}, I_D = 4.5 \text{ A}$		8.5		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25 V, f=1 MHz, V <sub>GS</sub> =0		857 147 20		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ = 15 V, $I_{D}$ = 9 A $V_{GS}$ = 4.5 V, (see Figure 16)		7.0 2.5 2.3	10	nC nC nC

<sup>1.</sup> Pulsed: pulse duration=300 μs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on delay time Rise time	$V_{DD}$ =15 V, $I_{D}$ = 4.5 A, $R_{G}$ = 4.7 $\Omega$ , $V_{GS}$ = 4.5 V (see Figure 15)		12 14.5		ns ns
t <sub>d(off)</sub>	Turn-off delay time Fall time	$V_{DD}$ =15 V, $I_{D}$ = 4.5 A, $R_{G}$ = 4.7 $\Omega$ , $V_{GS}$ = 4.5 V (see Figure 15)		23 8		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current Source-drain current (pulsed)				9 36	A A
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 4.5 A, V <sub>GS</sub> =0			1.5	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}$ = 9 A, di/dt = 100 A/µs, $V_{DD}$ = 15 V, Tj=150 °C (see Figure 17)		15 5.7 0.76		ns nC A

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration=300  $\mu$ s, duty cycle 1.5%

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### 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

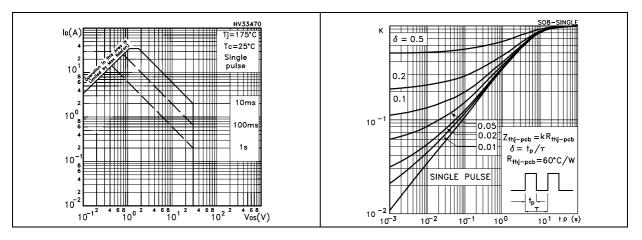


Figure 4. Output characteristics

Figure 5. Transfer characteristics

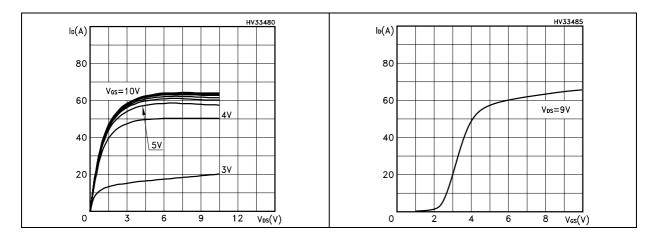


Figure 6. Transconductance

Figure 7. Static drain-source on resistance

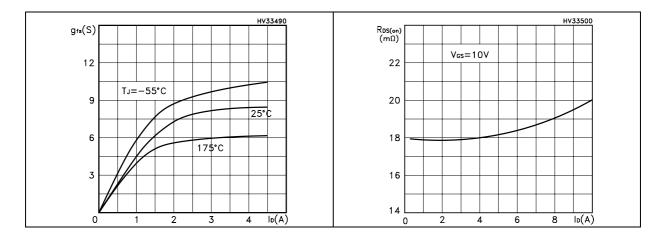


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

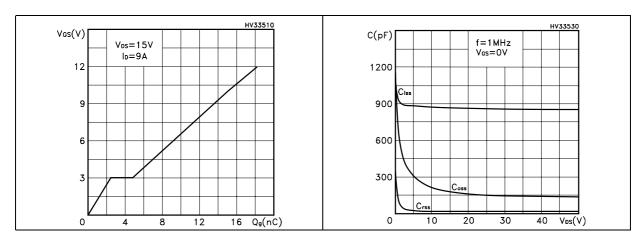


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

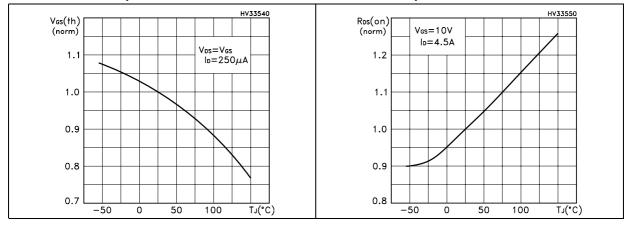
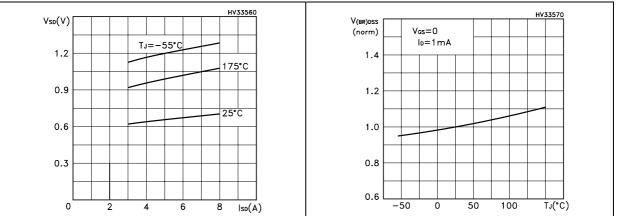


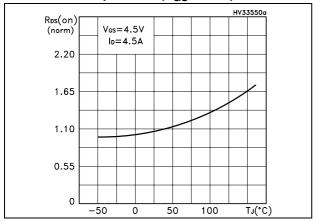
Figure 12. Source-drain diode forward characteristics

Figure 13. Normalized breakdown voltage vs temperature



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Figure 14. Normalized on resistance vs temperature ( $V_{GS} = 4.5V$ )



STS9NH3LL Test circuit

### 3 Test circuit

Figure 15. Switching times test circuit for resistive load

Figure 16. Gate charge test circuit

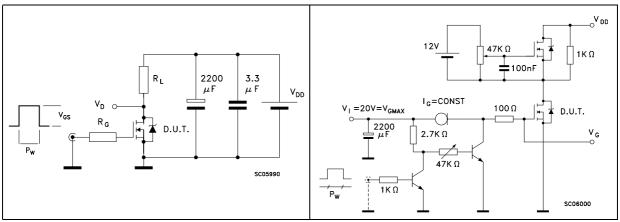


Figure 17. Test circuit for inductive load switching and diode recovery times

Figure 18. Unclamped inductive load test circuit

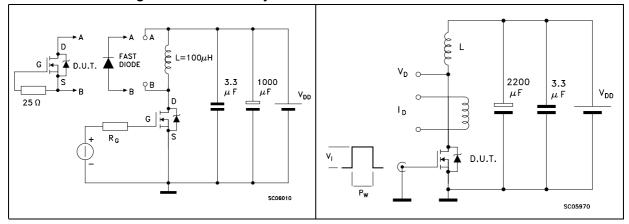
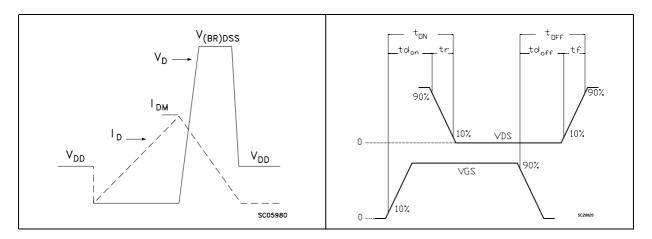


Figure 19. Unclamped inductive waveform

Figure 20. Switching time waveform



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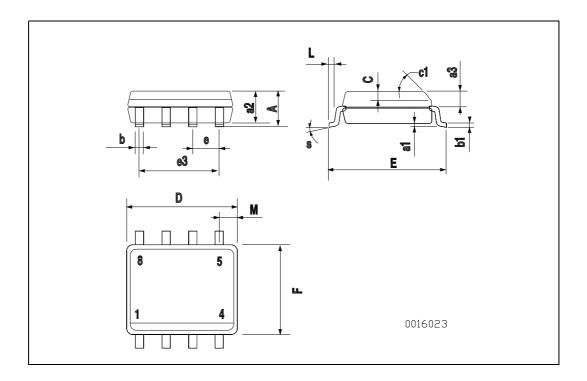
### 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: <a href="https://www.st.com">www.st.com</a>

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#### **SO-8 MECHANICAL DATA**

DIM	mm.			inch		
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1		•	45	(typ.)	•	
D	4.8		5.0	0.188		0.196
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S		•	8 (r	nax.)	•	·



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Revision history STS9NH3LL

## 5 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Jul-2006	1	Initial release.
15-May-2007	2	Update on <i>Table 2</i> .
12-Dec-2007	3	<ul> <li>Inserted Figure 14: Normalized on resistance vs temperature (V<sub>GS</sub> = 4.5V)</li> <li>Inserted new E<sub>AS</sub> value on Table 2.</li> </ul>

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