



STV200N55F3

N-channel 55 V - 1.8 mΩ - 200 A - PowerSO-10
STripFET™ Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on)}	I _D ⁽¹⁾
STV200N55F3	55 V	< 2.5 mΩ	200 A

1. Current limited by package

- Conduction losses reduced
- Low profile, very low parasitic inductance

Applications

- Switching applications

Description

This N-channel enhancement mode Power MOSFET is the latest refinement of ST's STripFET™ process. The resulting transistor shows extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

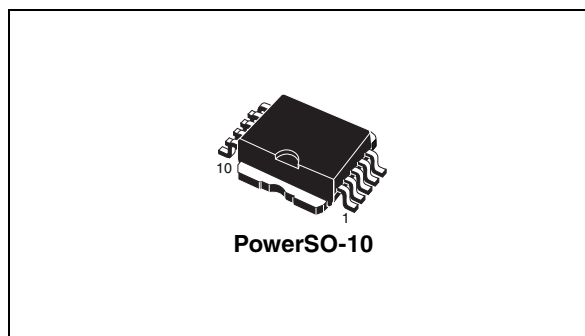


Figure 1. Internal schematic diagram and connection diagram (top view)

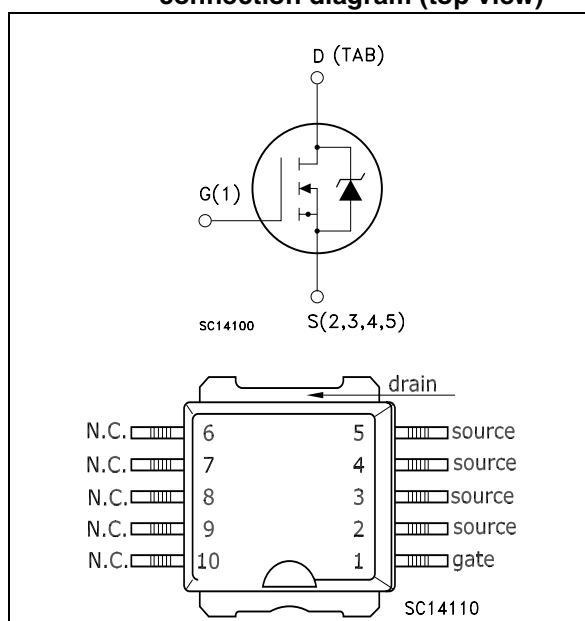


Table 1. Device summary

Order code	Marking	Package	Packaging
STV200N55F3	200N55F3	PowerSO-10	Tape and reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($v_{gs} = 0$)	55	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	200	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	170	A
$I_{DM}^{(2)}$	Drain current (pulsed)	800	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.0	J
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to R_{thj-c}
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 60\text{ A}$, $V_{DD} = 35\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb Max	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4 2 oz Cu

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	55			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 75\text{ A}$		1.8	2.5	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		6800		pF
C_{oss}	Output capacitance			1450		pF
C_{rss}	Reverse transfer capacitance			15		pF
Q_g	Total gate charge	$V_{DD} = 44\text{ V}$, $I_D = 120\text{ A}$,		100		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$		30		nC
Q_{gd}	Gate-drain charge	(see Figure 3)		26		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 27.5 \text{ V}$, $I_D = 60 \text{ A}$ $R_G = 4.7 \ \Omega$, $V_{GS} = 10 \text{ V}$, (see Figure 2)		25 150		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 27.5 \text{ V}$, $I_D = 60 \text{ A}$ $R_G = 4.7 \ \Omega$, $V_{GS} = 10 \text{ V}$, (see Figure 2)		110 50		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SD}^{(1)}$	Source-drain current Source-drain current (pulsed)				200 800	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120 \text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 120 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 35 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 7)		60 110 3.5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

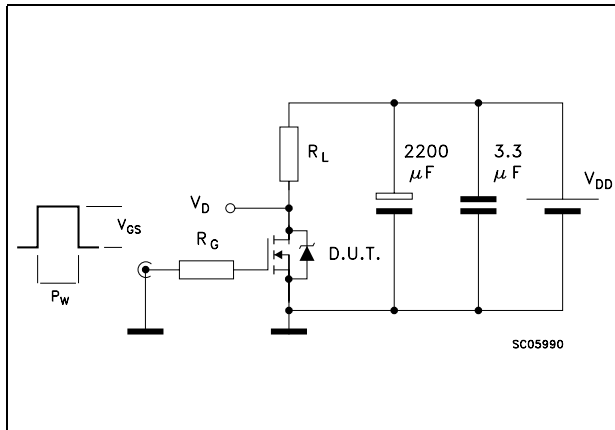


Figure 3. Gate charge test circuit

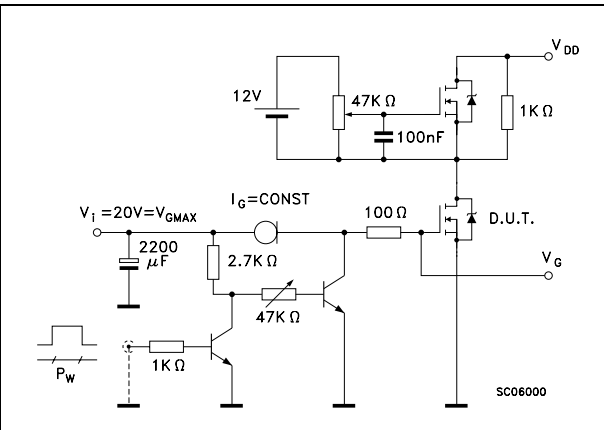


Figure 4. Test circuit for inductive load switching and diode recovery times

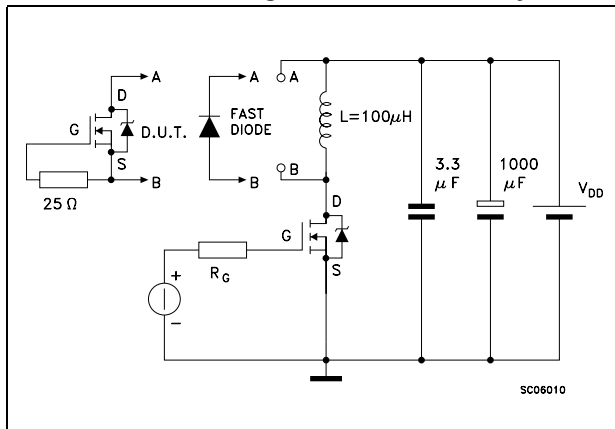


Figure 5. Unclamped inductive load test circuit

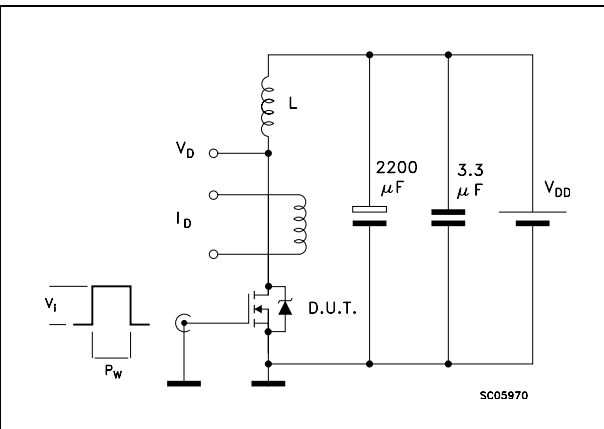


Figure 6. Unclamped inductive waveform

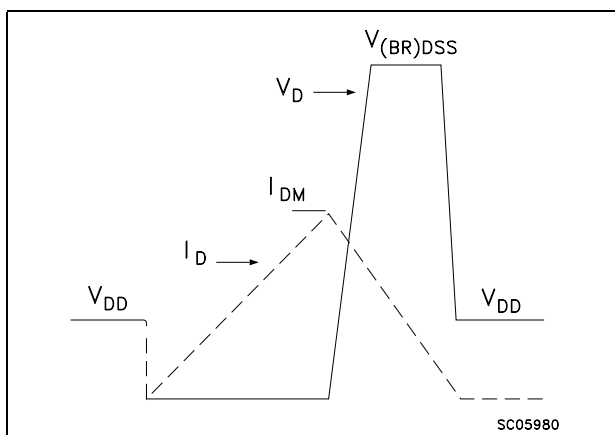
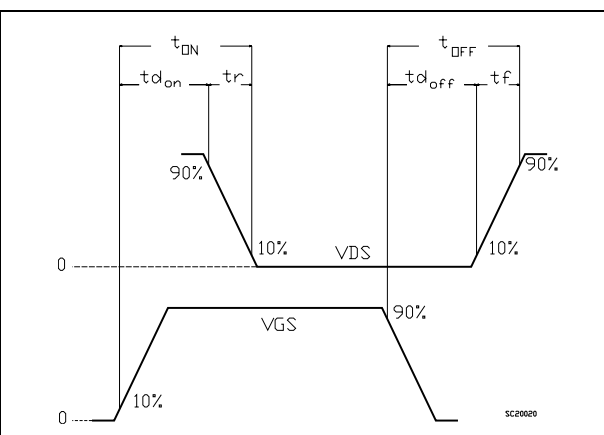


Figure 7. Switching time waveform

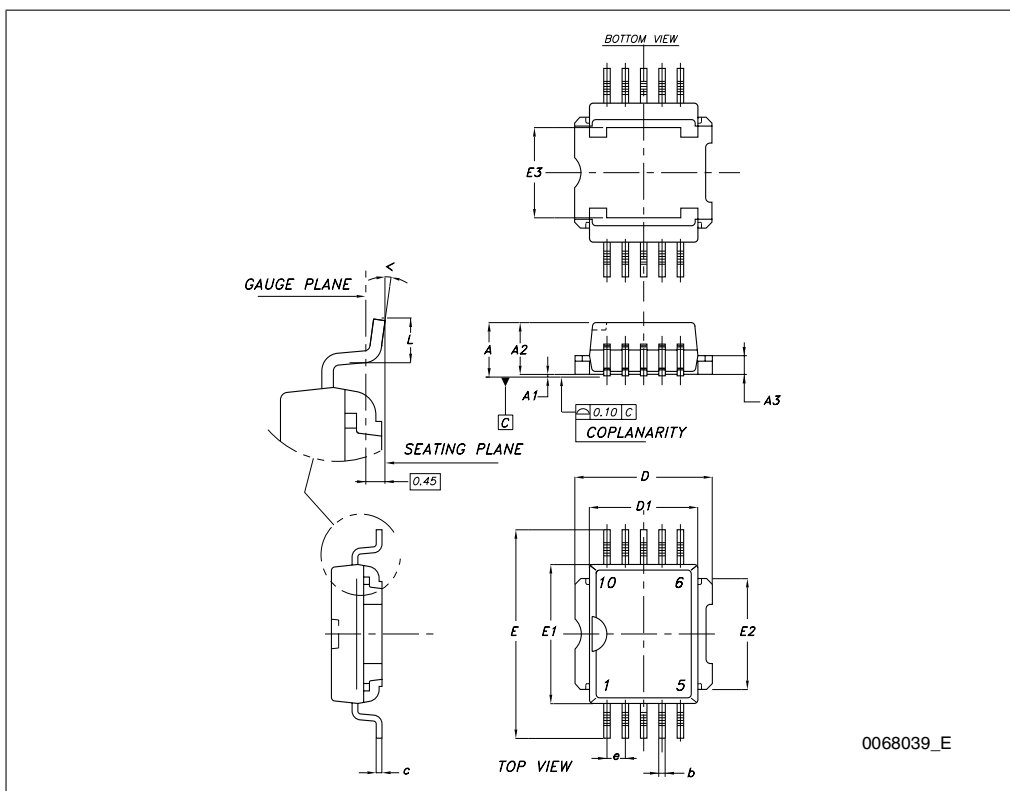


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

PowerSO-10 mechanical data

Dim	mm		
	Min	Typ	Max
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1	7.40		7.60
E	13.80		14.40
E1	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
05-Mar-2008	1	First release

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