

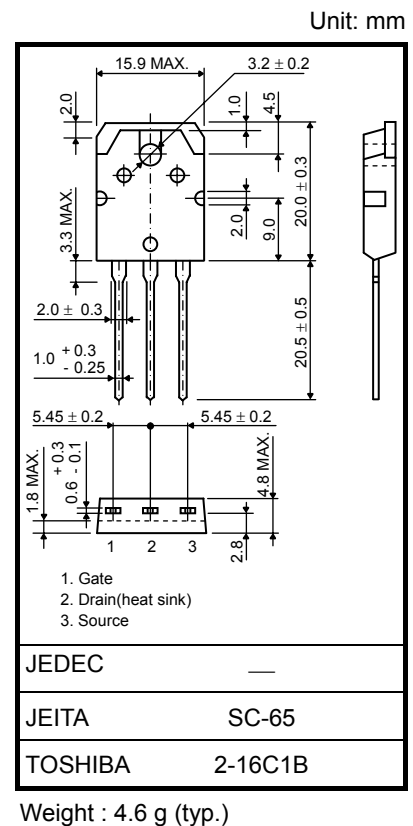
TK12J60U

Switching Regulator Applications

- Low drain-source ON resistance: $R_{DS(ON)} = 0.36$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 7.0$ S (typ.)
- Low leakage current: $I_{DSS} = 100 \mu A$ ($V_{DS} = 600$ V)
- Enhancement-mode: $V_{th} = 3.0\sim 5.0$ V ($V_{DS} = 10$ V, $I_D = 1$ mA)

Absolute Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	600	V
Gate-source voltage		V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	12	A
	Pulse ($t = 1$ ms) (Note 1)	I_{DP}	24	
Drain power dissipation ($T_c = 25^\circ C$)		P_D	144	W
Single pulse avalanche energy (Note 2)		E_{AS}	69	mJ
Avalanche current (Note 3)		I_{AR}	12	A
Repetitive avalanche energy		E_{AR}	14	mJ
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	-55 to 150	$^\circ C$



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

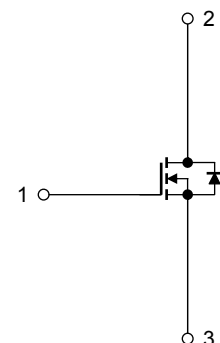
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.868	$^\circ C/W$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	50	$^\circ C/W$

Note 1: Please use devices on conditions that the channel temperature is below $150^\circ C$.

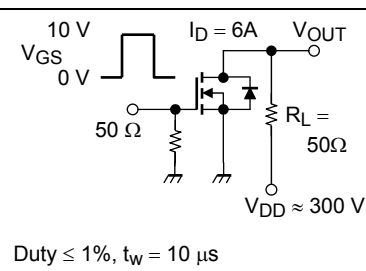
Note 2: $V_{DD} = 90$ V, $T_{ch} = 25^\circ C$ (initial), $L = 0.84$ mH, $R_G = 25$, $I_{AR} = 12$ A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.



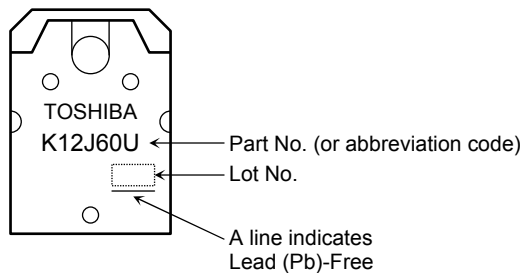
Electrical Characteristics (Ta = 25°C)

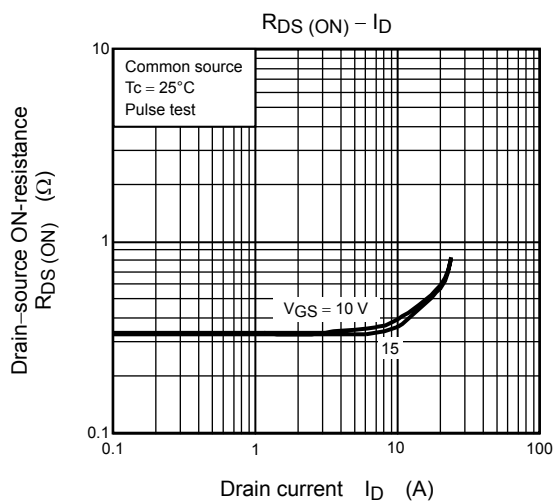
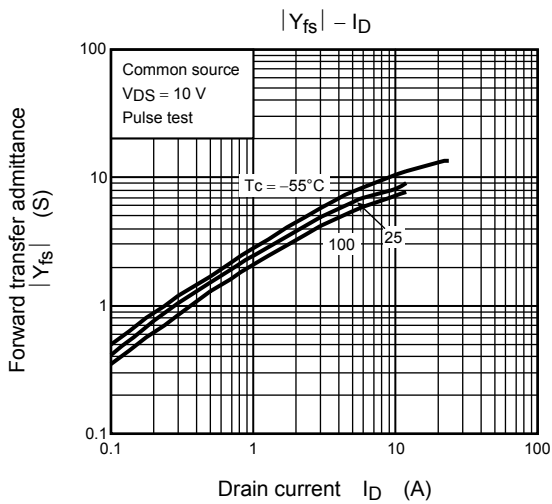
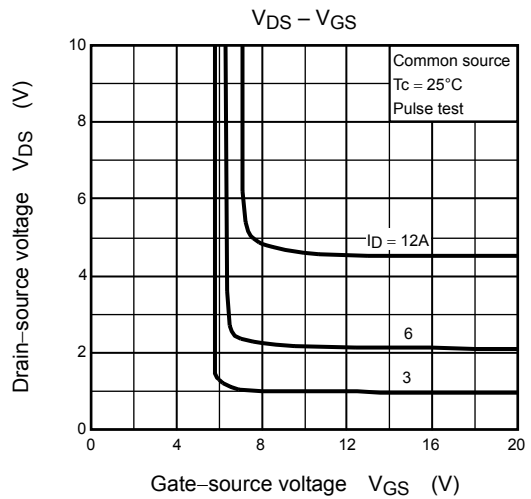
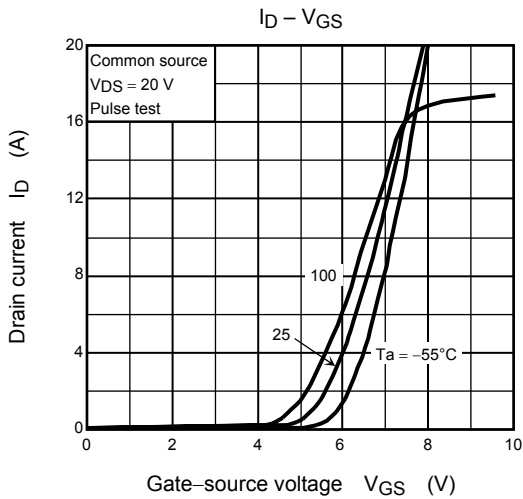
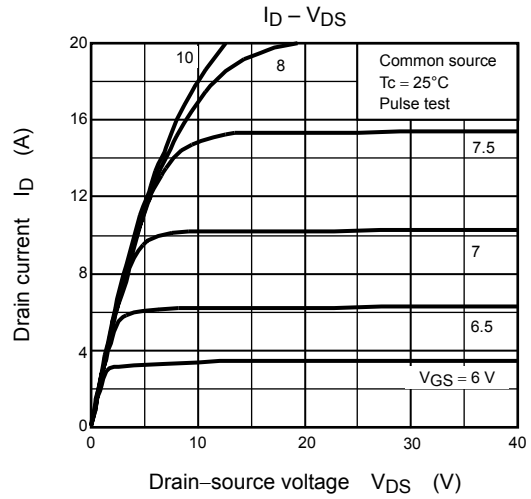
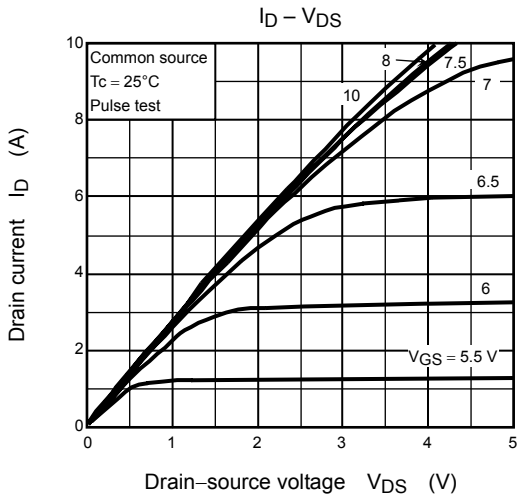
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 1	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	600	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	3.0	—	5.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	—	0.36	0.4	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 6\text{ A}$	2.0	7.0	—	S
Input capacitance		C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	720	—	pF
Reverse transfer capacitance		C_{rss}		—	55	—	
Output capacitance		C_{oss}		—	1700	—	
Switching time	Rise time	t_r		—	30	—	ns
	Turn-on time	t_{on}		—	60	—	
	Fall time	t_f		—	8	—	
	Turn-off time	t_{off}		Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$	—	75	
Total gate charge		Q_g	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	—	14	—	nC
Gate-source charge		Q_{gs}		—	8.5	—	
Gate-drain charge		Q_{gd}		—	5.5	—	

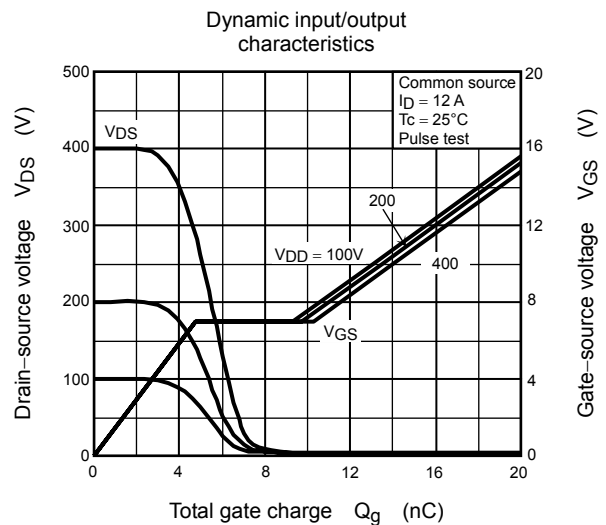
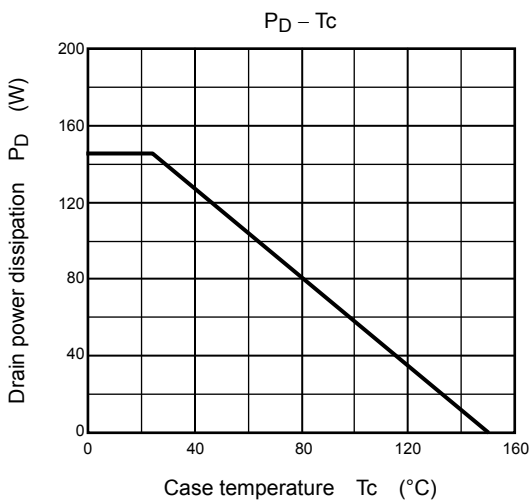
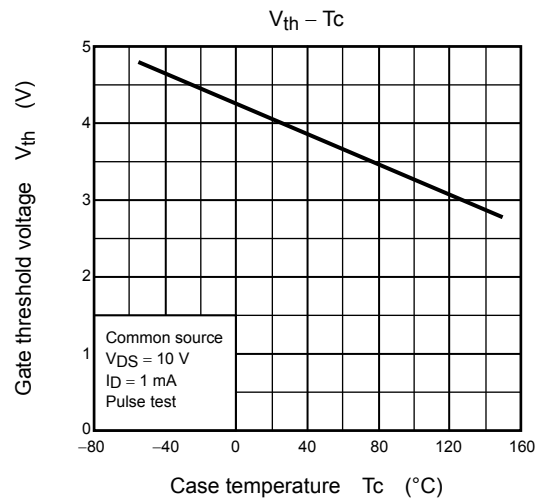
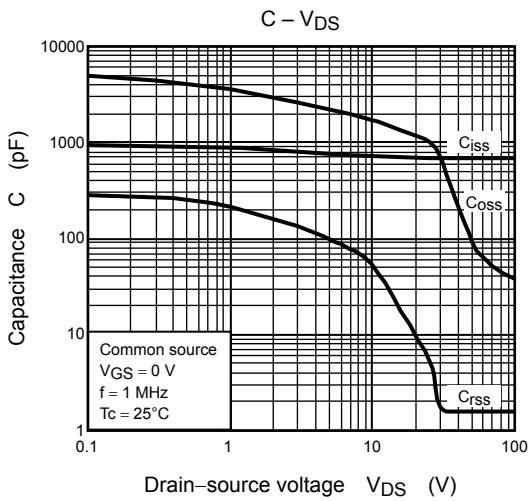
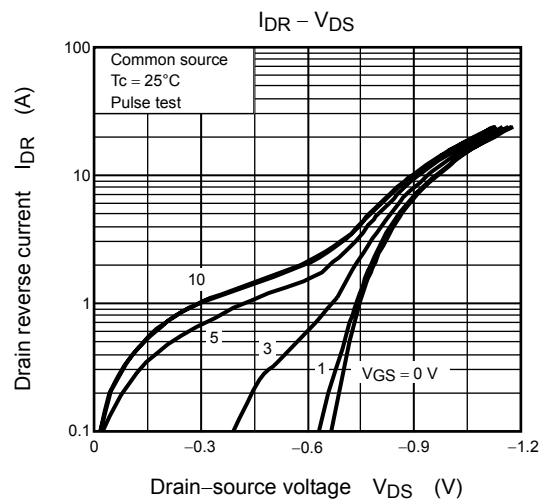
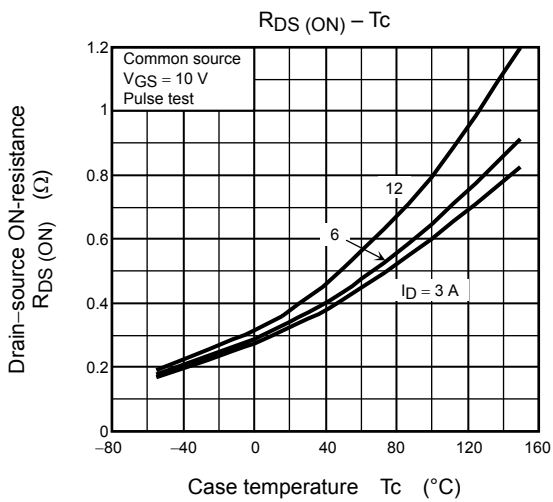
Source-Drain Ratings and Characteristics (Ta = 25°C)

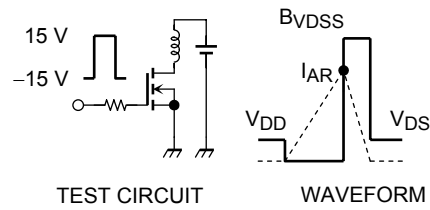
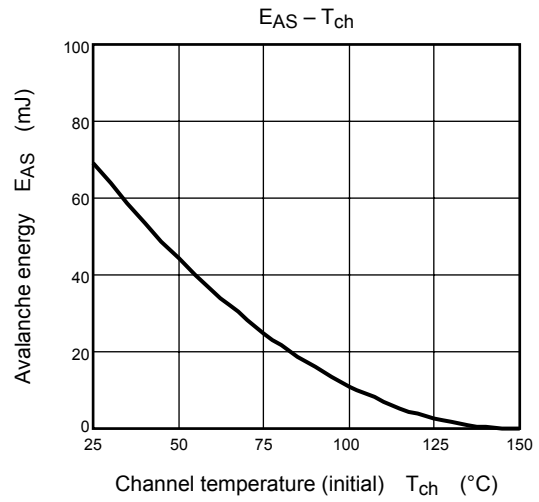
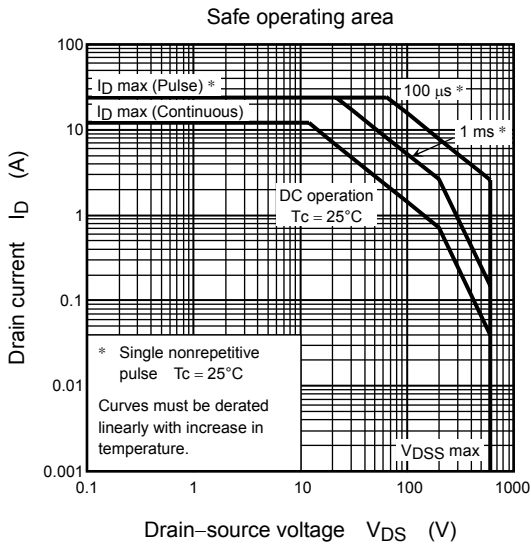
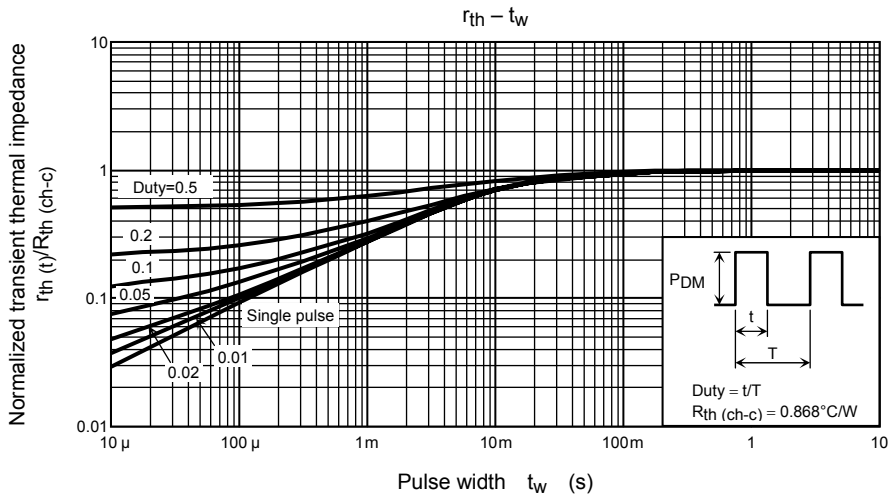
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	12	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	24	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 12\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 12\text{ A}, V_{GS} = 0\text{ V},$	—	380	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	5.3	—	μC

Marking









$R_G = 25 \Omega$
 $V_{DD} = 90 V, L = 0.84 mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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