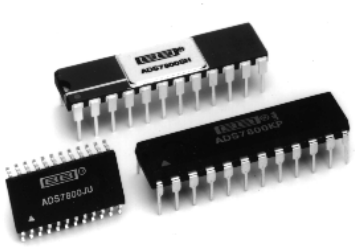
ADS7800



SBAS001A – OCTOBER 1989 – REVISED FEBRUARY 2004

12-Bit 3µs Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **333k SAMPLES PER SECOND**
- **STANDARD ±10V AND ±5V INPUT RANGES**
- **DC PERFORMANCE OVER TEMP:**
  No Missing Codes
  1/2LSB Integral Linearity Error
  3/4LSB Differential Linearity Error
- **AC PERFORMANCE OVER TEMP:**
  72dB Signal-to-Noise Ratio
  80dB Spurious-Free Dynamic Range
  –80dB Total Harmonic Distortion
- **INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND THREE-STATE OUTPUTS**
- **POWER DISSIPATION: 215mW max**
- **PACKAGE: 24-Pin Single-Wide DIP**
  24-Lead SOIC

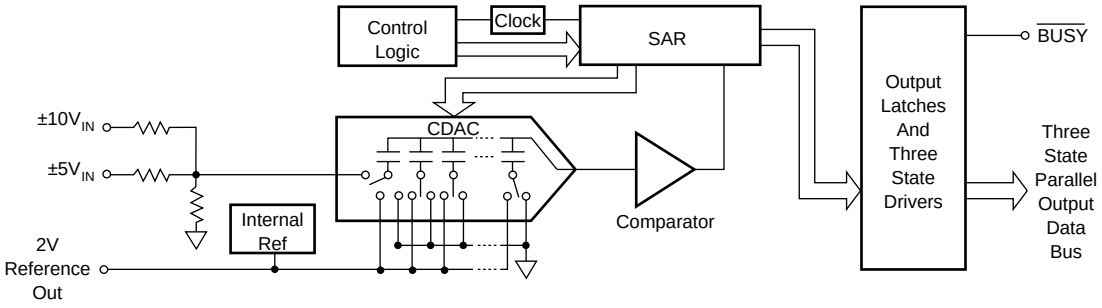
DESCRIPTION

The ADS7800 is a complete 12-bit sampling analog-to-digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high-speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of ±5V or ±10V.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a –12V or –15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and –40°C to +85°C temperature ranges.



SPECIFICATIONS

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH			ADS7800KP/KU/BH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V/±5V			*		V
Impedance	±10V Range	4.4	6.3	8.1	*	*	*	kΩ
	±5V Range	2.9	4.2	5.4	*	*	*	kΩ
THROUGHPUT SPEED								
Conversion Time	Conversion Alone		2.5	2.7		*	*	µs
Complete Cycle	Acquisition + Conversion		2.6	3.0		*	*	µs
Throughput Rate		333	380		*	*		kHz
DC ACCURACY								
Full Scale Error[1]				±0.50			±0.35	%
Full Scale Error Drift			6			*		ppm/°C
Integral Linearity Error				±1			±1/2	LSB[2]
Differential Linearity Error				±1			±3/4	LSB
No Missing Codes			Ensured			Ensured		
Bipolar Zero[1]				±4			±2	LSB
Bipolar Zero Drift			1			*		ppm/°C
Power Supply Sensitivity								
	$-16.5V < -V_S < -13.5V$			±1/2			*	LSB
	$-12.6V < -V_S < -11.4V$			±1/2			*	LSB
	$+4.75V < V_S < +5.25V$			±1			±1/2	LSB
Transition Noise[3]			0.1			*		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 47kHz	74	77		77	80		dB[4]
Total Harmonic Distortion	f_{IN} = 47kHz		–77	–74		–80	–77	dB
Two-tone Intermodulation Distortion	f_{IN1} = 24.4kHz (–6dB) f_{IN2} = 28.5kHz (–6dB)		–77	–74		–80	–77	dB
Signal-to-(Noise + Distortion) Ratio	f_{IN} = 47kHz	67	70		69	72		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 47kHz	68	71		70	73		dB
SAMPLING DYNAMICS								
Aperture Delay			13			*		ns
Aperture Jitter			150			*		ps, rms
Transient Response[5]			130			*		ns
Overvoltage Recovery[6]			150			*		ns
INTERNAL REFERENCE VOLTAGE								
Voltage		1.9	2.0	2.1	*	*	*	V
Source Current Available for External Loads			10			*		µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		+5.3	*		*	V
I_{IL}		–5			*			µA
I_{IH}		+5			*			µA
DIGITAL OUTPUTS								
Data Format		Parallel, 12-bit or 8-bit/4-bit						
Data Coding		Binary Offset Binary						
V_{OL}	I_{SINK} = 1.6mA	0.0		+0.4	*		*	V
V_{OH}	I_{SOURCE} = 500µA	+2.4		+5.0	*		*	V
$I_{LEAKAGE}$ (High-Z State)			±0.1	±5		*	*	µA
POWER SUPPLIES								
Rated Voltage								
$-V_S$		–11.4	–15	–16.5	*	*	*	V
V_S (V_{SA} and V_{SD})		+4.75	+5.0	+5.25	*	*	*	V
Current								
$-I_S$			3.5	6		*	*	mA
I_S			18	25		*	*	mA
Power Consumption			135	215		*	*	mW

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX}, Sampling Frequency, f_S, = 333kHz, $-V_S = -15V$, $V_S = +5V$, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7800JP/JU/AH			ADS7800KP/KU/BH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	JP/JU/KP/KU	0		+70	*		*	°C
	AH/BH	–40		+85	*		*	°C
Operating	JP/KP/JU/KU	–40		+85	*		*	°C
Storage		–65		+150	*		*	°C

* Same as specification for ADS7800JP/JU/AH.

NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the ±5V range, 1LSB = 4.88mV for the ±10V range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at +125°C. (4) All specifications in dB are referred to a full-scale input, either ±10V or ±5V. (5) For full scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after 2 x F_S input overvoltage.

ABSOLUTE MAXIMUM RATINGS

$-V_S$ to ANALOG COMMON	–16.5V
V_S to DIGITAL COMMON	+7V
Pin 23 (V_{SD}) to Pin 24 (V_{SA})	±0.3V
ANALOG COMMON to DIGITAL COMMON	±1V
Control Inputs to DIGITAL COMMON	–0.3 to V_S + 0.3V
Analog Input Voltage	±20V
Maximum Junction Temperature	160°C
Internal Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}:	
Plastic DIP	100°C/W
SOIC	100°C/W
Ceramic	50°C/W

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTROSTATIC DISCHARGE SENSITIVITY

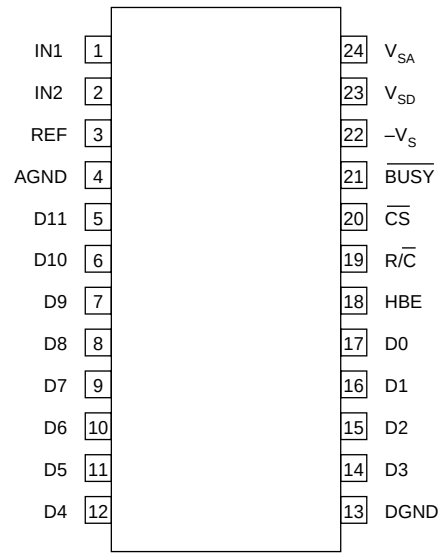
The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	IN1	±10V Analog Input. Connected to GND for ±5V range.
2	IN2	±5V Analog Input. Connected to GND for ±10V range.
3	REF	+2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads.
4	AGND	Analog Ground. Connect to pin 13.
5	D11	Data Bit 11. Most Significant Bit (MSB).
6	D10	Data Bit 10.
7	D9	Data Bit 9.
8	D8	Data Bit 8.
9	D7	Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.
10	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
11	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
12	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
13	DGND	Digital Ground. Connect to pin 4.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH.
18	HBE	High Byte Enable. When held LOW, data output as 12 bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion.
19	R/$\overline{C}$	Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and $\overline{BUSY}$ is HIGH.
20	$\overline{CS}$	Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.
21	$\overline{BUSY}$	Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode.
22	$-V_S$	Negative Power Supply. –12V or –15V. Bypass to GND.
23	V_{SD}	Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND.
24	V_{SA}	Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND.

PIN CONFIGURATION

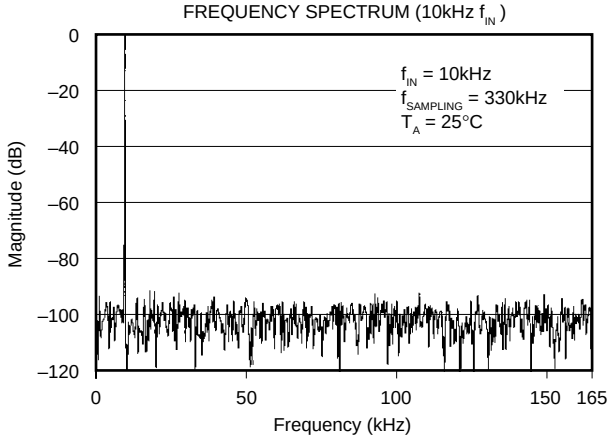
Top View **DIP/SOIC**



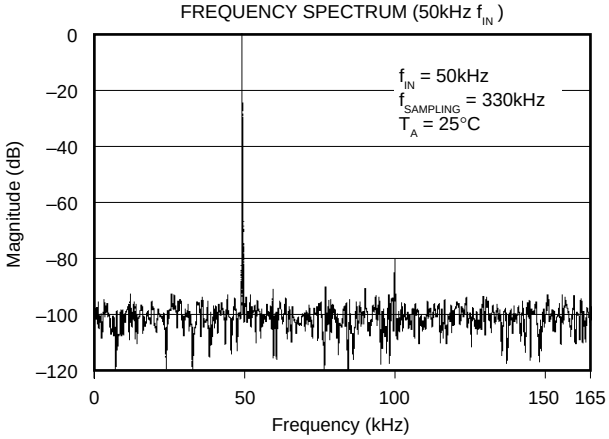
TYPICAL PERFORMANCE CURVES

At $+V_S$ = +5V, $-V_S$ = –15V, and T_A = +25°C, unless otherwise noted. All plots use 1024 point FFTs.

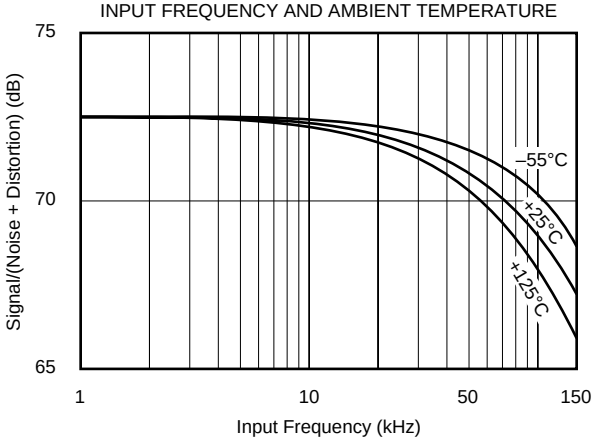
FREQUENCY SPECTRUM (10kHz f_{IN})



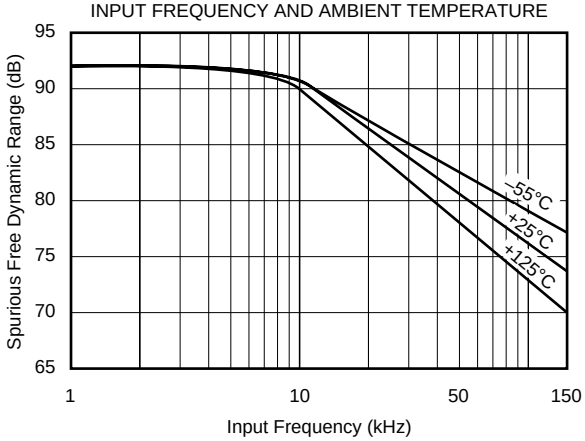
FREQUENCY SPECTRUM (50kHz f_{IN})



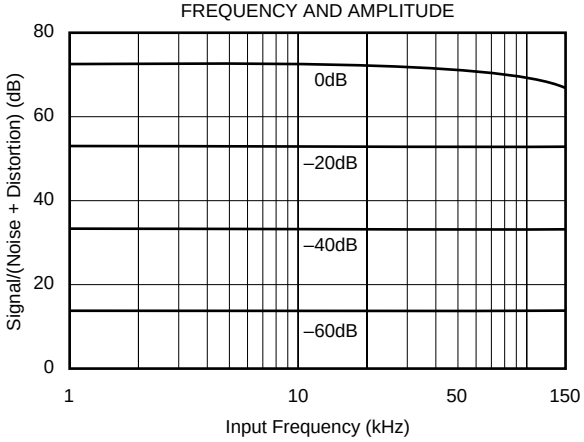
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



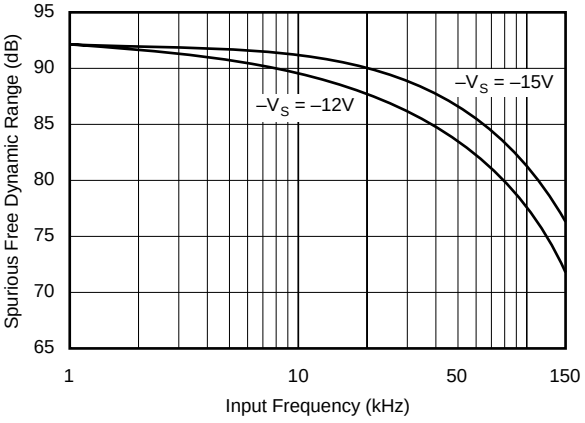
SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



SIGNAL/(NOISE + DISTORTION) vs
FREQUENCY AND AMPLITUDE



SPURIOUS FREE DYNAMIC RANGE vs
INPUT FREQUENCY AND NEGATIVE SUPPLY VOLTAGE



THEORY OF OPERATION

The ADS7800 combines the advantages of advanced CMOS technology (logic density, stable capacitors, and good analog switches) with Burr-Brown's proven skills in laser-trimmed thin-film resistors to provide a complete sampling A/D converter.

A basic charge-redistribution successive approximation architecture converts analog input voltages into digital words. Figure 1 shows the operation of a simplified 3-bit charge redistribution A/D. Precision laser-trimmed scaling resistors at the input divide standard input ranges (±10V or ±5V for the ADS7800) into levels compatible with the CMOS characteristics of the internal capacitor array.

While in the sampling mode, the capacitor array switch for the MSB capacitor (S_1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal, and the remaining array switches (S_2 and S_3) are set to position "R" to provide an accurate bipolar offset from the reference source REF. At the same time, switch S_C is also in the closed position to auto-zero any offset errors in the CMOS comparator.

When a convert command is received, switch S_1 is opened to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command, switches S_2 and S_3 are opened to trap an offset charge, and switch S_C is opened to float the comparator input. The charge trapped on the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S_2 and S_3 to positions "R" (to connect to REF) or "G" (to connect to GND) successively, changing the voltage generated at the comparator input node.

The first approximation connects the MSB capacitor via switch S_1 to REF, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is HIGH or LOW, the logic will then latch S_1 in position "R" or "G", and moves on to make the next approximation by connecting S_2 to REF and S_3 to GND. When the three successive approximation steps are made for this simple converter, the voltage level at the comparator will be within 1/2LSB of GND, and the data output word will be based on reading the positions of S_1, S_2 and S_3.

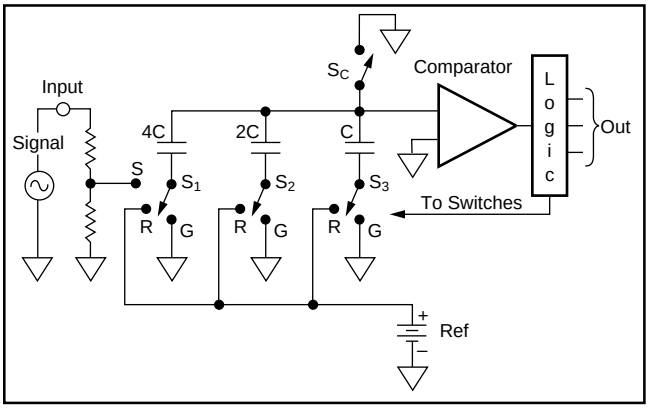


FIGURE 1. 3-Bit Charge Redistribution A/D.

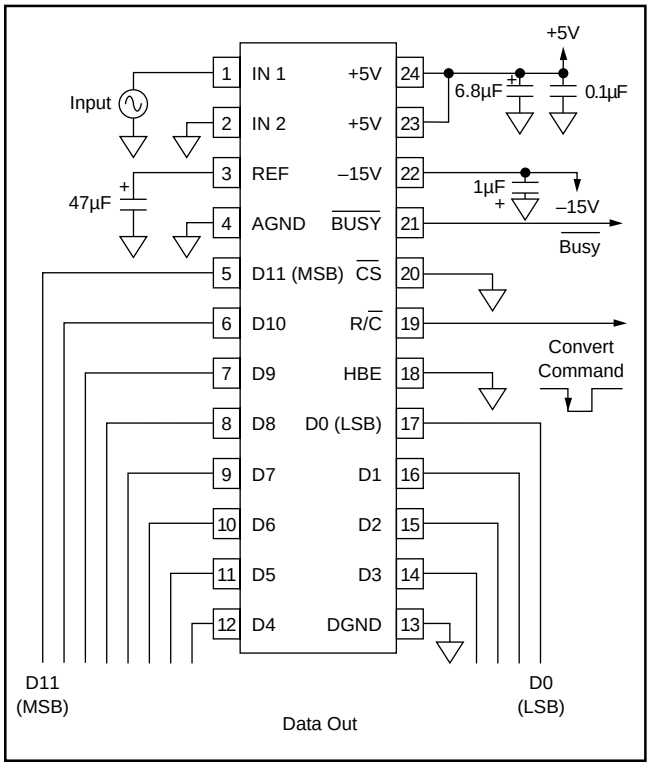


FIGURE 2. Basic ±10V Operation.

OPERATION

BASIC OPERATION

Figure 2 shows the simple hookup circuit required to operate the ADS7800 in a ±10V range in the Convert Mode. A convert command arriving on pin 19, R/$\overline{C}$, (a pulse taking pin 19 LOW for a minimum of 40ns) puts the ADS7800 in the hold mode, and a conversion is started. Pin 21, $\overline{BUSY}$, will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output latches. Thus, the rising edge of the signal on pin 21 can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits input lines. This means that pulses on pin 19 are ignored, so that new conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the ADS7800.

In the Read Mode, the input to pin 19 is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ on pin 19 will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the ADS7800 in a hold mode, and initiates a new conversion.

The ADS7800 will begin acquiring a new sample as soon as the conversion is completed, even before the $\overline{BUSY}$ output rises on pin 21, and will track the input signal until the next conversion is started, whether in the Convert Mode or the Read Mode.

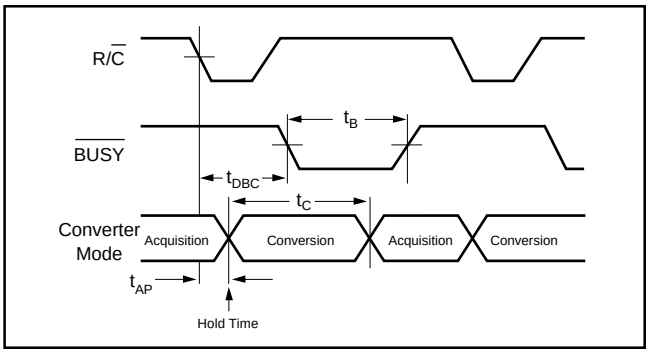


FIGURE 3. Acquisition and Conversion Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

TABLE I. Acquisition and Conversion Timing.

For use with an 8-bit bus, the data can be read out in two bytes under the control of pin 18, HBE. With a LOW input on pin 18, at the end of a conversion, the 8 LSBs of data are loaded into the latches on pins 9 through 12 and 14 through 17. Taking pin 18 HIGH then loads the 4 MSBs on pins 14 through 17, with pins 9 through 12 being forced LOW.

ANALOG INPUT RANGES

The ADS7800 offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration. (See Figures 4 and 5, or 10 and 11.)

CONTROLLING THE ADS7800

The ADS7800 can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the ADS7800 may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in Table II.

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	OPERATION
1	X	X	1	None - Outputs in Hi-Z State.
0	1↓0	0	1	Holds Signal and Initiates Conversion.
0	1	0	1	Output Three-State Buffers Enabled once Conversion has Finished.
0	1	1	1	Enable Hi-Byte in 8-bit Bus Mode.
0	1↓0	1	1	Inhibit Start of Conversion.
0	0	1	1	None - Outputs in Hi-Z State.
X	X	X	0	Conversion in Progress. Outputs Hi-Z State. New Conversion Inhibited until Present Conversion has Finished.

TABLE II. Control Line Functions.

For stand-alone operation, control of the ADS7800 is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition on R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and $\overline{BUSY}$ is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain LOW a minimum of 40ns.

Figure 6 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access of the data after completion of the conversion.

Figure 7 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

CONVERSION START

A conversion is initiated on the ADS7800 only by a negative transition occurring on R/$\overline{C}$, as shown in Table I. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$. Timing relationships for start of conversion are illustrated in Figure 8.

The $\overline{BUSY}$ output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

INTERNAL CLOCK

The ADS7800 has an internal clock that is factory trimmed to achieve a typical conversion time of 2.47µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3µs.

READING DATA

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{C}$ is HIGH, $\overline{BUSY}$ is HIGH and $\overline{CS}$ is LOW. Upon satisfaction of these conditions, the data lines are enabled according to the state of HBE. See Figure 9 and Table III for timing relationships and specifications.

CALIBRATION

OPTIONAL EXTERNAL GAIN AND OFFSET TRIM

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS7800 as shown in Figures 10 and 11.

If adjustment of offset and full scale is not required, connections as shown in Figures 4 and 5 should be used.

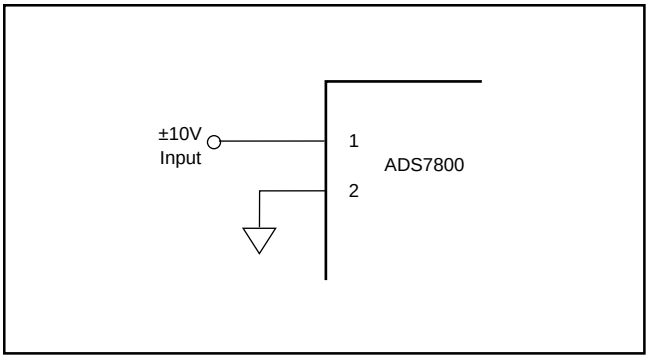


FIGURE 4. ±10V Range Without Trims.

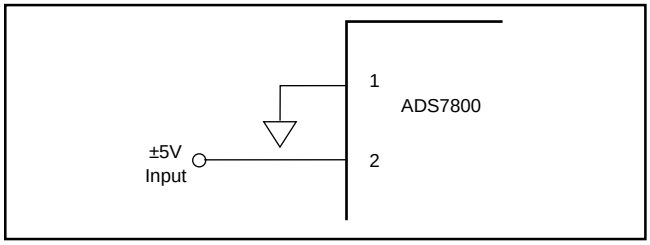


FIGURE 5. ±5V Range Without Trims.

CALIBRATION PROCEDURE

First, trim offset, by applying at the input (pin 1 or 2) the mid-point transition voltage (–2.44mV for the ±10V range, –1.22mV for the ±5V range.) With the ADS7800 converting continually, adjust potentiometer R_1 until the MSB (D11 on pin 5) is toggling alternately HIGH and LOW.

Next adjust full scale, by applying at the input a DC input signal that is 3/2LSB below the nominal full scale voltage (+9.9927V for the ±10V range, +4.9963V for the ±5V range.) With the ADS7800 converting continually, adjust R_2 until the LSB (D0 on pin 17) is toggling HIGH and LOW with all of the other bits HIGH.

LAYOUT CONSIDERATIONS

Because of the high resolution and linearity of the ADS7800, system design problems such as ground path resistance and contact resistance become very important.

ANALOG SIGNAL SOURCE IMPEDANCE

The input resistance of the ADS7800 is 6.3kΩ or 4.2kΩ (for the ±10V and ±5V ranges respectively.) To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal.

Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the ADS7800, to maximize accuracy on the chip. They should be connected together as close as possible to the unit.

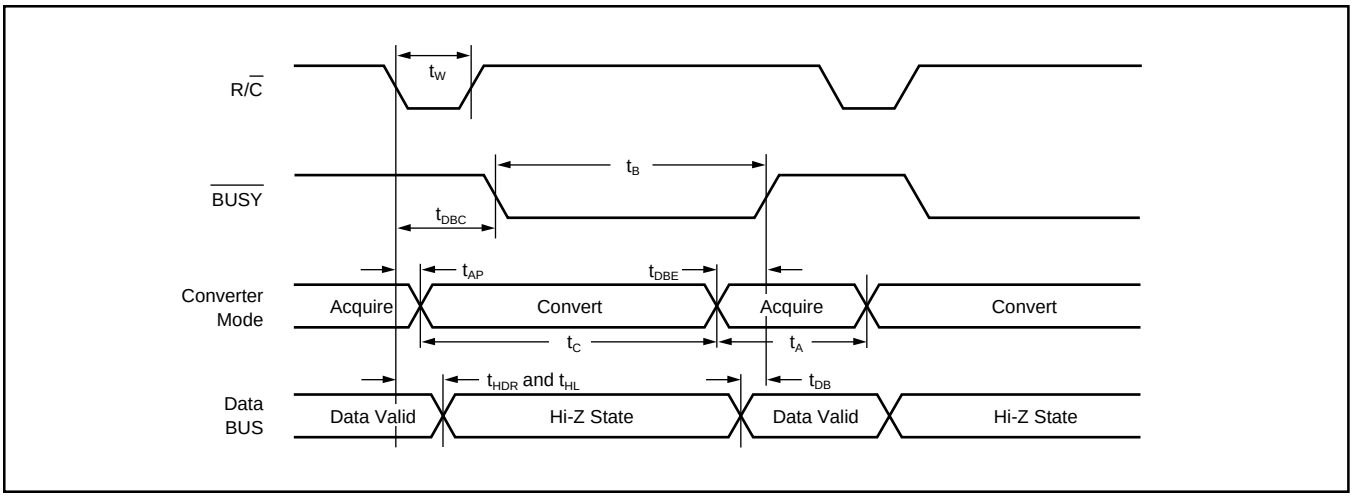


FIGURE 6. Convert Mode: R/$\overline{C}$ Pulse LOW — Outputs Enabled After Conversion.

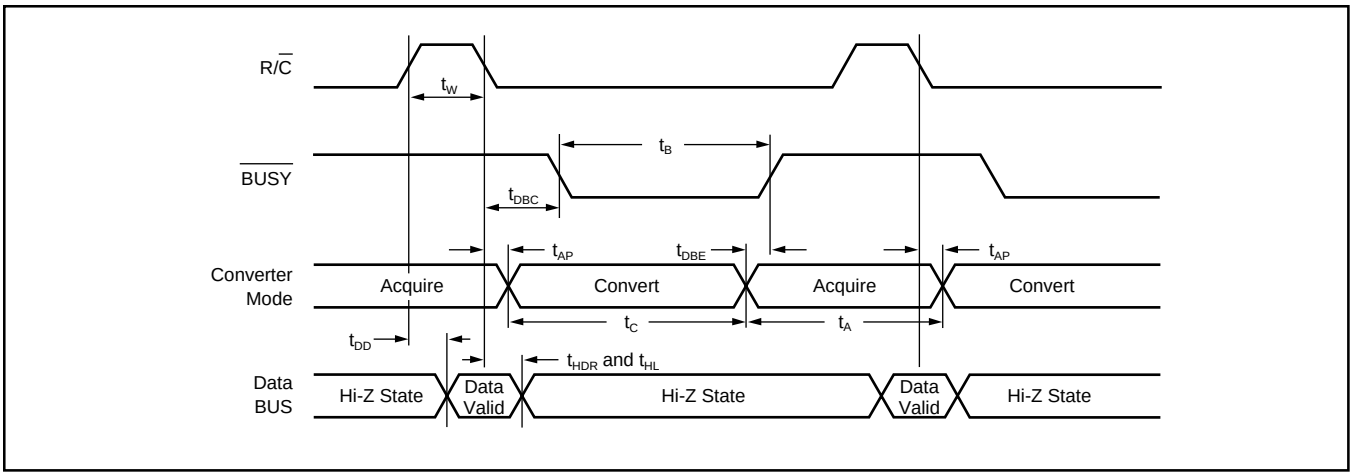


FIGURE 7. Read Mode: R/$\overline{C}$ Pulse HIGH— Outputs Enabled Only When R/$\overline{C}$ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_W	R/$\overline{C}$ Pulse Width	40	10		ns
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ LOW		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		ns
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
t_A+t_C	Throughput Time		2.6	3.0	µs
t_{HDR}	Valid Data Held After R/$\overline{C}$ LOW	20	50		ns
t_S	$\overline{CS}$ or HBE LOW before R/$\overline{C}$ Falls	25	5		ns
t_H	$\overline{CS}$ or HBE LOW after R/$\overline{C}$ Falls	25	0		ns
t_{DD}	Data Valid from $\overline{CS}$ LOW, R/$\overline{C}$ HIGH, and HBE in Desired State (Load = 100pF)		65	150	ns
t_{HDR}	Valid Data Held After R/$\overline{C}$ Low	20	50		ns
t_{HL}	Delay to Hi-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown)		50	150	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

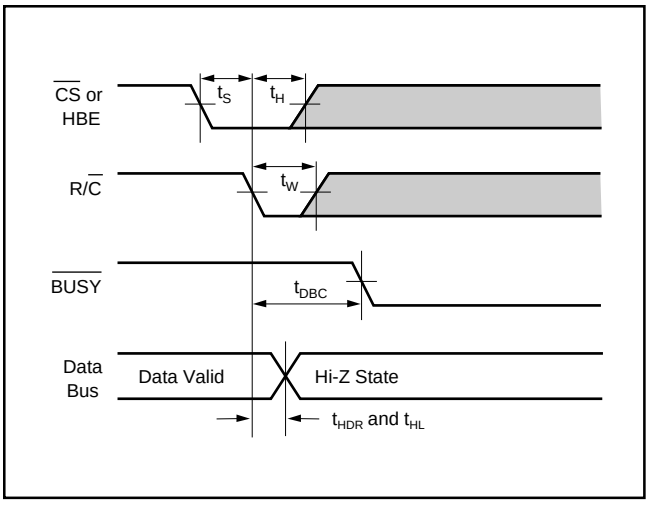


FIGURE 8. Conversion Start Timing.

Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain maximum system accuracy, both should be well isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the ADS7800.

The V_S pins (23 and 24) should be connected together and bypassed with a parallel combination of a 6.8µF tantalum capacitor and a 0.1µF ceramic capacitor located close to the converter to obtain noise-free operation. (See Figure 2.) The $-V_S$ pin 22 should be bypassed with a 1µF tantalum capacitor, again as close as possible to the ADS7800.

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the

converter if at all possible. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the ADS7800, which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the ADS7800 as possible.

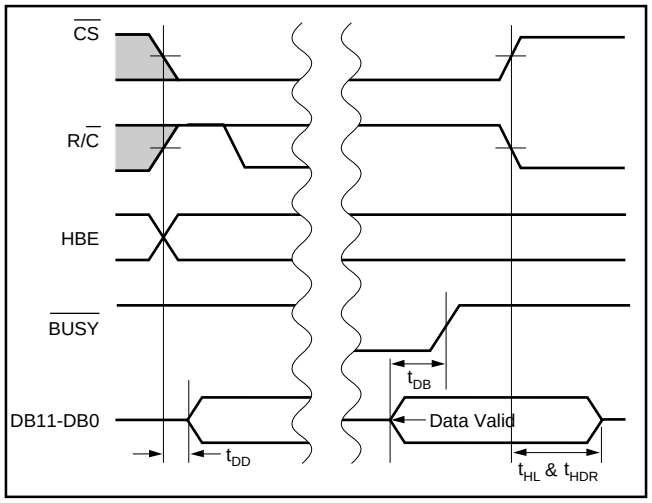


FIGURE 9. Read Cycle Timing.

REFERENCE BYPASS

Pin 3 (REF) should be bypassed with a 22µF to 47µF tantalum capacitor. A rated working voltage of 2V or more is acceptable here. This pin is used to enhance the system accuracy of the internal reference circuit, and is not recommended for driving external signals. If there are important system reasons for using the ADS7800 reference externally, the output of pin 3 must be appropriately buffered.

"HOT SOCKET" PRECAUTION

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the ADS7800 may "Latch Up" and draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to power the ADS7800 only after it has been socketed.

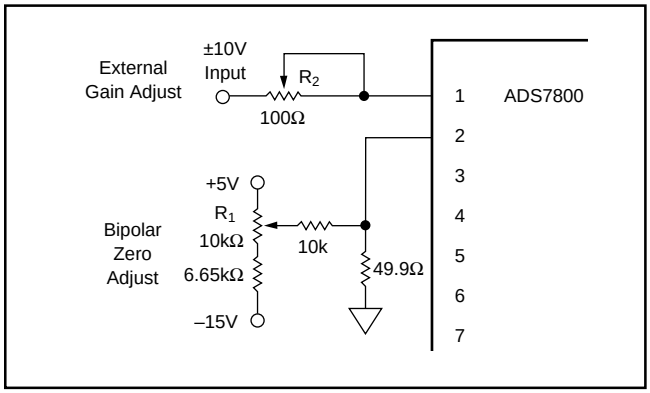


FIGURE 10. ±10V Range With External Trims.

MINIMIZING "GLITCHES"

Coupling of external transients into an A/D converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using the ADS7800. These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the ADS7800 has an internal sample/hold function, the signal that puts it into the hold state (R/$\overline{C}$ going LOW) is critical, as it would be on any sample/hold amplifier. The R/$\overline{C}$ falling edge should be sharp and have minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitching the ADS7800 while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/$\overline{C}$, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).

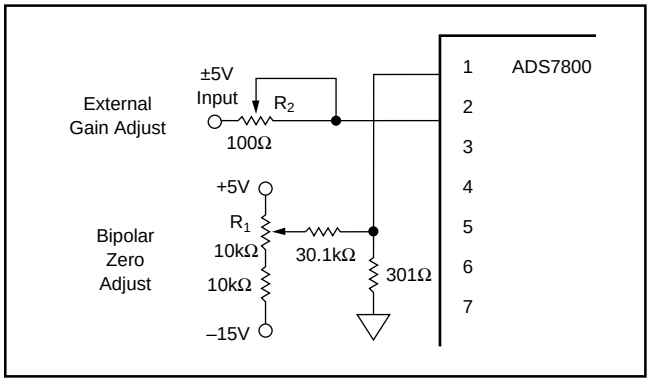


FIGURE 11. ±5V Range With External Trims.

Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the ADS7800. If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{BUSY}$ output can be used to enable the buffer.

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{C}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the ADS7800.

Finally, in multiplexed systems, the timing on when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{C}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the ADS7800 input. Whenever possible, it is safer to wait until the conversion is completed before switching the multiplexer. The extremely fast acquisition time and conversion time of the ADS7800 make this practical in many applications.

INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range Defined As:		±10V	±5V
Analog Input Connected to Pin		1	2
Pin Connected to GND		2	1
One Least Significant Bit (LSB)	FSR/2^{12}	20V/2^{12}	10V/2^{12}
		4.88mV	2.44mV
OUTPUT TRANSITION VALUES			
FFE_H to FFF_H	+Full Scale	+10V–3/2LSB	+5V–3/2LSB
		+9.9927V	+4.9963V
$7FF_H$ to 800_H	Mid Scale	0V–1/2LSB	0V–1/2LSB
	(Bipolar Zero)	–2.44mV	–1.22mV
000_H to 001_H	–Full Scale	–10V+1/2LSB	–5V+1/2LSB
		–9.9976V	–4.9988V

TABLE IV. Input Voltages, Transition Values, and LSB Values.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7800AH	NRND	CDIP SB	JDN	24	1	TBD	Call TI	Call TI
ADS7800AH-BI	OBSOLETE	CDIP SB	JD	24		TBD	Call TI	Call TI
ADS7800BH	NRND	CDIP SB	JDN	24	1	TBD	Call TI	Call TI
ADS7800BH-BI	OBSOLETE	CDIP SB	JD	24		TBD	Call TI	Call TI
ADS7800JP	ACTIVE	PDIP	NT	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7800JPG4	ACTIVE	PDIP	NT	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7800JU	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7800JU/1K	ACTIVE	SOIC	DW	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7800JU/1KE4	ACTIVE	SOIC	DW	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7800JU/1KG4	ACTIVE	SOIC	DW	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7800JUE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7800KP	ACTIVE	PDIP	NT	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7800KPG4	ACTIVE	PDIP	NT	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ADS7800KU	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS7800KUE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

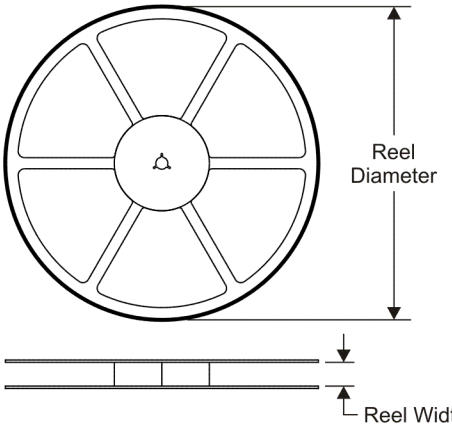
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

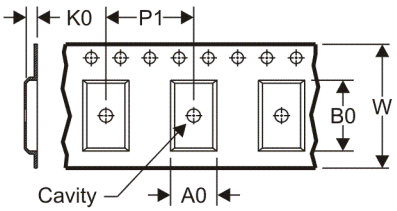
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

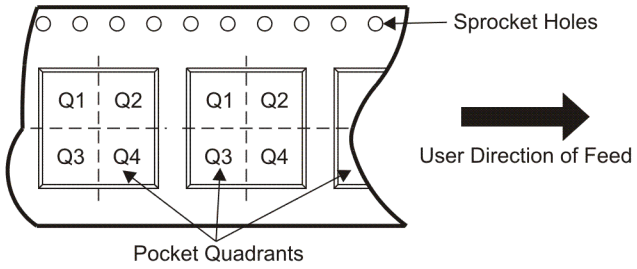


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

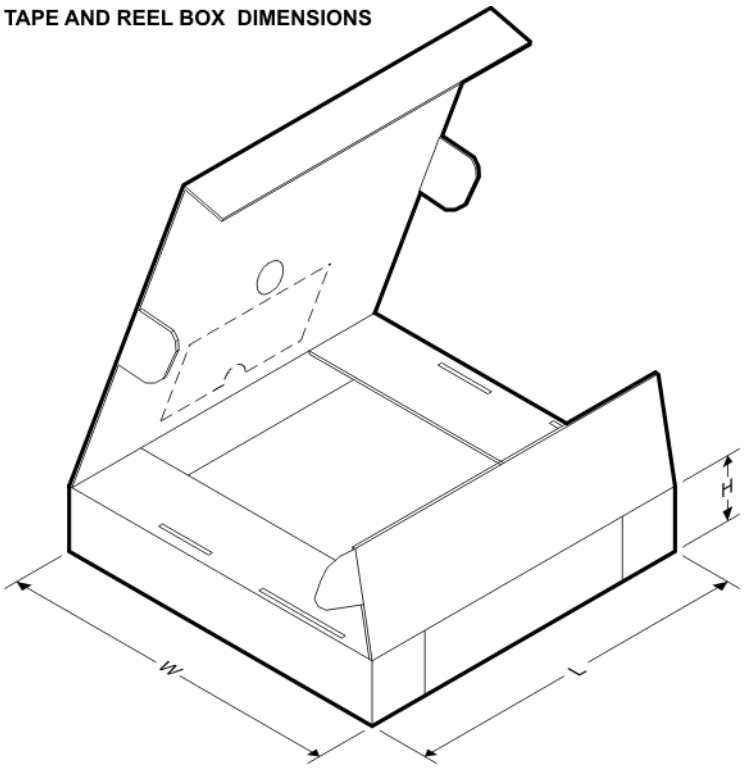
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7800JU/1K	SOIC	DW	24	1000	330.0	24.4	10.85	15.8	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

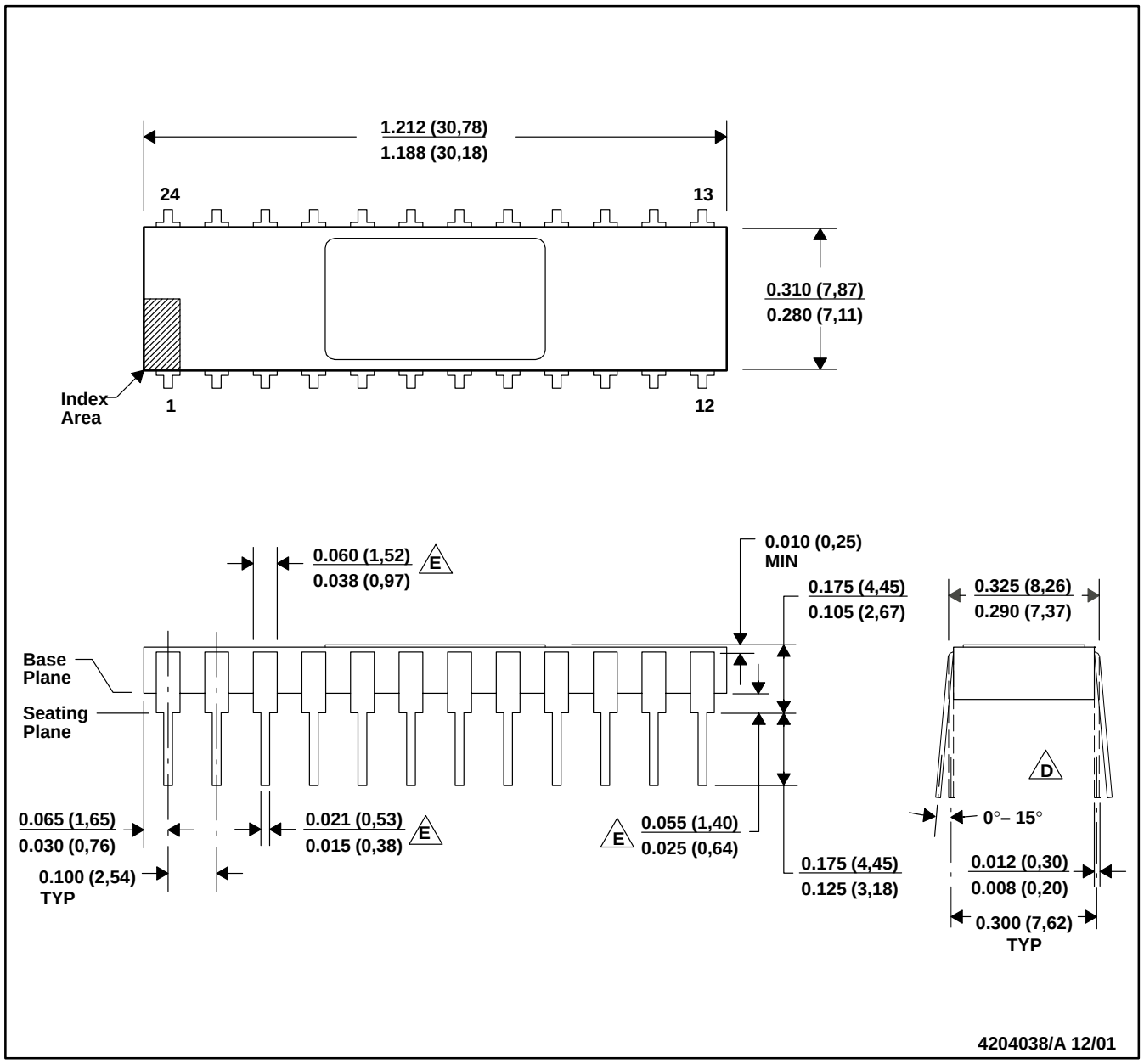


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7800JU/1K	SOIC	DW	24	1000	346.0	346.0	41.0

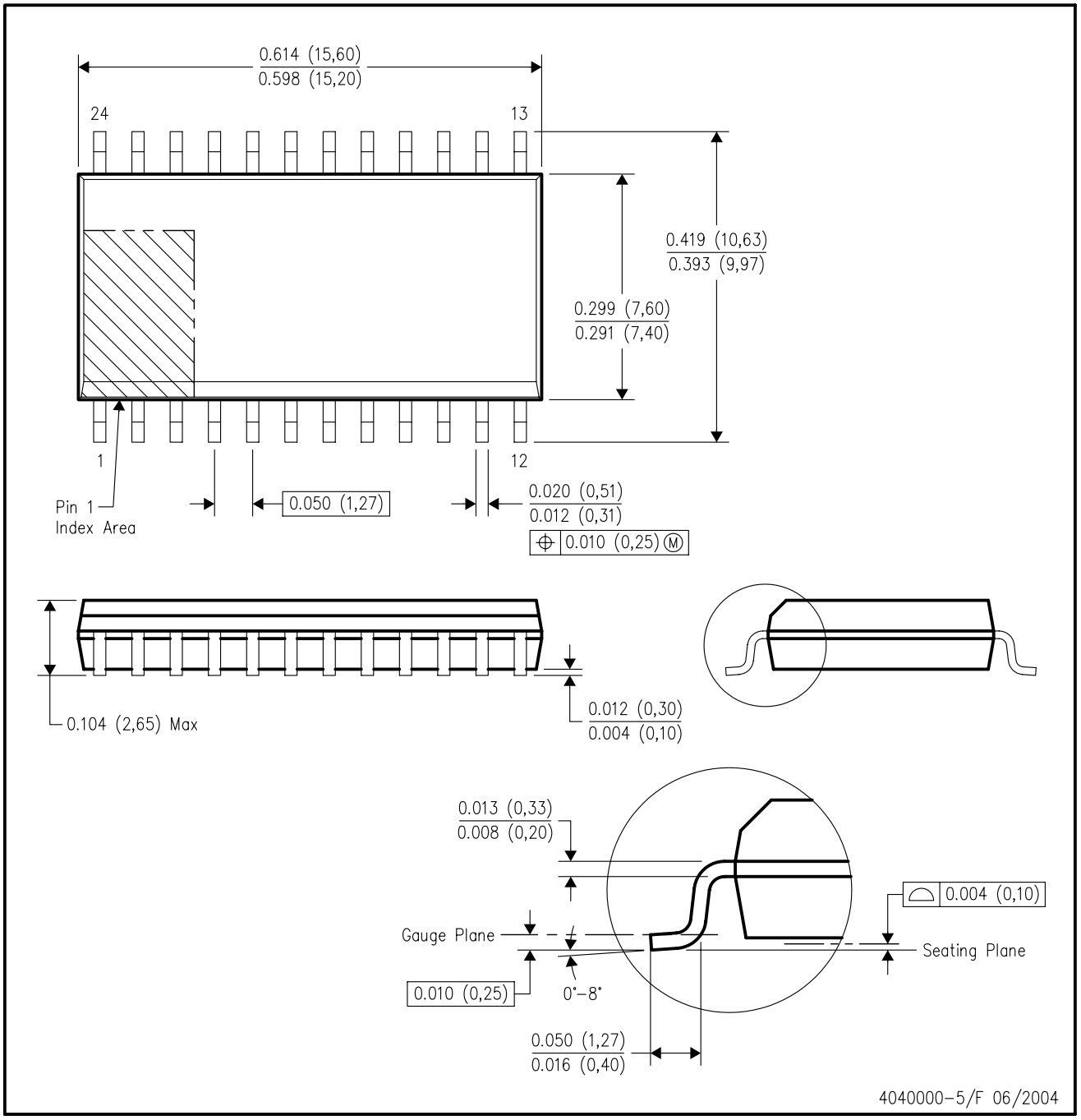
MCDI046 – JANUARY 2002

JDN (R–CDIP–T24) **CERAMIC SIDE-BRAZE DUAL-IN-LINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads within 0.005 (0.13) radius of true position (TP) at gage plane with maximum material condition and unit installed.
D. The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
E. Outlines on which the seating plane is coincident with the plane (standoff = 0), terminal lead standoffs are not required, and lead shoulder may equal lead width along any part of the lead above the seating/base plane.
F. A visual index feature must be located within the cross-hatched area.

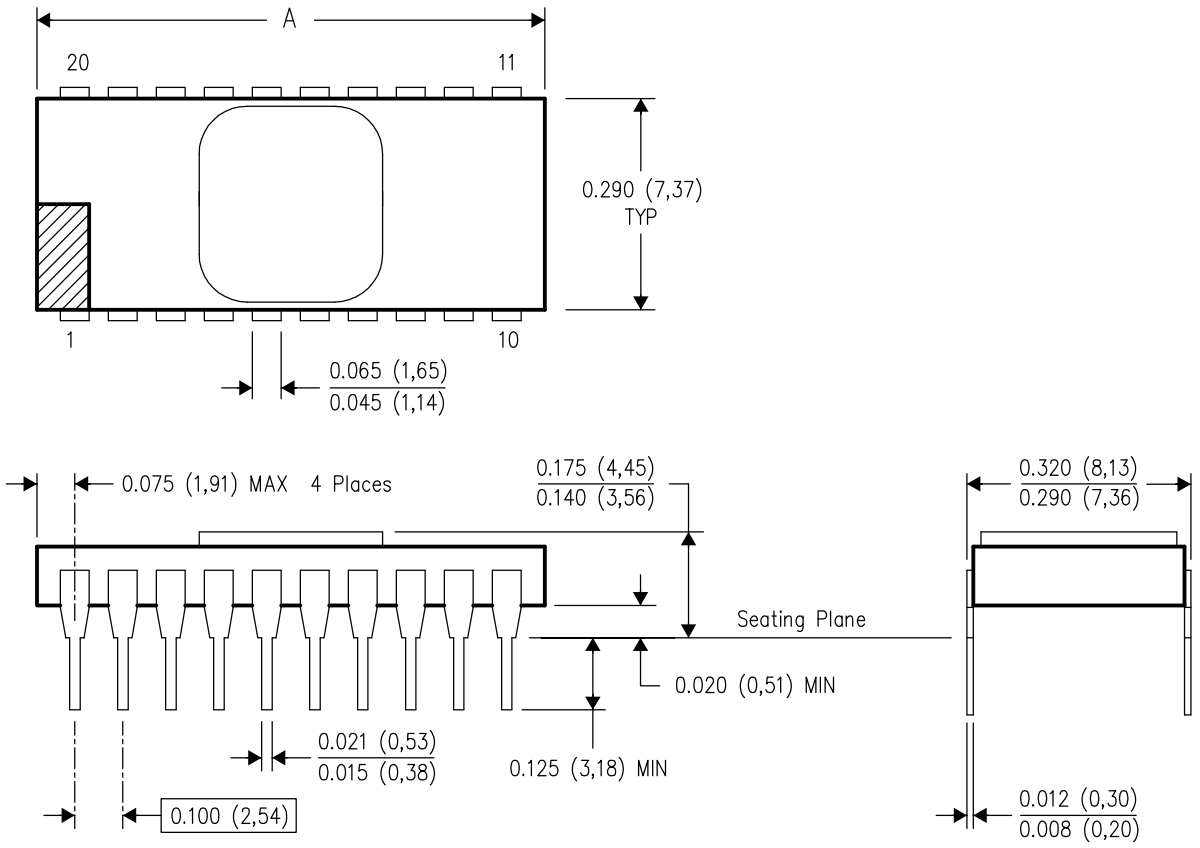
DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

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