Octal, 14-Bit, Low-Power, ±15-V Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Bipolar Output: ±15 V, Up to ±16.5 V**
- **Unipolar Output: 0 V to +18 V**
- **14-Bit Resolution**
- **Low Power: 20.6 mW/Ch**
- **Relative Accuracy: 1 LSB Max**
- **Low Zero-Code/Gain Error**
  - **Before User Calibration: ±2 LSB Max**
  - **After User Calibration: ±1 LSB Max**
- **Flexible System Calibration**
- **Low Glitch**
- **Settling Time: 10 μs**
- **Channel Monitor Output**
- **Programmable Offset**
- **SPI™: Up to 50-MHz, 1.8-V/3-V/5-V Logic**
- **Schmitt Trigger Inputs**
- **Daisy-Chain Mode**
- **Packages: QFN-48 (7x7mm), TQFP-64 (10x10mm)**

APPLICATIONS

- **Automatic Test Equipment**
- **PLC and Industrial Process Control**
- **Communications**

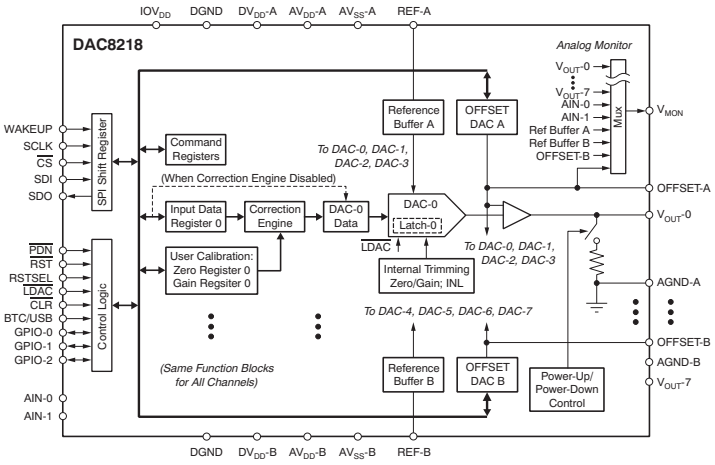
DESCRIPTION

The DAC8218 is a low-power, octal, 14-bit digital-to-analog converter (DAC). The output can be a bipolar ±15-V voltage when operating from a dual ±16.5V power supply, or a unipolar 0-V to +18-V voltage when operating from a +20-V power supply. This DAC provides low-power operation, good linearity, and low glitch over the specified temperature range of –40°C to +105°C. This device is trimmed in manufacturing and has very low zero-code and gain error. In addition, system level calibration can be performed to achieve ±1 LSB zero-code and gain error over entire signal chain. The output range can be offset by properly setting the DAC offset register.

The DAC8218 features a standard, high-speed serial peripheral interface (SPI) at up to 50 MHz and 1.8-V, 3-V, and 5-V logic compatible, to communicate with a DSP or microprocessor. The input data of the device are double-buffered. An asynchronous load input (LDAC) transfers data from the DAC data register to the DAC latch. The asynchronous CLR input sets the output of all eight DACs to AGND. The V_{MON} pin is a monitor output that connects to the individual analog outputs and two external inputs through a multiplexer (mux).

The DAC8218 is pin-to-pin compatible with the DAC8718 (16-bit) and the DAC7718 (12-bit).

PRODUCT PREVIEW



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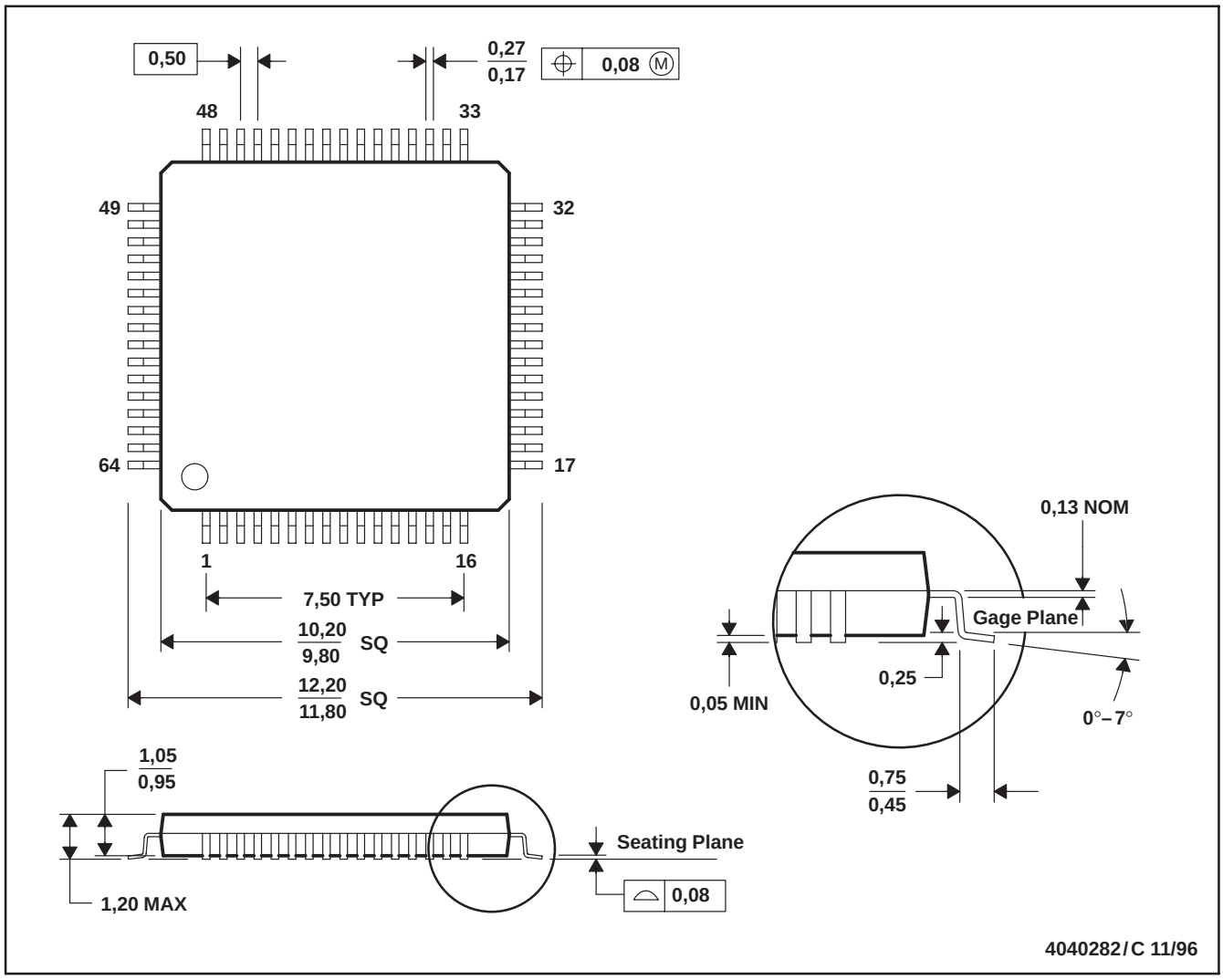
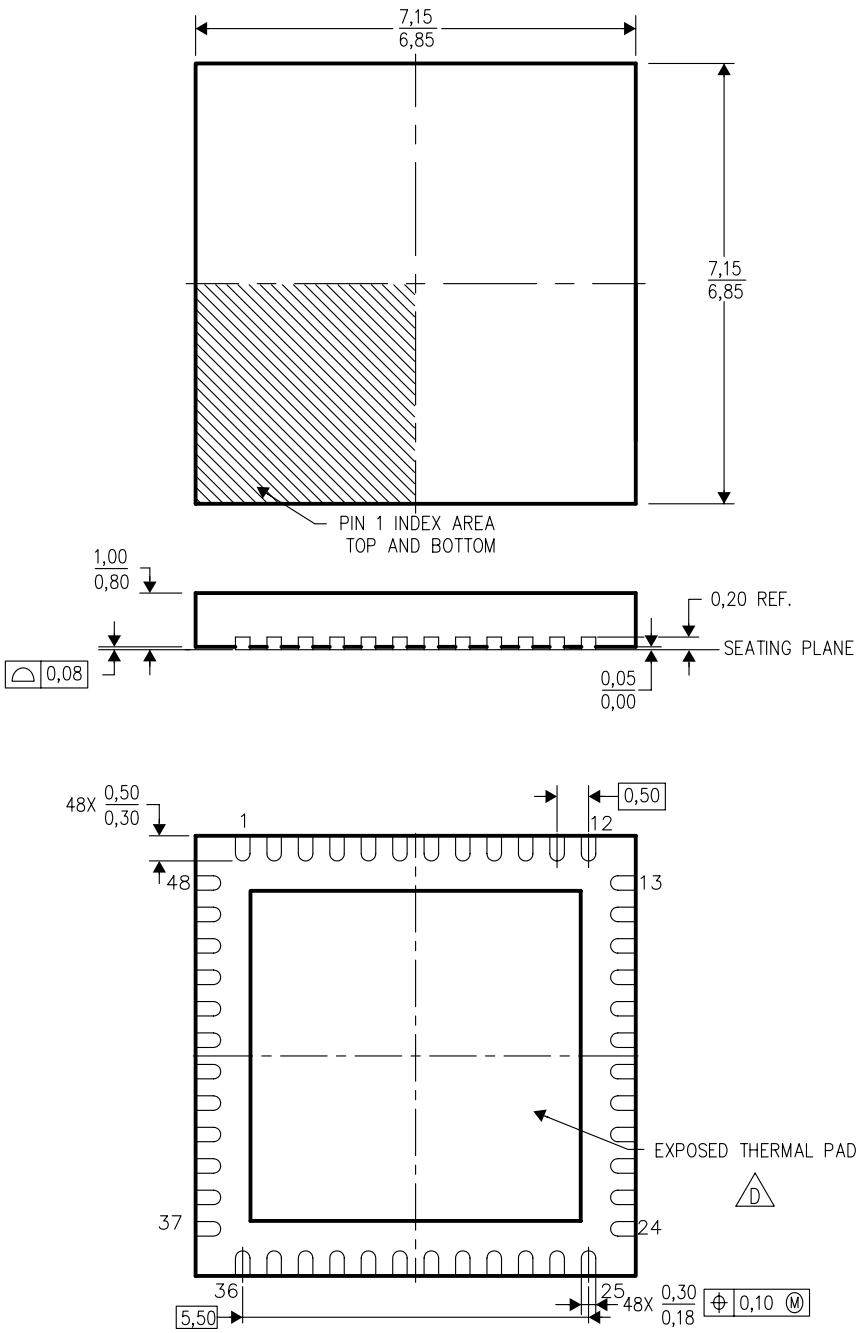
PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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