ISOLATED RS-485 PROFIBUS TRANSCEIVER

FEATURES

- 4000-V_{PEAK} Isolation
- Bus-Pin ESD Protection
  - 16 kV HBM Between Bus Pins and GND2
  - 6 kV HBM Between Bus Pins and GND1
- Meets or Exceeds the Requirements of EN 50170 and TIA/EIA-485
- Signaling Rates up to 40 Mbps
- Differential Output Exceeds 2.1 V (54 Ω Load)
- Low Bus Capacitance – 10 pF (MAX)
- 50 kV/μs Typical Transient Immunity
- Failsafe Receiver for Bus Open, Short, Idle
- 3.3-V Inputs are 5-V Tolerant

APPLICATIONS

- Profibus
- Factory Automation
- Networked Sensors
- Motor/Motion Control
- HVA and Building Automation Networks
- Networked Security Stations

DESCRIPTION

The ISO1176 is an isolated differential line transceiver designed for use in PROFIBUS applications. The device is ideal for long transmission lines since the ground loop is broken to provide for operation with a much larger common mode voltage range. The symmetrical isolation barrier of each device is tested to provide 2500 Vrms of isolation between the line transceiver and the logic level interface.

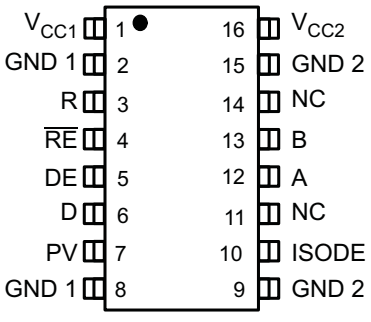
The galvanically isolated differential bus transceiver is an integrated circuit designed for bi-directional data communication on multipoint bus-transmission lines. The transceiver combines a galvanically isolated differential line driver and differential input line receiver. The driver has an active-high enable with isolated enable-state output on the ISODE pin (pin 10) to facilitate direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or Vcc2 = 0.

The PV pin (pin 7) is provided as a full-chip enable option. All device outputs become high impedance when a logic low is applied to the PV pin. For more information, see the function tables in the device information section.

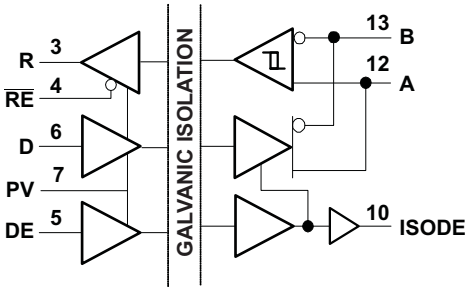
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. The ISO1176 can significantly reduce the risk of data corruption and damage to expensive control circuits.

The device is characterized for operation over the ambient temperature range of –40°C to 85°C.

DW PACKAGE
(TOP VIEW)



ISO1176
function diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)

					VALUE	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)				–0.5 to 7	V
V_O	Voltage at any bus I/O terminal				–9 to 14	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal				–0.5 to 7	V
I_O	Receiver output current				±10	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus pins to GND1	±6	kV
				Bus pins to GND2	±16	
				All pins	±4	
		Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1	
		Machine model	ANSI/ESDS5.2-1996	All pins	±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Logic side supply voltage, V_{CC1} (with respect to GND1)		3.15		5.5	V
	Bus side supply voltage, V_{CC2} (with respect to GND2)		4.75		5.25	
V_{CM}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	PV, $\overline{RE}$	2		V_{CC1}	V
		D, DE	0.7 V_{CC1}			
V_{IL}	Low-level input voltage	PV, $\overline{RE}$	0		0.8	V
		D, DE			0.3 V_{CC1}	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
I_O	Output current	Driver	–70		70	mA
		Receiver	–8		8	
T_J	Operating junction temperature		–40		150	Ω

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Logic side RMS supply current	3 V	DE at 0 V		4	6	mA
			DE at V_{CC1}, 2 Mbps		5		
			DE at V_{CC1}, 25 Mbps		6		
		5.5 V	DE at 0 V		7	10	mA
			DE at V_{CC1}, 2 Mbps		8		
			DE at V_{CC1}, 25 Mbps		11		
I_{CC2}	Bus side RMS supply current	5.25 V	DE at 0 V		15	18	mA
			DE at V_{CC1}, 2 Mbps, 54 Ω load		70		
			DE at V_{CC1}, 25 Mbps, 54 Ω load		75		

ISODE-PIN ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{CC2} – 0.8	4.6		V
		I_{OH} = –20 µA	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.2	0.4	V
		I_{OL} = 20 µA		0	0.1	

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OD}	Open-circuit differential output voltage	$\|V_A – V_B\|$, Figure 1		1.5		V_{CC2}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	See Figure 2 and Figure 6		2.1			V
		Common-mode loading with V_{test} from –7 V to 12 V, See Figure 3		2.1			
$\|\Delta V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	R_L = 54 Ω, See Figure 4 andFigure 5		–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 54 Ω, See Figure 4 and Figure 5		2		3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			–0.2		0.2	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				0.5		
$V_{OD(RING)}$	Differential output voltage over and under shoot	See Figure 6 and Figure 10				10%	$V_{OD(pp)}$
$V_{I(HYS)}$	Input voltage hysteresis	See Figure 7			150		mV
I_I	Input current	D, DE at 0 V or V_{CC1}		–10		10	µA
		PV[1] at 0 V or V_{CC1}				120	
$I_{O(OFF)}$	Output current with power off	V_{CC} ≤ 2.5 V		See Receiver input current			
I_{OZ}	High impedance state output current	DE at 0 V					
$I_{OS(P)}$	Peak short-circuit output current	DE at V_{CC}, See Figure 8 and Figure 9	V_{OS} = –7 V to 12 V	–250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current		V_{OS} = 12 V, D at GND1			135	
			V_{OS} = –7 V, D at V_{CC1}	–135			
C_{OD}	Differential output capacitance			See Receiver C_{IN}			
CMTI	Common-mode transient immunity	See Figure 20		25			kV/µs

(1) The PV pin has a 50 kΩ pull-up resistor and leakage current depends on supply voltage.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 5 V V_{CC2} at 5 V	See Figure 10			35	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				2	5	ns
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 3.3 V V_{CC2} at 5 V				40	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				2	5	ns
t_r	Differential output signal rise time			2	3	7.5	ns
t_f	Differential output signal fall time			2	3	7.5	ns
t_{pDE}	DE to ISODE prop delay		See Figure 14			30	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew		See Figure 11			1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output		C_L = 50 pF, $\overline{RE}$ at 0 V, See Figure 12 and Figure 13			80	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-to- high-impedance output					80	ns
$\lvert t_{p(AZL)} - t_{p(BZH)} \rvert$ $\lvert t_{p(AZH)} - t_{p(BZL)} \rvert$	Enable skew time				0.55	1.5	ns
$t_{(CFB)}$	Time from application of short-circuit to current foldback		See Figure 9		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown		T_A = 25°C, See Figure 9	100			µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold		See Figure 15	I_O = –8 mA		–80	–10	mV
$V_{IT(–)}$	Negative-going differential input voltage threshold			I_O = 8 mA	–200	–120		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					40		mV
V_{OH}	High-level output voltage	V_{CC1} at 3.3 V and V_{CC2} at 5 V	V_{ID} = 200 mV, See Figure 15	I_{OH} = –8 mA	V_{CC1} –0.4	3		V
				I_{OH} = –20 µA	V_{CC1} –0.1	3.3		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 15	I_{OL} = 8 mA		0.2	0.4	V
				I_{OL} = 20 µA		0	0.1	
V_{OH}	High-level output voltage	V_{CC1} at 5 V and V_{CC2} at 5 V	V_{ID} = 200 mV, See Figure 15	I_{OH} = –8 mA	V_{CC1} –0.8	4.6		V
				I_{OH} = –20 µA	V_{CC1} –0.1	5		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 15	I_{OL} = 8 mA		0.2	0.4	V
				I_{OL} = –20 µA		0	0.1	
I_A, I_B	Bus pin input current		V_I = –7 V or 12 V, Other input = 0 V	V_{CC} = 4.75 V or 5.25 V	–160		200	µA
$I_{A(OFF)}$ $I_{B(OFF)}$				V_{CC2} = 0 V				
I_I	Receiver enable input current		$\overline{RE}$ = 0 V		–50		50	µA
I_{OZ}	High-impedance state output current		$\overline{RE}$ = V_{CC1}		–1		1	µA
R_{ID}	Differential input resistance		A, B		48			kΩ
C_{ID}	Differential input capacitance		Test input signal is a 1.5 MHz sine wave with 1 V_{pp} amplitude , C_D is measured across A and B			7	10	pF
C_{MR}	Common mode rejection		See Figure 19			4		V

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 5 V, V_{CC2} at 5 V	See Figure 16			50	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				2	5	
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 3.3 V, V_{CC2} at 5 V				55	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				2	5	
t_r	Output signal rise time				2	4	ns
t_f	Output signal fall time				2	4	
t_{pZH}	Propagation delay time, high-impedance-to-high-level output		DE at V_{CC1}, See Figure 17		13	25	ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output				13	25	
t_{pZL}	Propagation delay time, high-impedance-to-low-level output		DE at V_{CC}, See Figure 18		13	25	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output				13	25	

PARAMETER MEASUREMENT INFORMATION

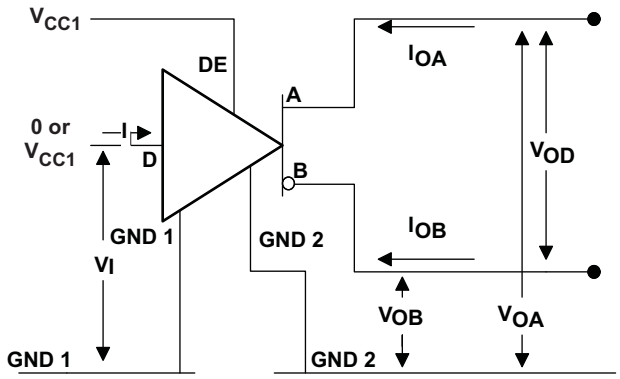


Figure 1. Open Circuit Voltage Test Circuit

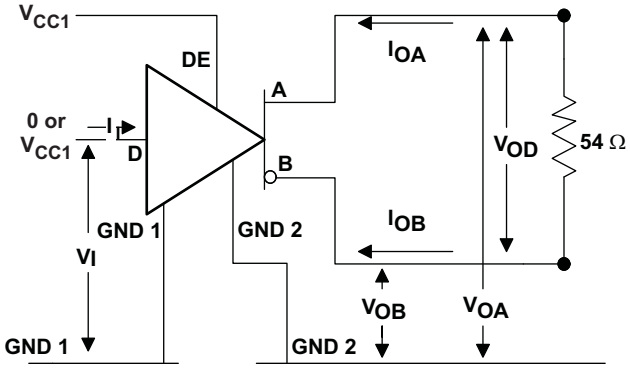


Figure 2. V_{OD} Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

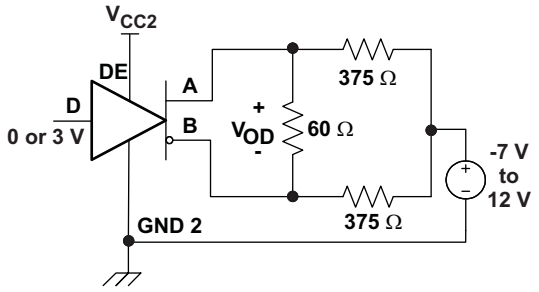


Figure 3. Driver V_{OD} with Common-mode Loading Test Circuit

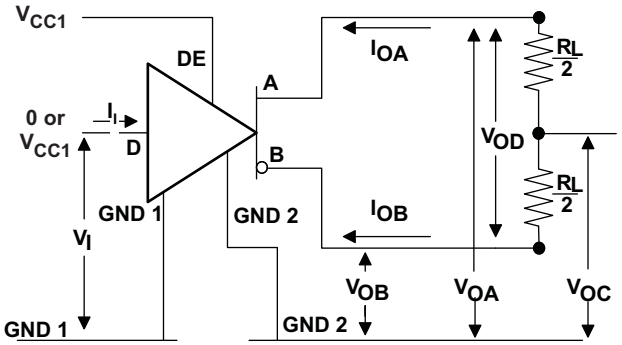


Figure 4. Driver V_{OD} and V_{OC} Without Common-Mode Loading Test Circuit

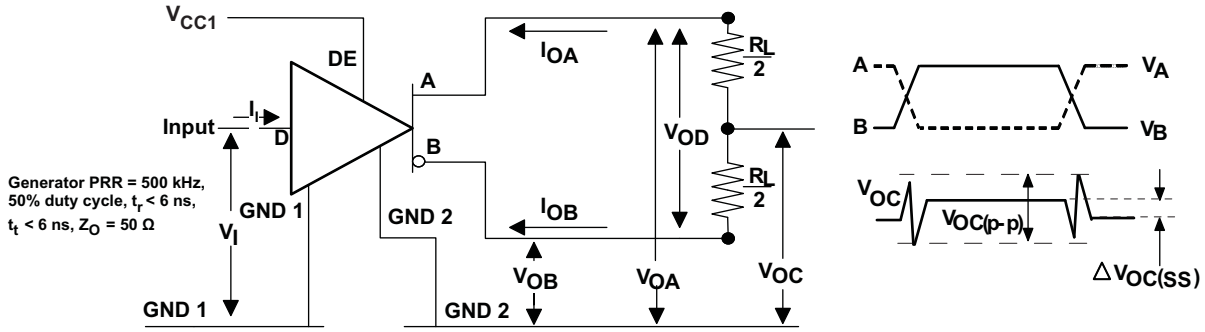


Figure 5. Steady-State Output Voltage Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

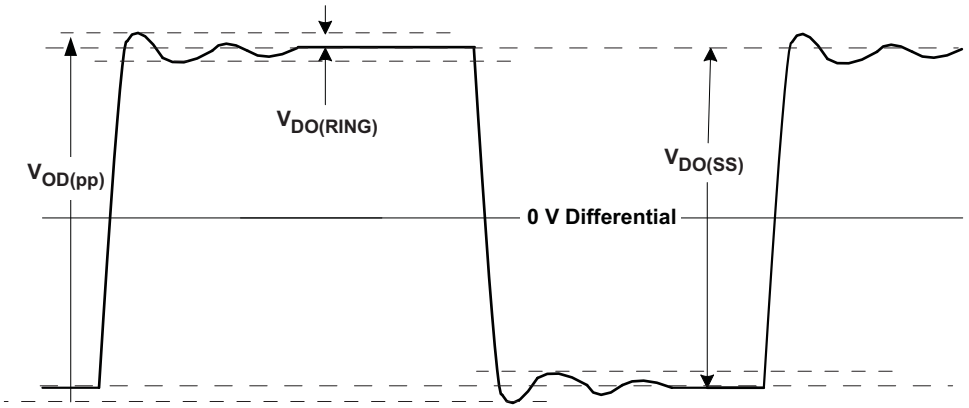


Figure 6. $V_{OD(RING)}$ Waveform and Definitions

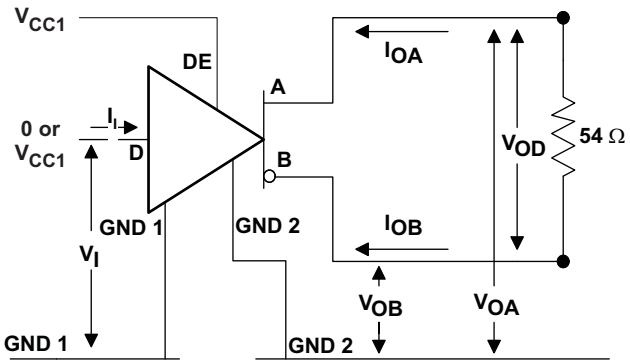


Figure 7. Input Voltage Hysteresis Test Circuit

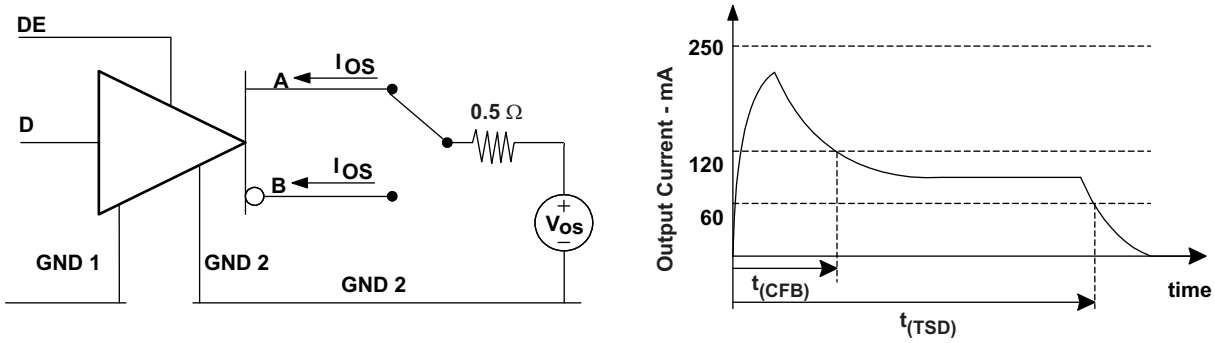


Figure 8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0)

PARAMETER MEASUREMENT INFORMATION (continued)

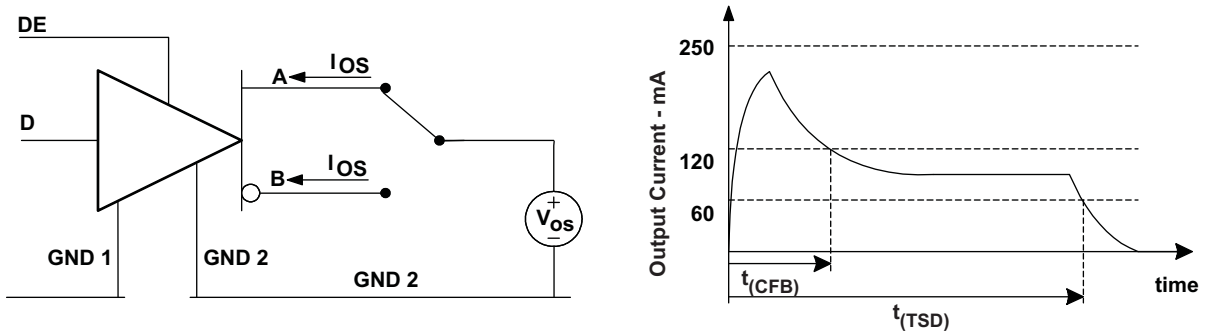


Figure 9. $I_{OS(SS)}$ Steady State Short Circuit Output Current Test Circuit

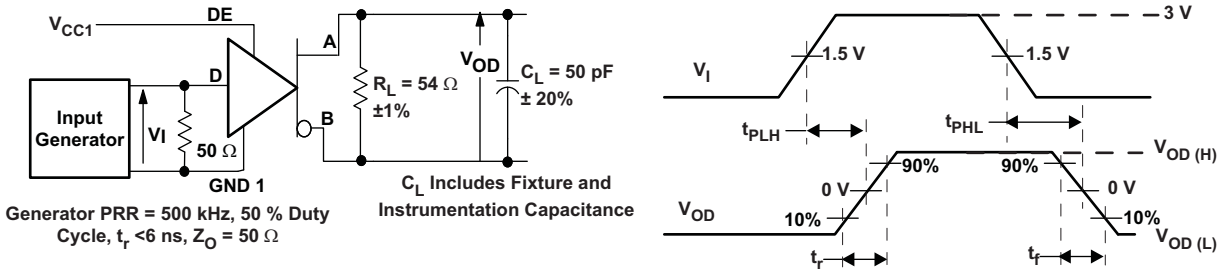


Figure 10. Driver Switching Test Circuit and Waveforms

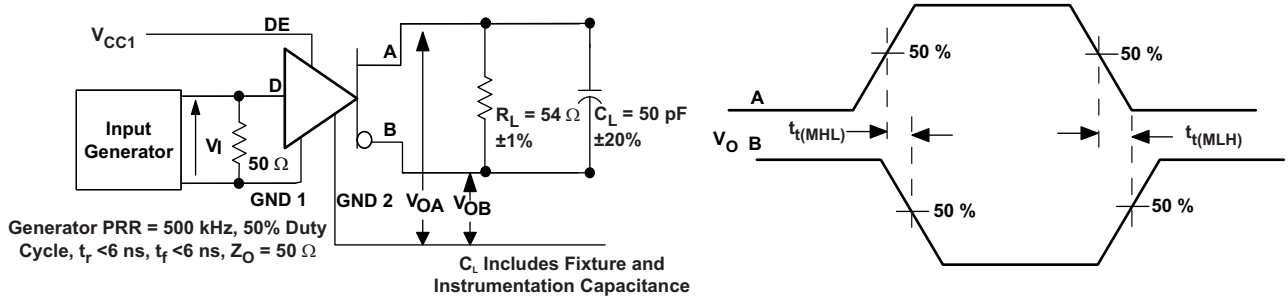


Figure 11. Driver Output Transition Skew Test Circuit and Waveforms

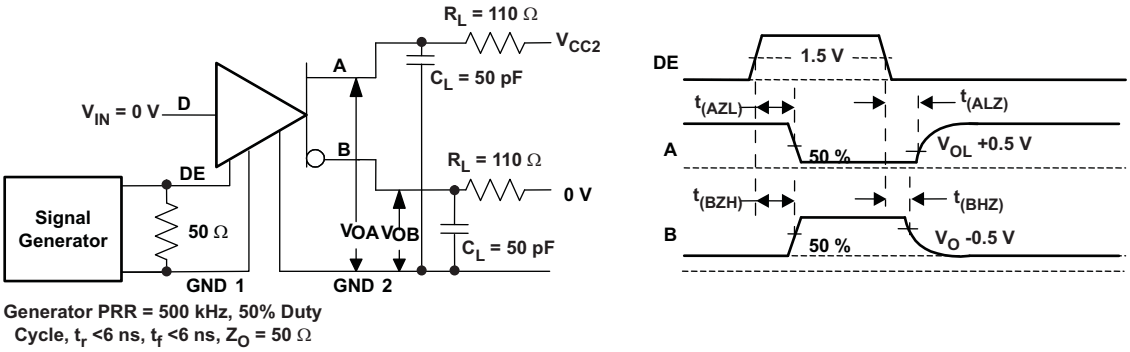


Figure 12. Driver Enable/Disable Test, D at Logic Low Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

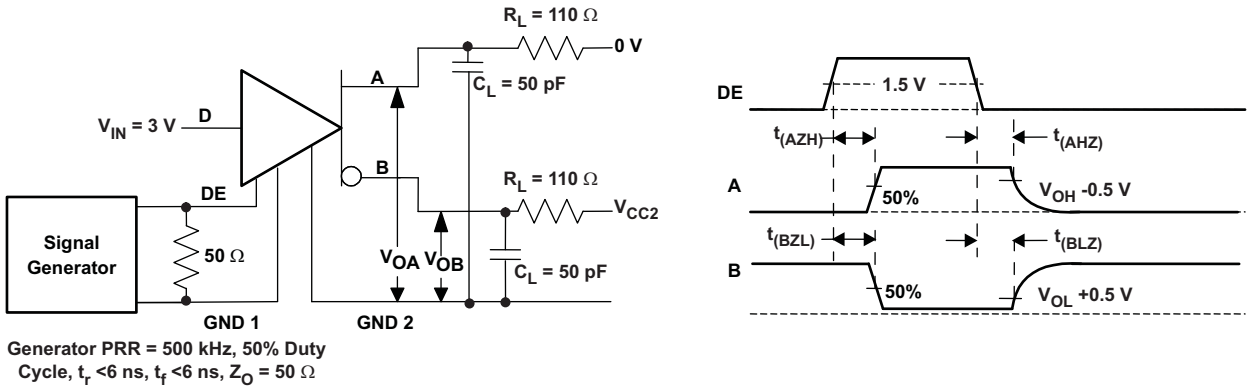


Figure 13. Driver Enable/Disable Test, D at Logic High Test Circuit and Waveforms

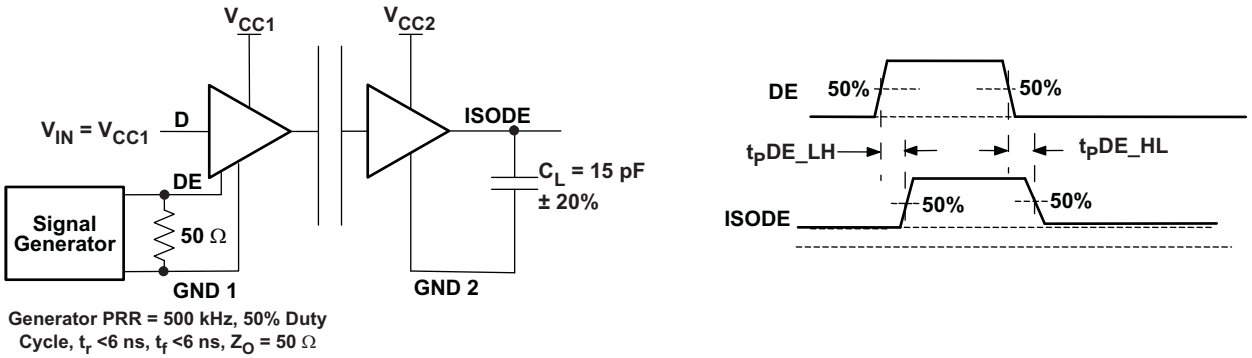


Figure 14. DE to ISODE Prop Delay Test Circuit and Waveforms

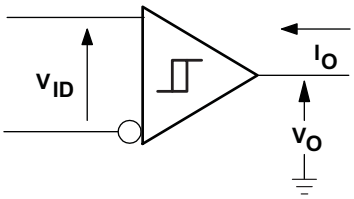


Figure 15. Receiver DC Parameter Definitions

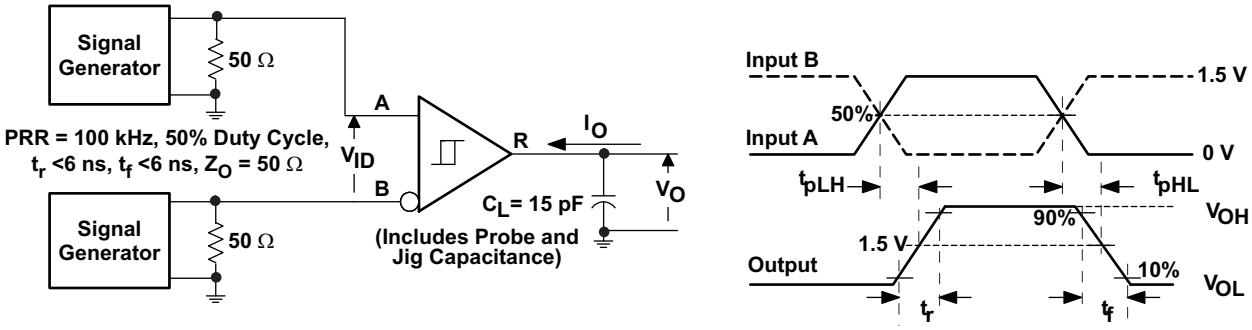


Figure 16. Receiver Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

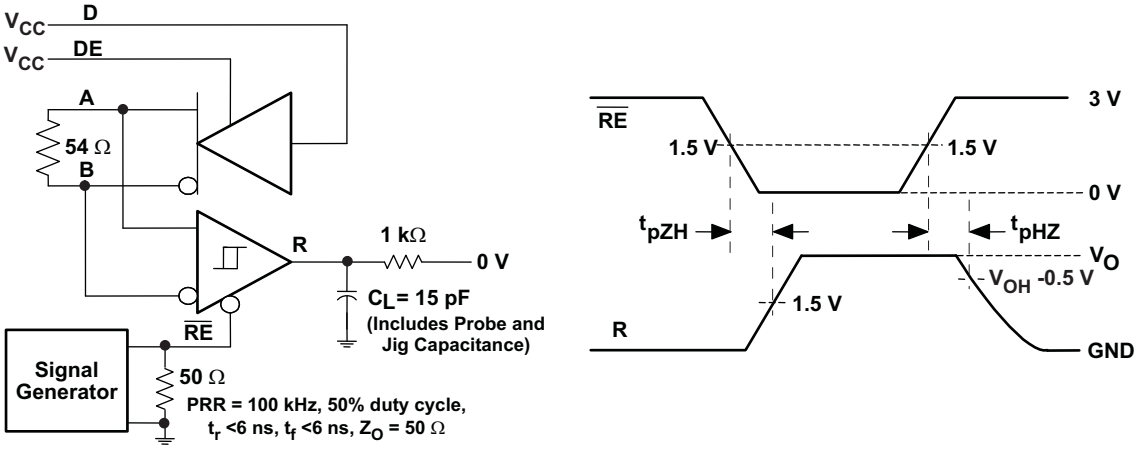


Figure 17. Receiver Enable Test Circuit and Waveforms, Data Output High

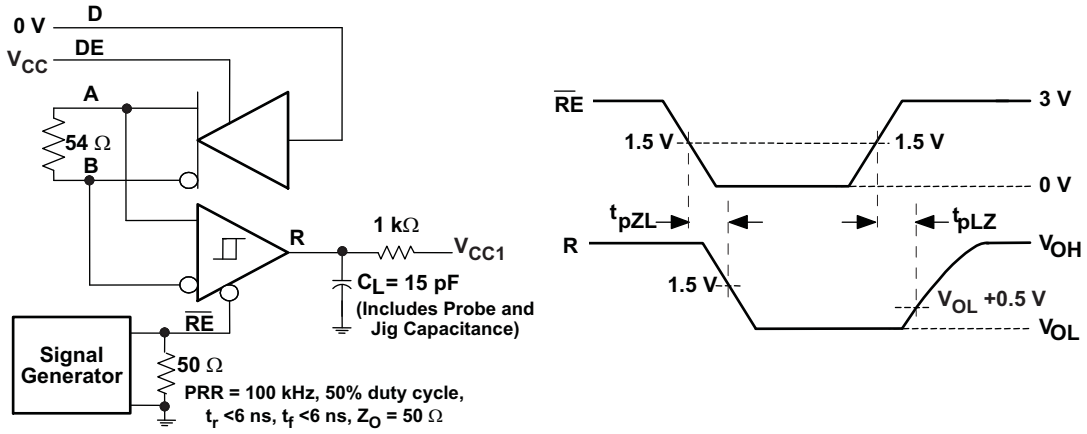


Figure 18. Receiver Enable Test Circuit and Waveforms, Data Output Low

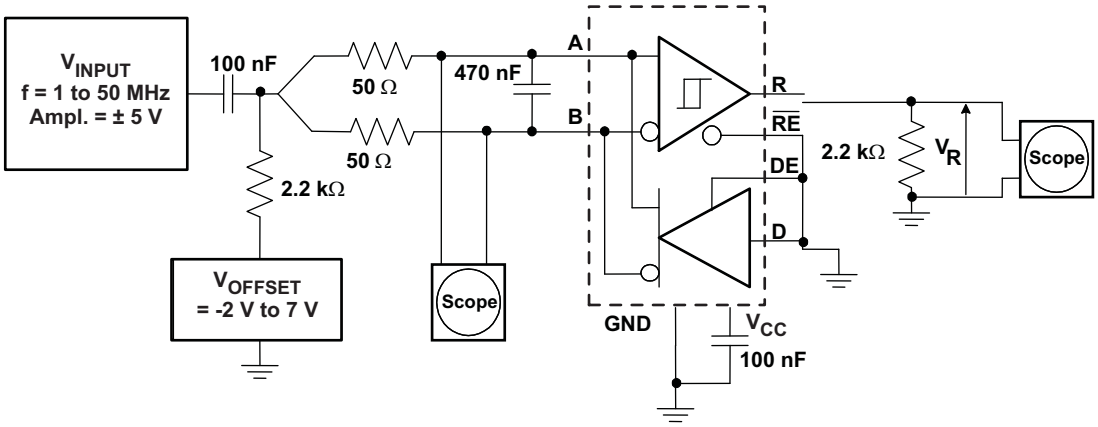


Figure 19. Common-Mode Rejection Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

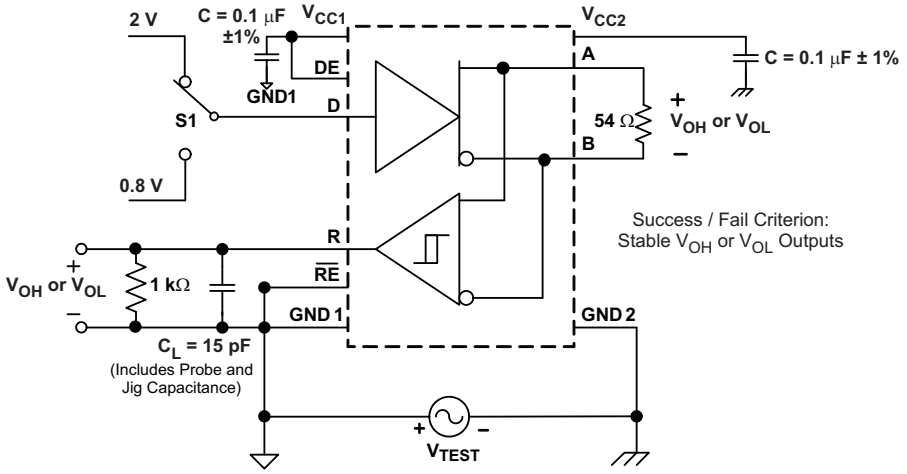


Figure 20. Common-Mode Transient Immunity Test Circuit

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
LOAD CURRENT

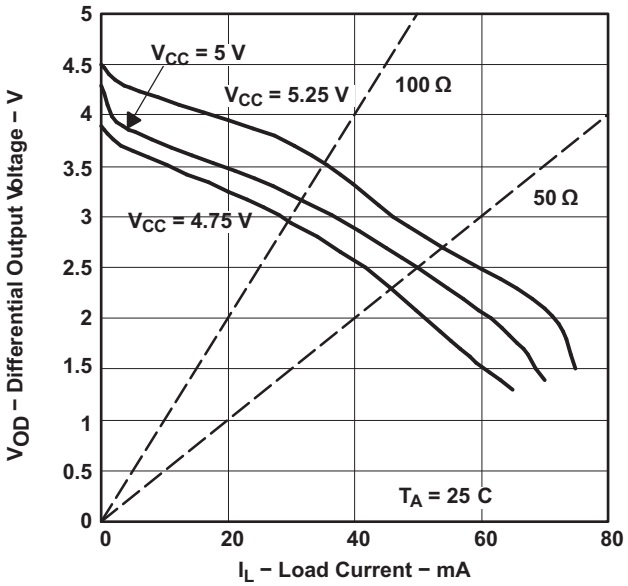


Figure 21.

RMS SUPPLY CURRENT
vs
SIGNALING RATE

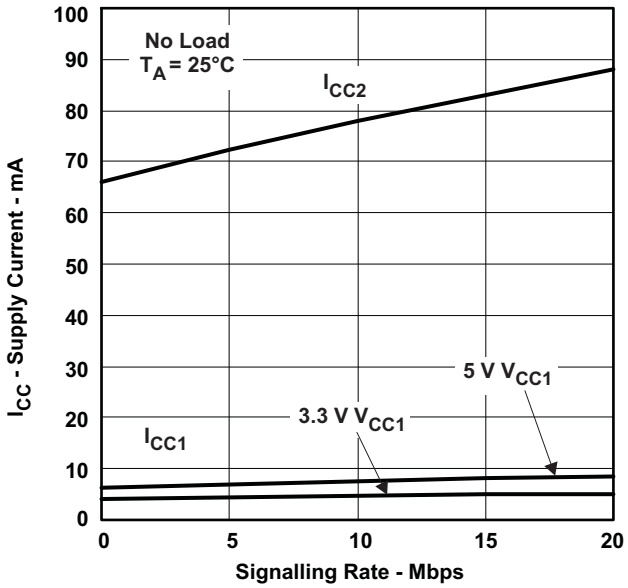


Figure 22.

DRIVER OUTPUT TRANSITION SKEW
vs
FREE-AIR TEMPERATURE

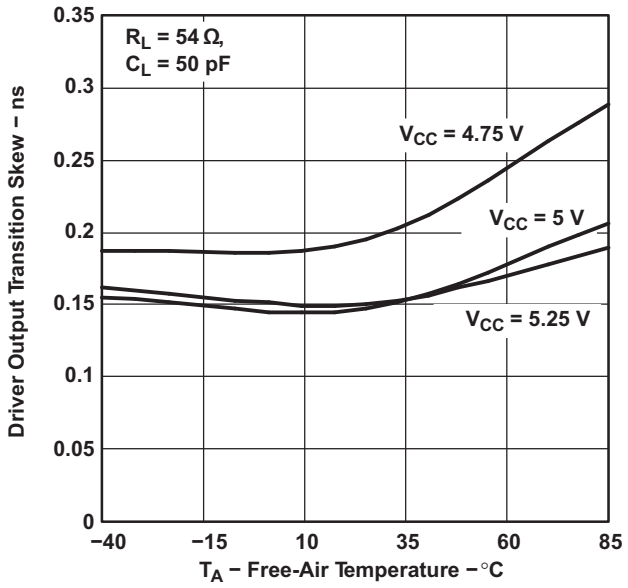


Figure 23.

DRIVER RISE, FALL TIME
vs
FREE-AIR TEMPERATURE

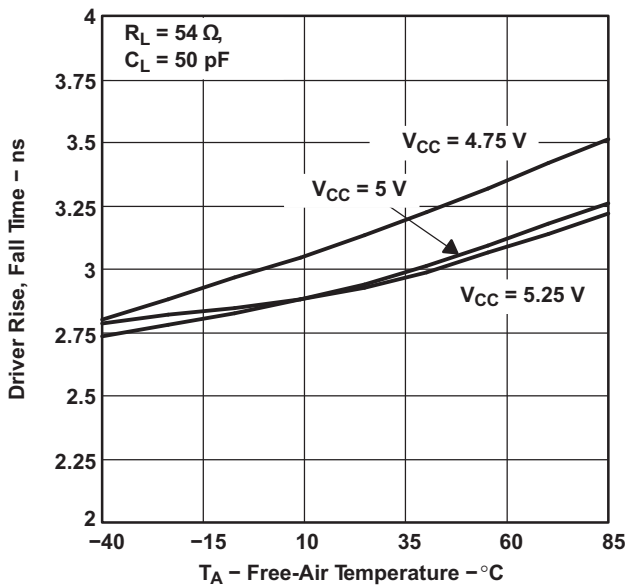


Figure 24.

TYPICAL CHARACTERISTICS (continued)

DRIVER ENABLE SKEW
vs
FREE-AIR TEMPERATURE

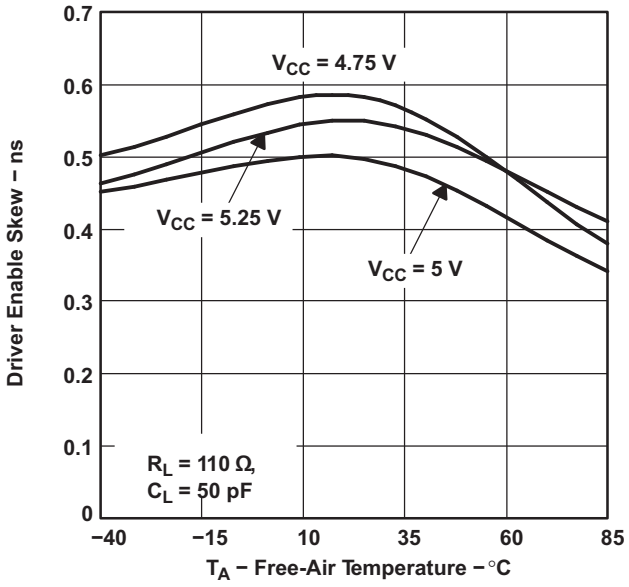


Figure 25.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

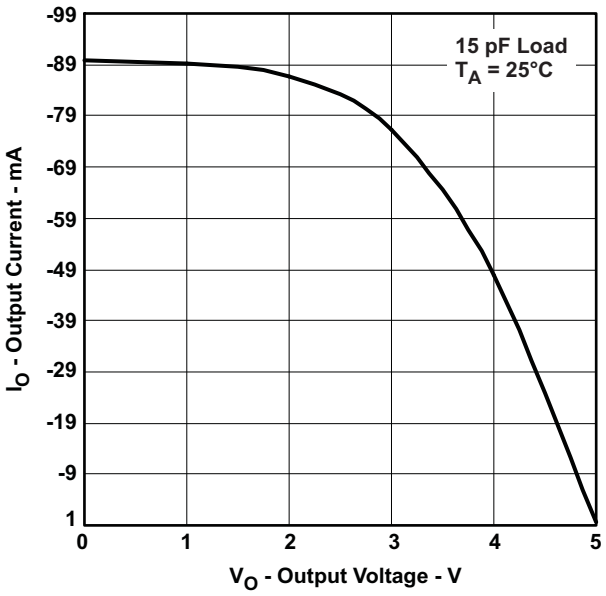


Figure 26.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

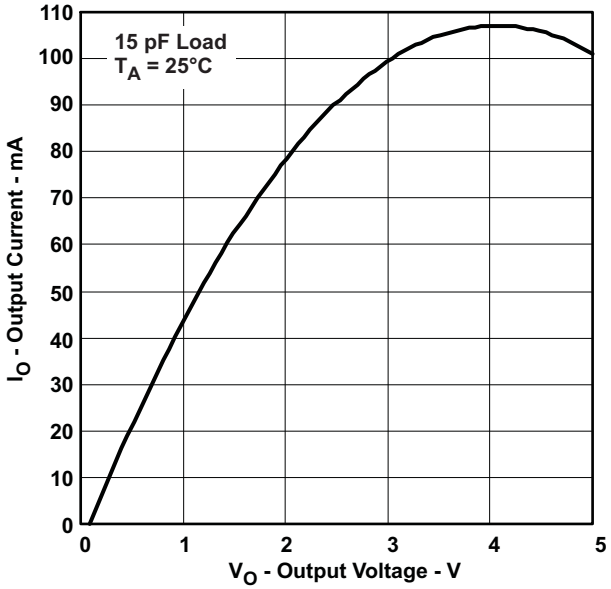
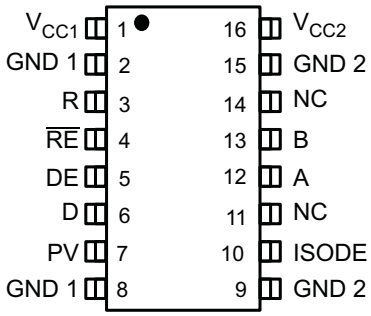


Figure 27.

DEVICE INFORMATION

DW PACKAGE
(TOP VIEW)



PACKAGE PIN FUNCTION DESCRIPTION

NAME	PIN NO.	FUNCTION
Vcc1	1	logic side power supply
GND1	2, 8	logic side ground, internally connected
R	3	receiver output
$\overline{RE}$	4	receiver logic-low enable
DE	5	driver logic-high enable input
D	6	driver input
PV	7	ISO1176 chip enable, logic high applied immediately after power-up for device operation. A logic low 3-states all outputs.
GND2	9, 15	bus side ground, internally connected
ISODE	10	bus-side driver enable output
nc	11, 14	not connected internally, may be left floating
A	12	non-inverting bus output
B	13	inverting bus output
Vcc2	16	bus side power supply

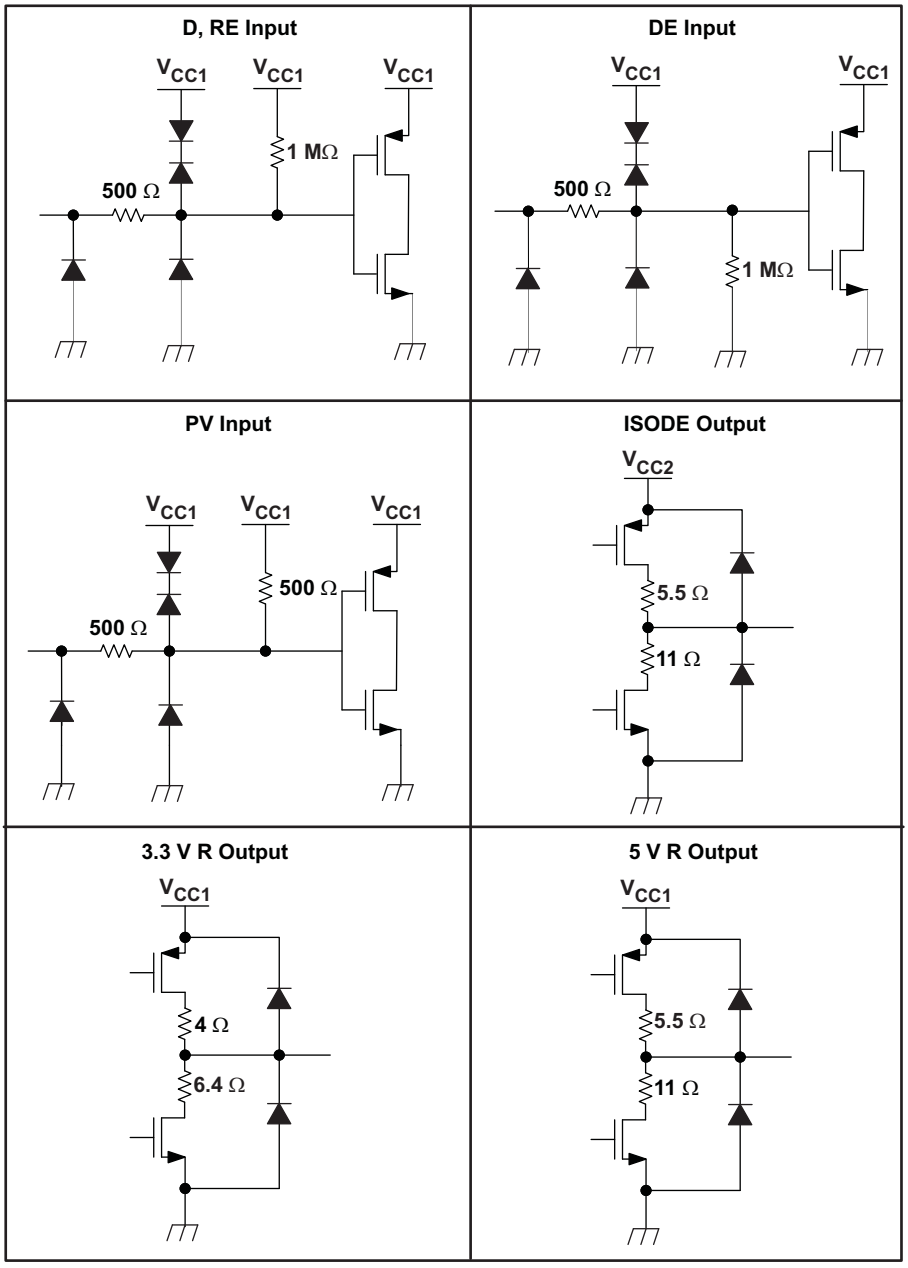
DRIVER FUNCTION TABLE

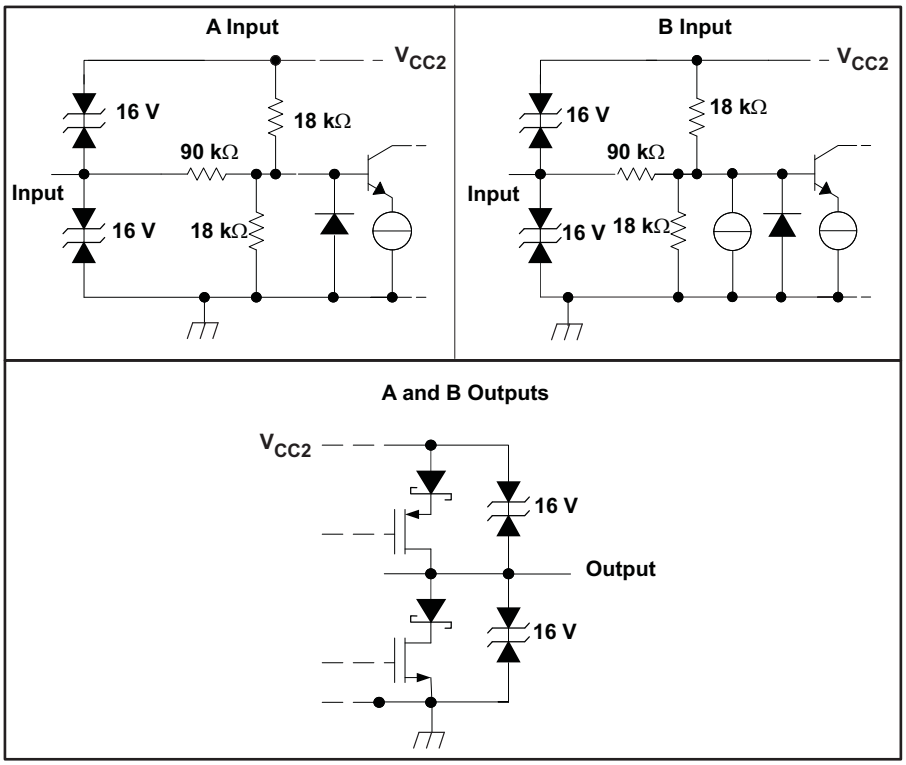
V_{CC1}	V_{CC2}	POWER VALID (PV) (ISO1176)	INPUT (D)	ENABLE INPUT (DE)	ENABLE OUTPUT (ISODE)	OUTPUTS	
						A	B
PU	PU	H or open	H	H	H	H	L
PU	PU	H or open	L	H	H	L	H
PU	PU	H or open	X	L	L	Z	Z
PU	PU	H or open	X	open	L	Z	Z
PU	PU	H or open	open	H	H	H	L
PD	PU	X	X	X	L	Z	Z
PU	PD	X	X	X	L	Z	Z
PD	PD	X	X	X	L	Z	Z
X	X	L	X	X	L	Z	Z
H = high level, L= low level, X = don't care, Z = high impedance (off), ? = indeterminate							

RECEIVER FUNCTION TABLE

V_{CC1}	V_{CC2}	POWER VALID (PV) (ISO1176)	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT)
PU	PU	H or open	$-0.01\ V \le V_{ID}$	L	H
PU	PU	H or open	$-0.2\ V < V_{ID} < -0.01\ V$	L	?
PU	PU	H or open	$V_{ID} \le -0.2\ V$	L	L
PU	PU	H or open	X	H	Z
PU	PU	H or open	X	open	Z
PU	PU	H or open	Open circuit	L	H
PU	PU	H or open	Short Circuit	L	H
PU	PU	H or open	Idle (terminated) bus	L	H
PD	PU	X	X	X	Z
PU	PD	H or open	X	L	H
PD	PD	X	X	X	Z
X	X	L	X	X	Z
H = high level, L= low level, X = don't care, Z = high impedance (off), ? = indeterminate					

EQUIVALENT CIRCUIT SCHEMATICS





IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A Failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			128	mA
T_S	Maximum case temperature	DW-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K thermal resistance(1)		168		°C/W
		High-K board(1)		96.1		
θ_{JB}	Junction-to-board thermal resistance			61		°C/W
θ_{JC}	Junction-to-case thermal resistance			48		°C/W
P_D	Device power dissipation	Vcc1 = Vcc2 = 5.25 V, T_J = 150°C, C_L = 15 pF, Input a 20 MHz 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

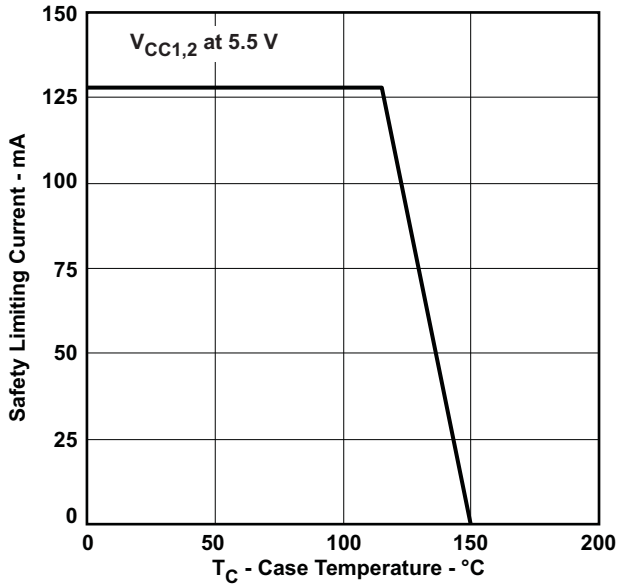


Figure 28. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2

PACKAGE CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	7.7			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File Number: 40014131	File Number: Pending	File Number: E181974

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

IEC 60554-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage < 150 VRMS	I-IV
	Rated mains voltage < 300 VRMS	I-III
	Rated mains voltage < 400 VRMS	I-II

IEC 60747-5-2 INSULATION CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge <5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

APPLICATION INFORMATION

Transient Voltages

Isolating of a circuit insulates it from other circuits and earth, so that noise voltage develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation. The transient ratings of the ISO1176 standard are sufficient for all but the most severe installations. However, some equipment manufacturers use ESD generators to test equipment transient susceptibility. This practice can easily exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but very high-voltage transients.

Figure 29 models the ISO1176 bus IO connected to a noise generator. C_{IN} and R_{IN} is the device, and any other stray or added capacitance or resistance across the A or B pin to GND2. C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of the ISO1176, plus those of any other insulation (transformer, etc.). Stray inductance is assumed to be negligible.

From this model, the voltage at the isolated bus return is

$$V_{GND2} = V_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \quad (1)$$

and will always be less than 16 V from V_N. If the ISO1176 is tested as a stand-alone device,

- R_{IN}= 6 x 10^4 Ω,
- C_{IN}= 16 x 10^{-12} F,
- R_{ISO}= 10^9 Ω and
- C_{ISO}= 10^{-12} F.

Notice from Figure 29 that the resistor ratio determines the voltage ratio at low frequencies, and that the inverse capacitance ratio determines the voltage ration at high frequencies. In the stand-alone case and for low frequencies,

$$\frac{V_{GND2}}{V_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6x10^4} \quad (2)$$

, or essentially all of the noise appears across the barrier.

At very high frequencies,

$$\frac{V_{GND2}}{V_N} = \frac{1/C_{ISO}}{1/C_{ISO} + 1/C_{IN}} = \frac{1}{1 + C_{ISO}/C_{IN}} = \frac{1}{1 + 1/16} = 0.94 \quad (3)$$

, and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of the transient noise appears across the isolation barrier, as it should.

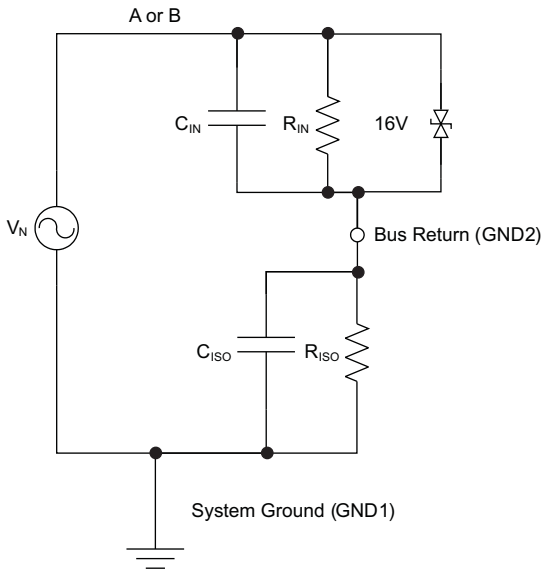


Figure 29. Device Model For Static Discharge Testing

We do not recommend using ESD generators to test equipment transient susceptibility, or considering product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell, and by proper installer training.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ISO1176DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO1176DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

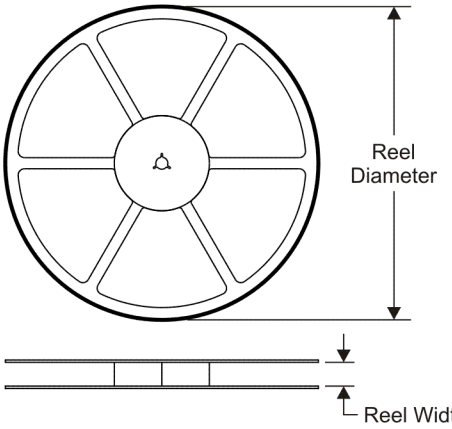
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

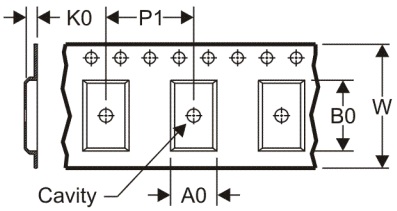
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

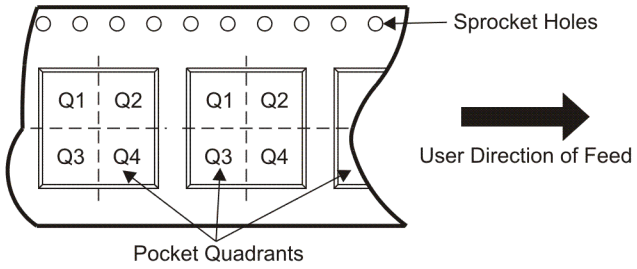


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

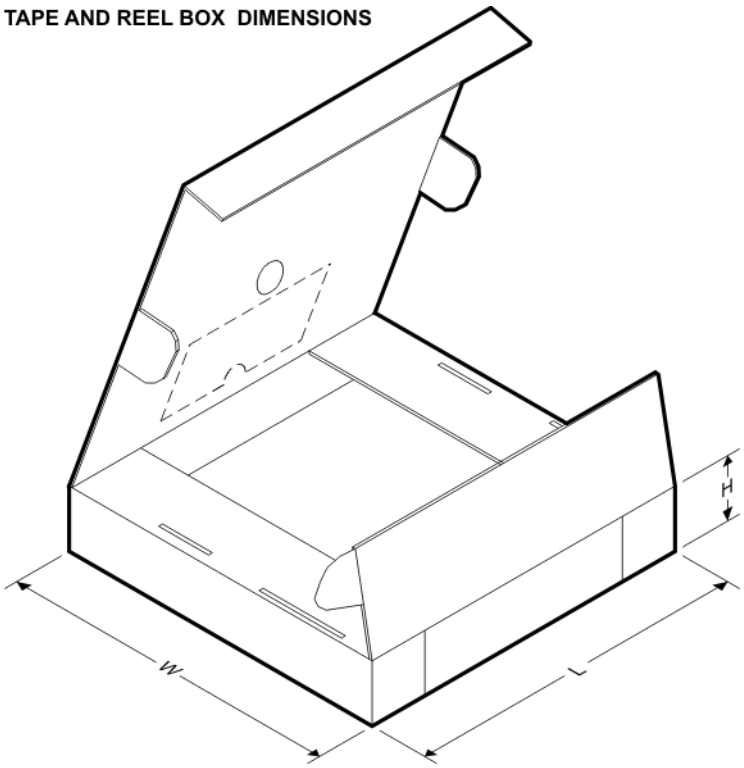
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1176DWR	SOIC	DW	16	2000	330.0	16.4	10.9	10.78	3.0	12.0	16.0	Q1

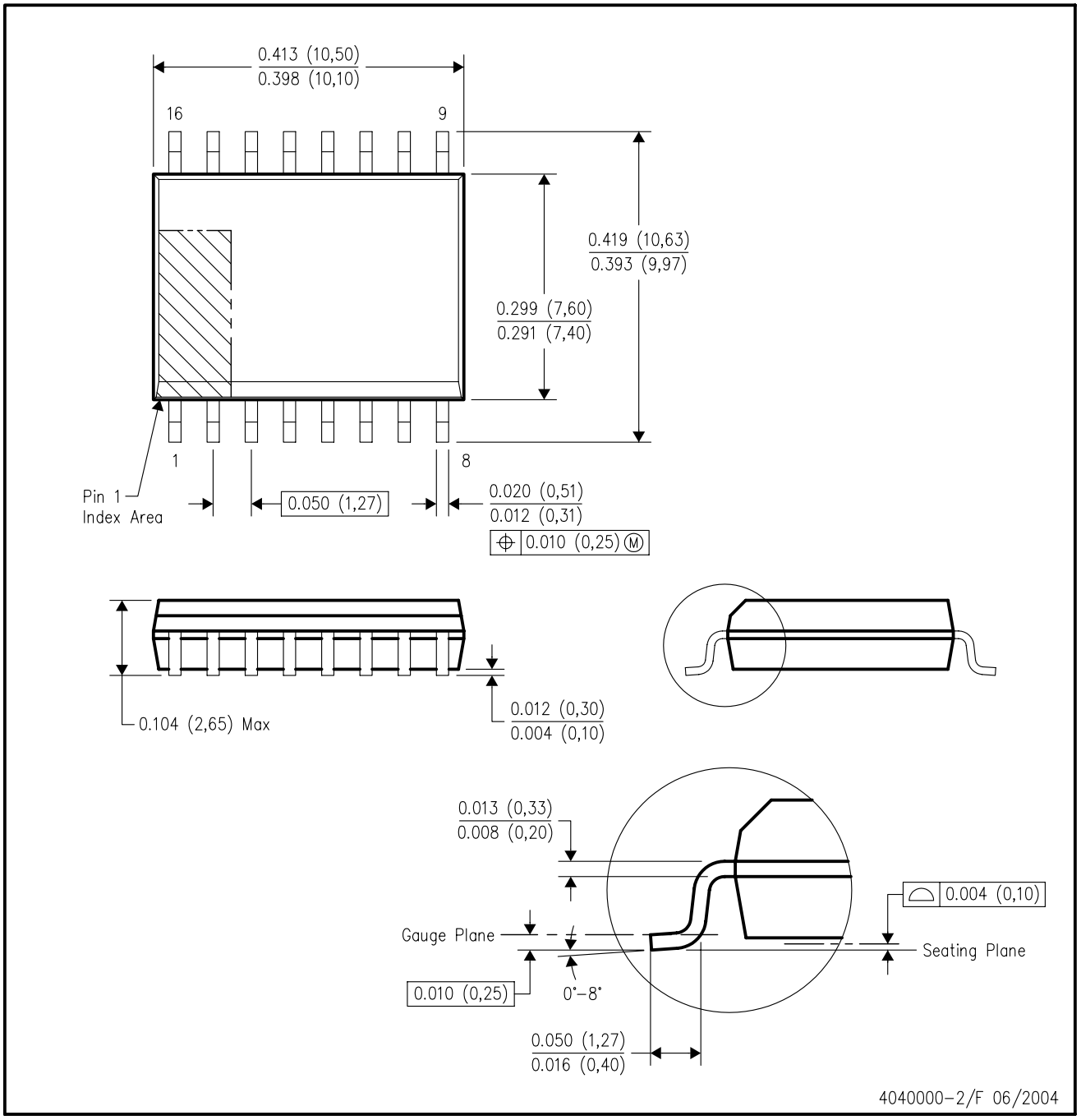
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1176DWR	SOIC	DW	16	2000	358.0	335.0	35.0

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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