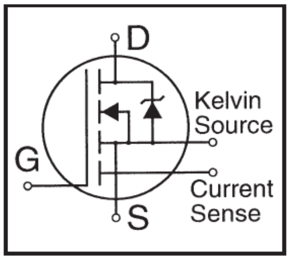
International
IOR Rectifier

PD- 95999B

IRCZ34PbF

HEXFET® Power MOSFET

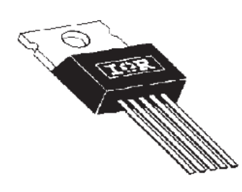
- Dynamic dv/dt Rating
- Current Sense
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



V_{DSS} = 60V

$R_{DS(on)}$ = 0.050Ω

I_D = 30A



TO-220 HexSense

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device, low on-resistance and cost-effectiveness.

The HEXSence device provides an accurate fraction of the drain current through the additional two leads to be used for control or protection of the device. These devices exhibit similar electrical and thermal characteristics as their IRF-series equivalent part numbers. The provision of a kelvin source connection effectively eliminates problems of common source inductance when the HEXSence is used as a fast, high-current switch in non current-sensing applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	30	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	21	
I_{DM}	Pulsed Drain Current ①	120	
P_D @T_C = 25°C	Power Dissipation	88	W
	Linear Derating Factor	0.59	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

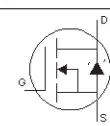
	Parameter	Min.	Max.	Units	
$R_{θJC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{θJA}$	Junction-to-Ambient	—	—	62	

** When mounted on FR-4 board using minimum recommended footprint. For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.065	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	–––	–––	0.050	Ω	V_{GS} = 10V, I_D = 18A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	9.4	–––	–––	S	V_{DS} = 25V, I_D = 18A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25		V_{DS} = 60V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 48V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100		V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
Q_g	Total Gate Charge	–––	–––	46		I_D = 30A
Q_{gs}	Gate-to-Source Charge	–––	–––	11	nC	V_{DS} = 48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	22		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	13	–––		V_{DD} = 30V
t_r	Rise Time	–––	100	–––		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	–––	29	–––		R_G = 12Ω
t_f	Fall Time	–––	52	–––		R_D = 1.0Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6 mm (0.25 in.) from package and center of die contact
L_c	Internal Source Inductance	–––	7.5	–––		
C_{iss}	Input Capacitance	–––	1300	–––		V_{GS} = 0V
C_{oss}	Output Capacitance	–––	640	–––	pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	96	–––		f = 1.0MHz, See Fig. 5
r	Current Sensing Ratio	1340	–––	1480	–––	I_D = 30A, V_{GS} = 10V
C_{oss}	Output Capacitance of Sensing Cells	–––	9.0	–––	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	120		
V_{SD}	Diode Forward Voltage	–––	–––	1.6	V	T_J = 25°C, I_S = 30A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	120	230	ns	T_J = 25°C, I_F = 30A
Q_{rr}	Reverse Recovery Charge	–––	0.70	1.4	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 0.019mH R_G = 25Ω, I_{AS} = 30A. (See Figure 12)

③ $I_{SD} \le$ 30A, di/dt ≤ 200A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

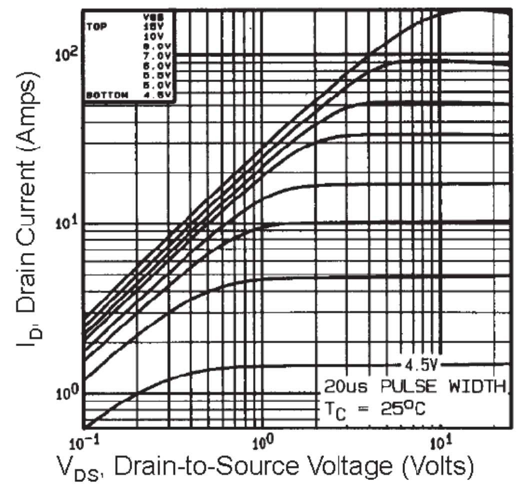


Fig. 1 Typical Output Characteristics, T_C=25°C

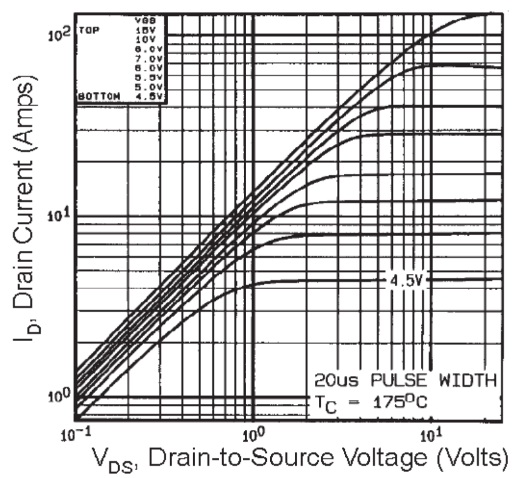


Fig. 2 Typical Output Characteristics, T_C=175°C

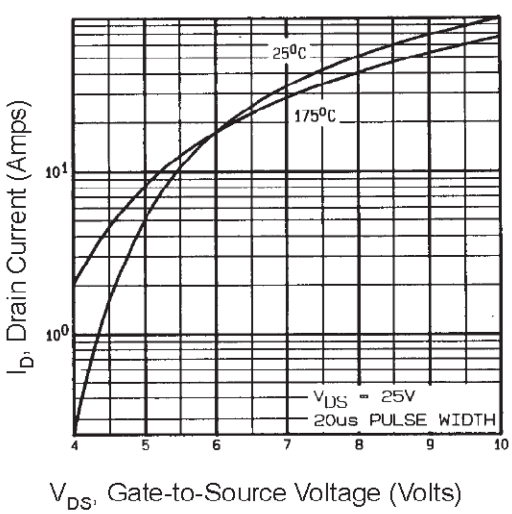


Fig. 3 Typical Transfer Characteristics

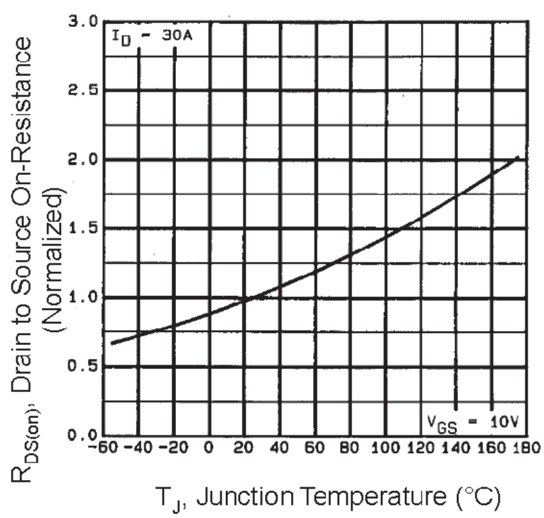


Fig. 4 Normalized On-Resistance vs. Temperature

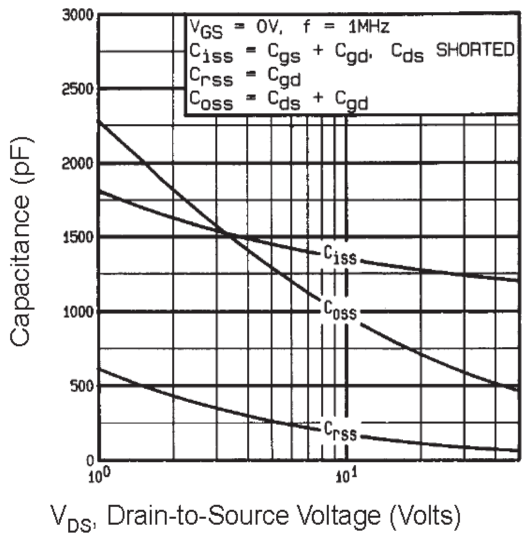


Fig. 5 Typical Capacitance vs. Drain-to-Source Voltage

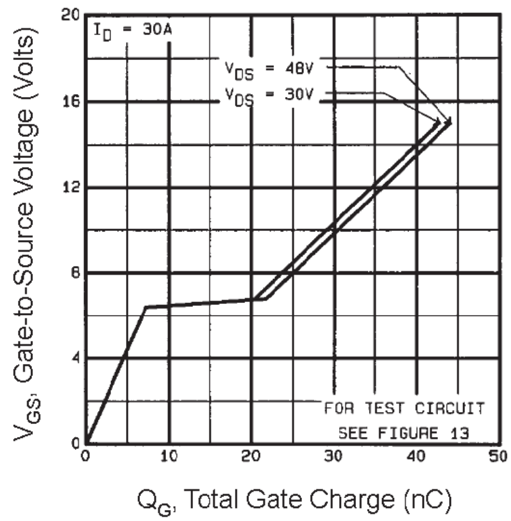


Fig. 6 Typical Gate Charge vs. Gate-to-Source Voltage

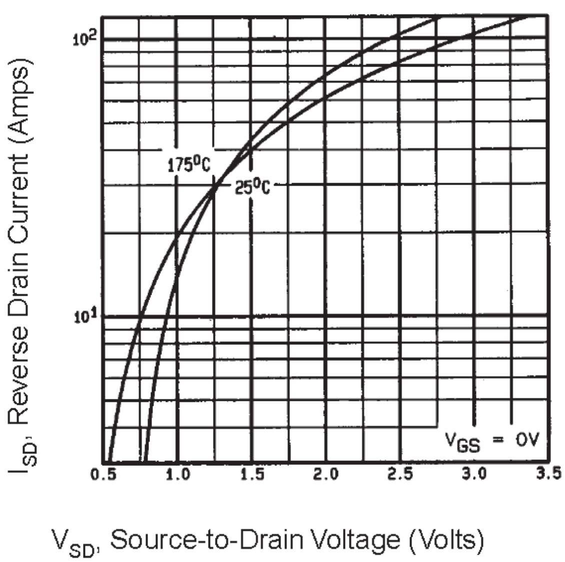


Fig. 7 Typical Source-Drain Diode Forward Voltage

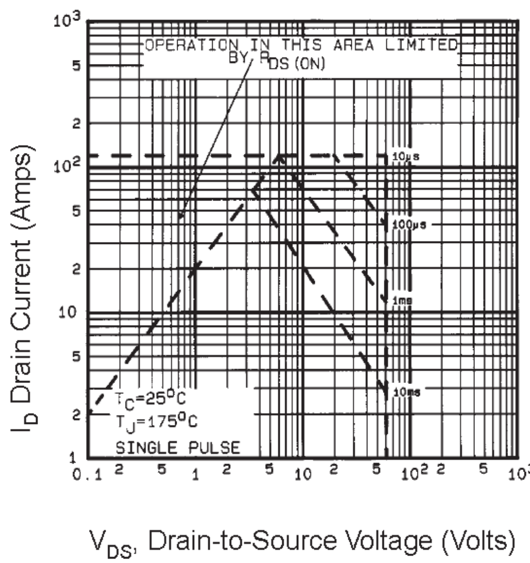


Fig. 8 Maximum Safe Operating Area

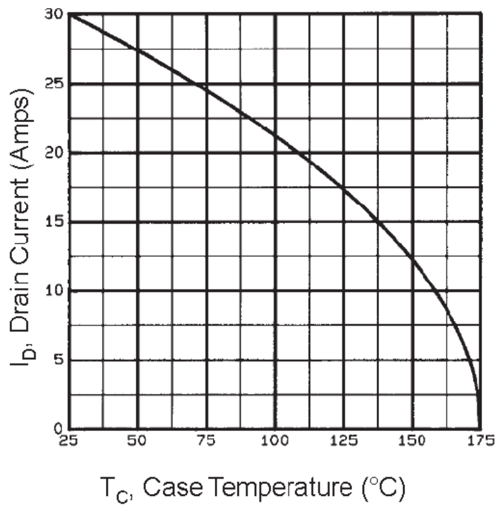


Fig. 9 Maximum Drain Current vs. Case Temperature

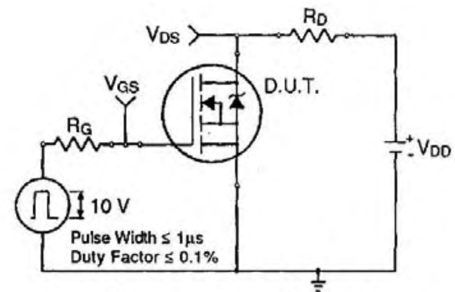


Fig 10a. Switching Time Test Circuit

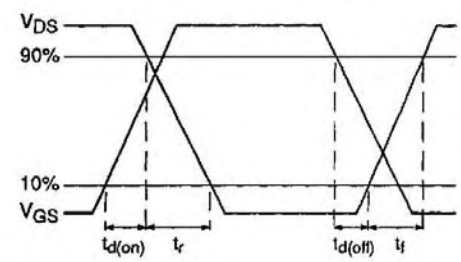


Fig 10b. Switching Time Waveforms

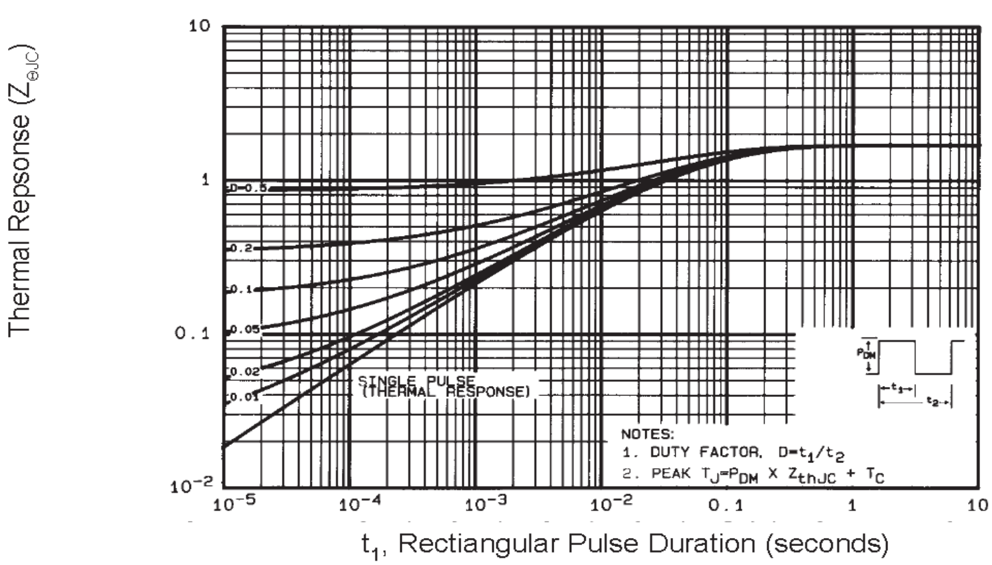


Fig. 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

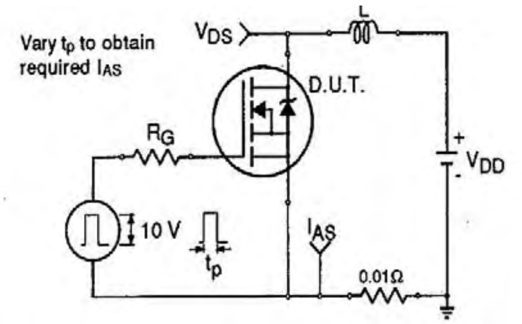


Fig 12a. Unclamped Inductive Test Circuit

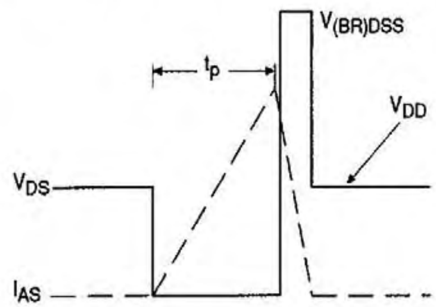


Fig 12b. Unclamped Inductive Waveforms

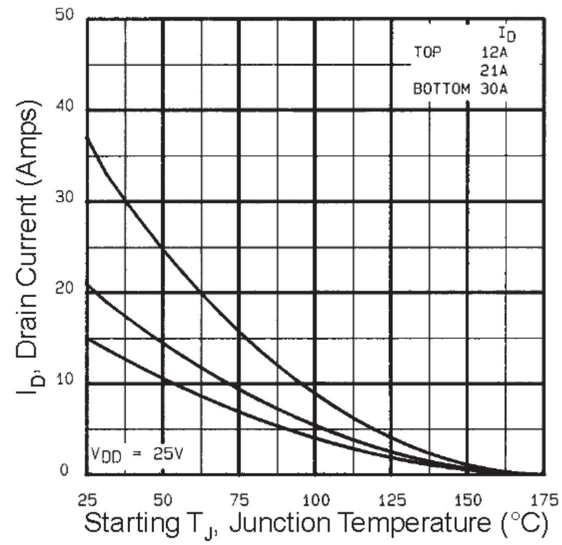


Fig. 12c Maximum Avalanche Energy vs. Drain Current

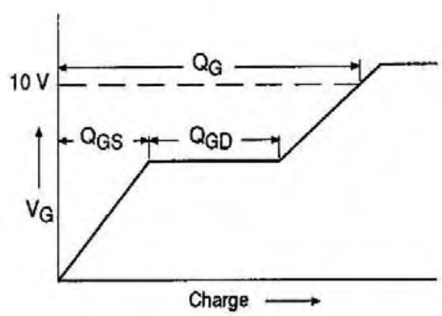


Fig 13a. Basic Gate Charge Waveform

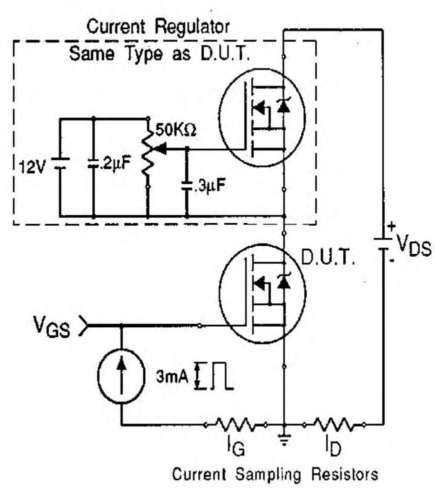


Fig 13b. Gate Charge Test Circuit

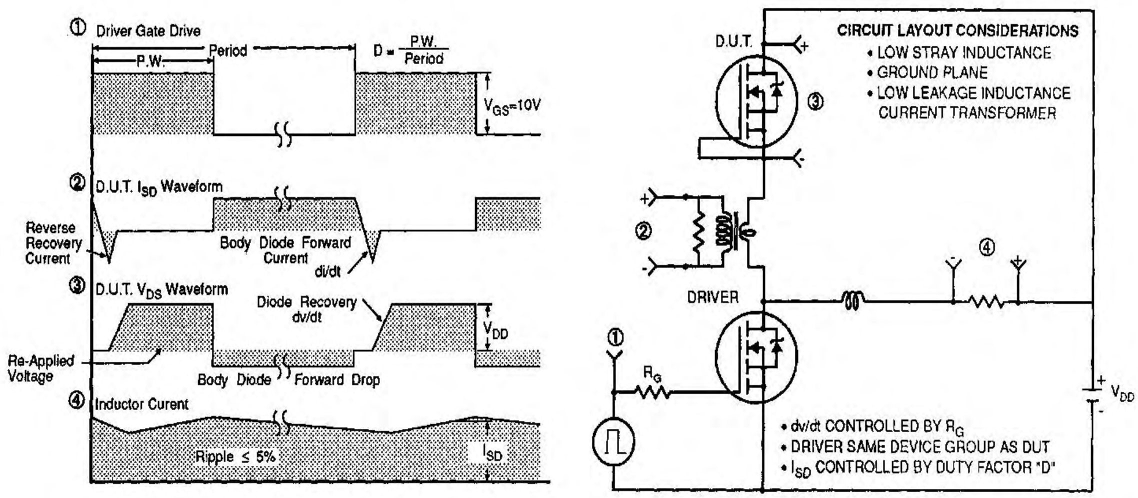


Fig 14. Peak Diode Recovery dv/dt Test Circuit

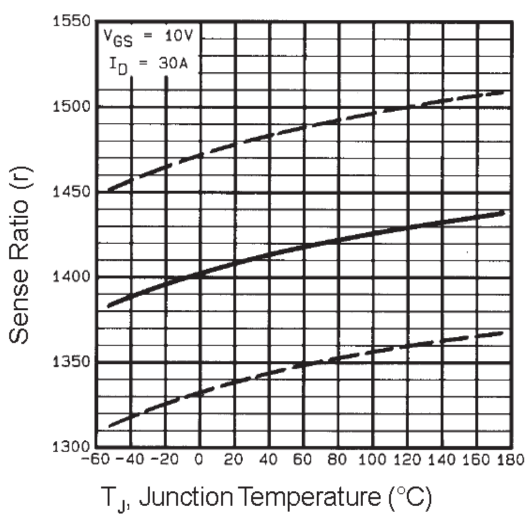


Fig. 15 Typical HEXSense Ratio vs. Junction Temperature

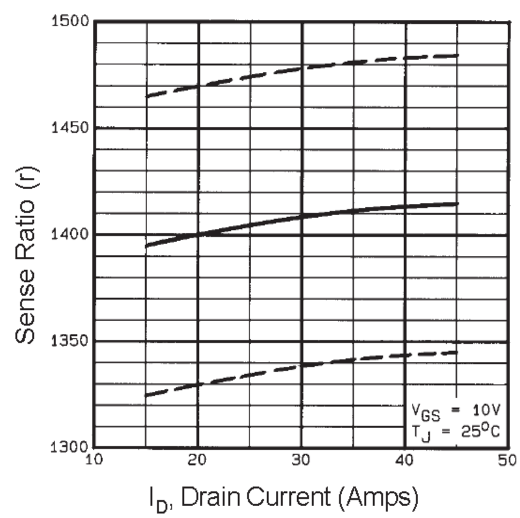


Fig. 16 Typical HEXSense Ratio vs. Drain Current

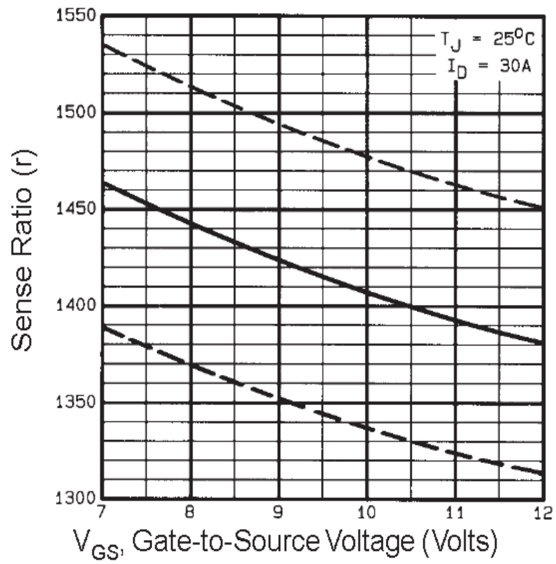


Fig. 17 Typical HEXSense Ratio vs. Gate Voltage

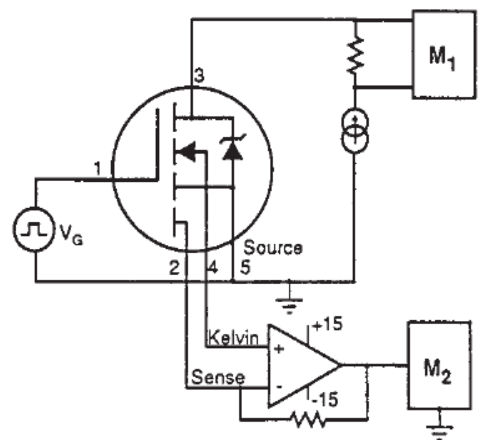


Fig. 18 HEXSense Ratio Test Circuit

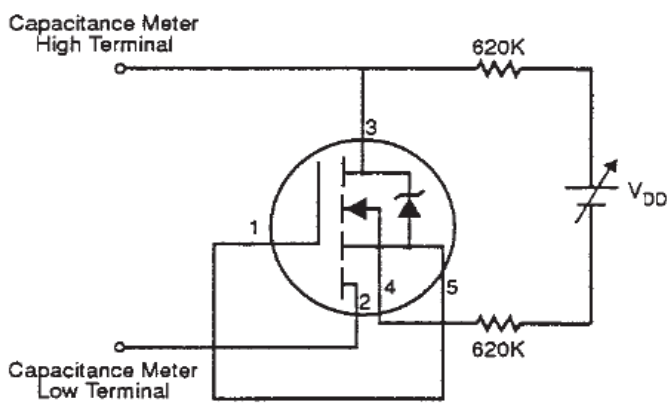
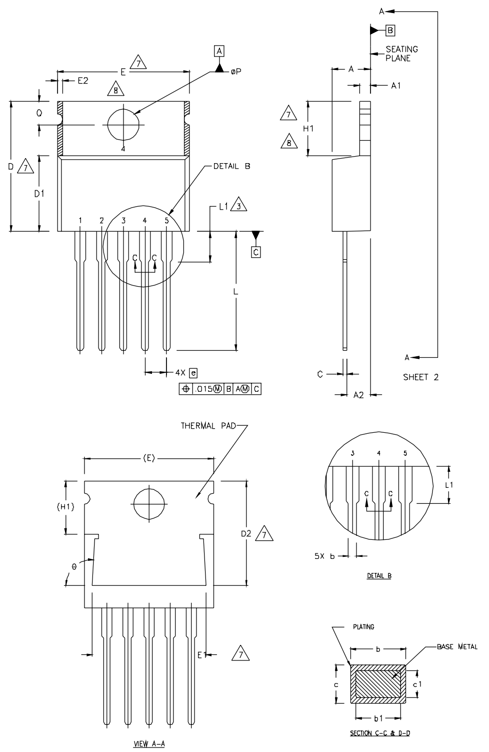


Fig. 19 HEXSense Sensing Cell Output Capacitance Test Circuit

HexsenseTO-220 5L Package Outline

(Dimensions are shown in millimeters (inches)



NOTES:

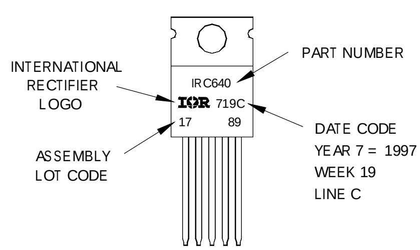
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION : INCHES.
7. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8. DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.64	0.88	.025	.035	
b1	0.64	0.84	.025	.033	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	1.70 BSC		.067 BSC		
H1	5.85	6.55	.230	.270	7,8
L	13.47	14.09	.530	.555	
L1	–	6.35	–	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°–93°		90°–93°		

Hexsense TO-220 5L Part Marking Information

EXAMPLE: THIS IS AN IRC640
WITH ASSEMBLY
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International
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02/05

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