

IRFIB7N50LPbF

SMPS MOSFET
HEXFET® Power MOSFET

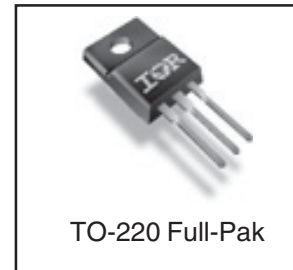
Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications
- Lead-Free

V _{DSS}	R _{DS(on) typ.}	T _{rr typ.}	I _D
500V	320mΩ	85ns	6.8A

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



Absolute Maximum Ratings

Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	6.8
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	4.3
I _{DM}	Pulsed Drain Current ①	27
P _D @ T _C = 25°C	Power Dissipation	46
	Linear Derating Factor	0.37
V _{GS}	Gate-to-Source Voltage	±30
dv/dt	Peak Diode Recovery dv/dt ③	24
T _J	Operating Junction and	-55 to + 150
T _{STG}	Storage Temperature Range	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	6.8	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	27		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 6.8A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	85	130	ns	T _J = 25°C, I _F = 6.8A T _J = 125°C, di/dt = 100A/μs ④
Q _{rr}	Reverse Recovery Charge	—	280	420	nC	T _J = 25°C, I _S = 6.8A, V _{GS} = 0V ④ T _J = 125°C, di/dt = 100A/μs ④
I _{RRM}	Reverse Recovery Current	—	5.9	8.9	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.44	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.32	0.38	Ω	$V_{GS} = 10V, I_D = 4.1A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
R_G	Internal Gate Resistance	—	0.88	—	Ω	$f = 1\text{MHz}, \text{open drain}$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.7	—	—	S	$V_{DS} = 50V, I_D = 4.1A$
Q_g	Total Gate Charge	—	—	92	nC	$I_D = 6.8A$ $V_{DS} = 400V$ $V_{GS} = 10V, \text{See Fig. 7 \& 16}$ ④
Q_{gs}	Gate-to-Source Charge	—	—	24		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	44		
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	$V_{DD} = 250V$ $I_D = 6.8A$ $R_G = 9.0\Omega$ $V_{GS} = 10V, \text{See Fig. 11a \& 11b}$ ④
t_r	Rise Time	—	36	—		
$t_{d(off)}$	Turn-Off Delay Time	—	47	—		
t_f	Fall Time	—	19	—		
C_{iss}	Input Capacitance	—	2220	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}, \text{See Fig. 5}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤
C_{oss}	Output Capacitance	—	230	—		
C_{rss}	Reverse Transfer Capacitance	—	23	—		
C_{oss}	Output Capacitance	—	2780	—		
C_{oss}	Output Capacitance	—	63	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	140	—		
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	100	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	550	mJ
I_{AR}	Avalanche Current ①	—	6.8	A
E_{AR}	Repetitive Avalanche Energy ①	—	4.6	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.69	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient	—	65	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 12).
- ② Starting $T_J = 25^\circ\text{C}$, $L = 24\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 6.8A$, (See Figure 14).
- ③ $I_{SD} \leq 6.8$, $di/dt \leq 650A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $dv/dt = 24V/ns$, $T_J \leq 150^\circ\text{C}$.

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

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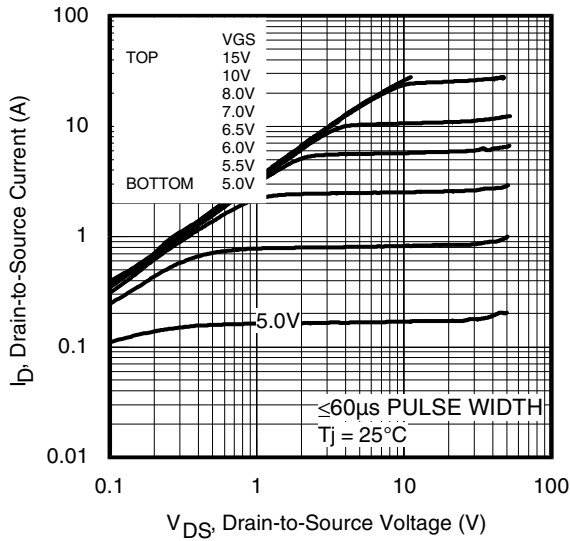


Fig 1. Typical Output Characteristics

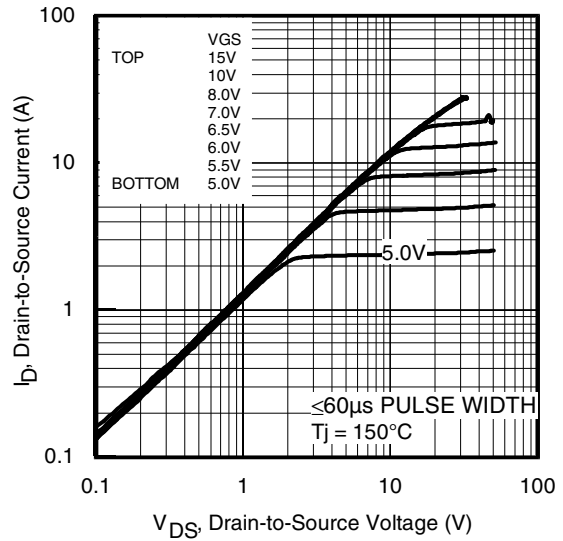


Fig 2. Typical Output Characteristics

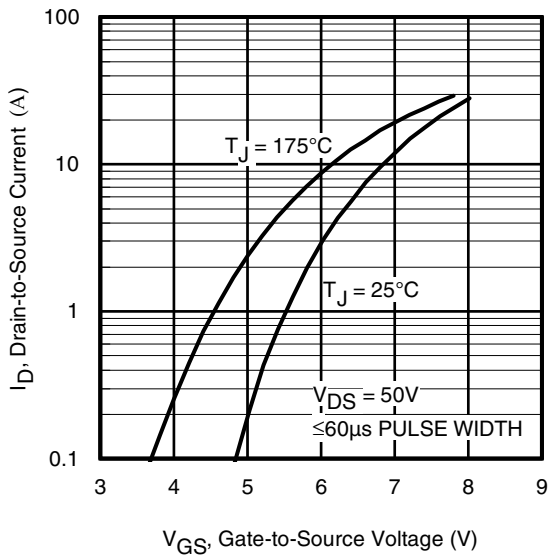


Fig 3. Typical Transfer Characteristics

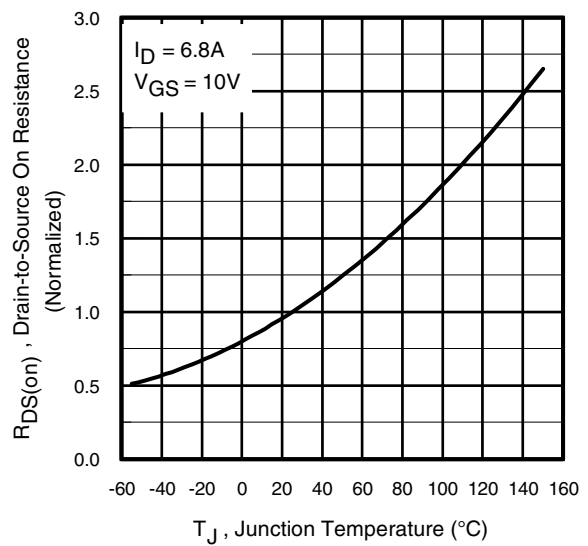


Fig 4. Normalized On-Resistance vs. Temperature

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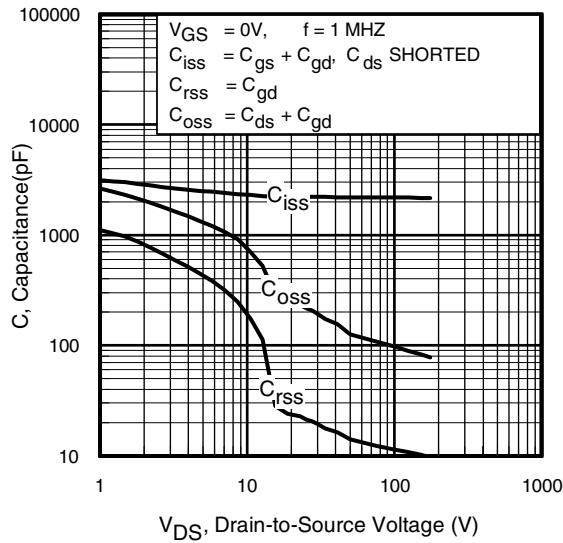


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

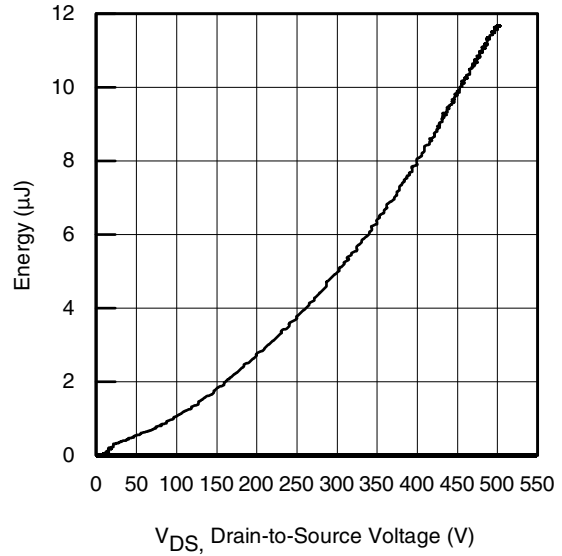


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

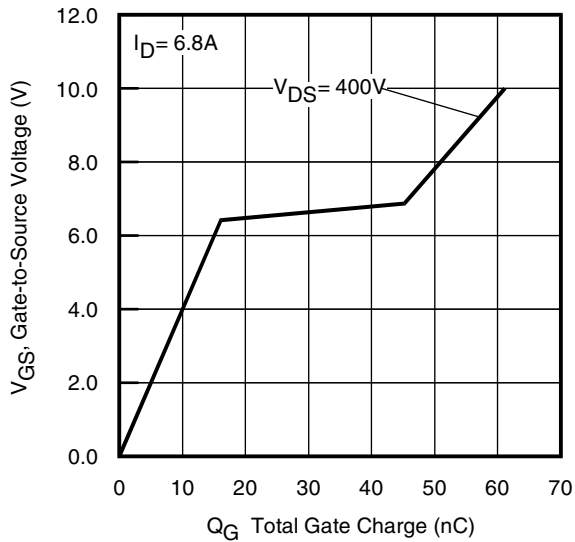


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

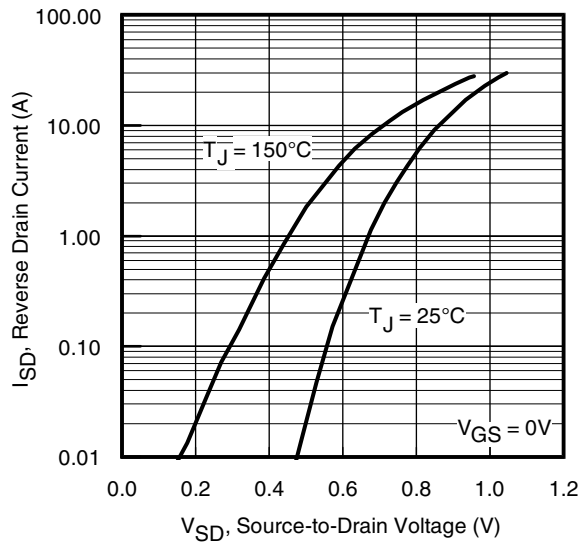


Fig 8. Typical Source-Drain Diode Forward Voltage

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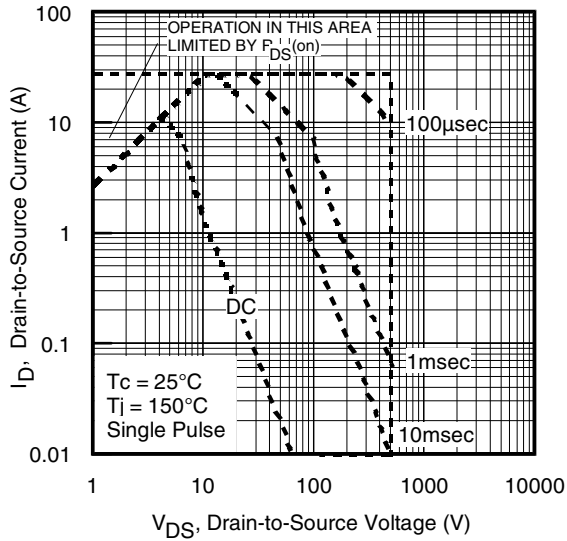


Fig 9. Maximum Safe Operating Area

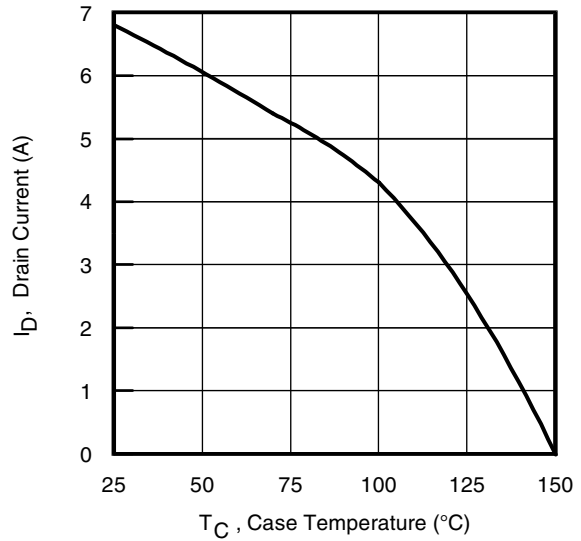


Fig 10. Maximum Drain Current vs. Case Temperature

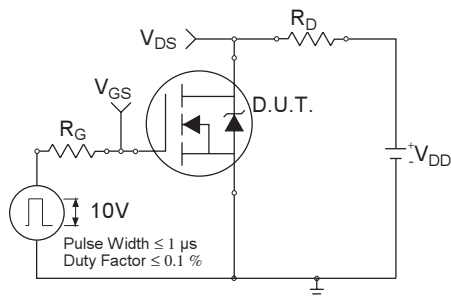


Fig 11a. Switching Time Test Circuit

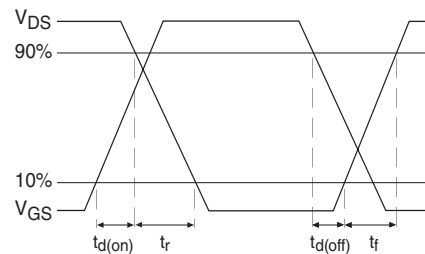


Fig 11b. Switching Time Waveforms

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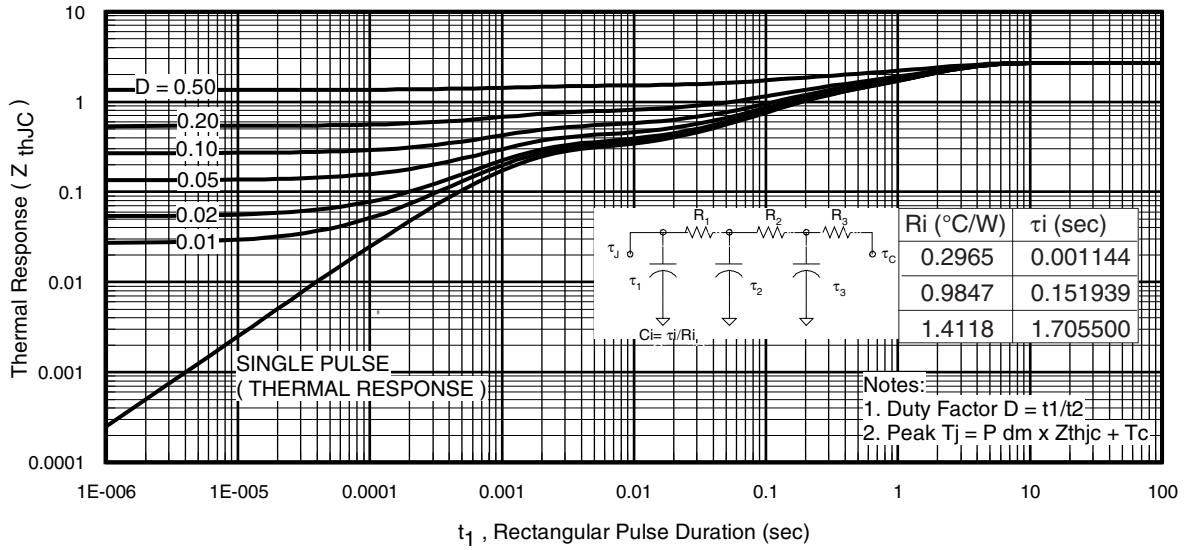


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Case

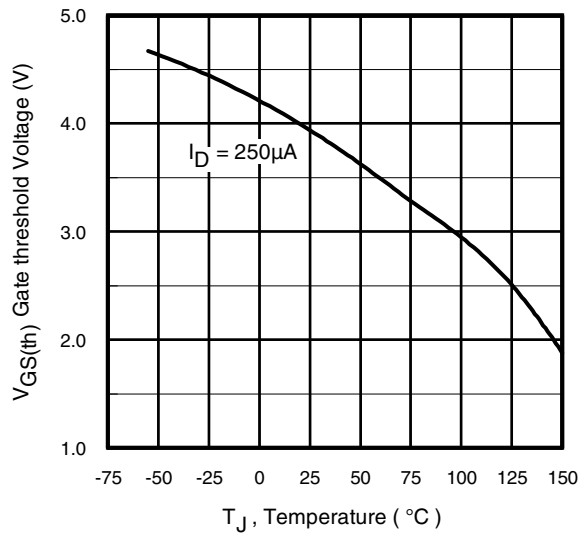


Fig 13. Threshold Voltage vs. Temperature

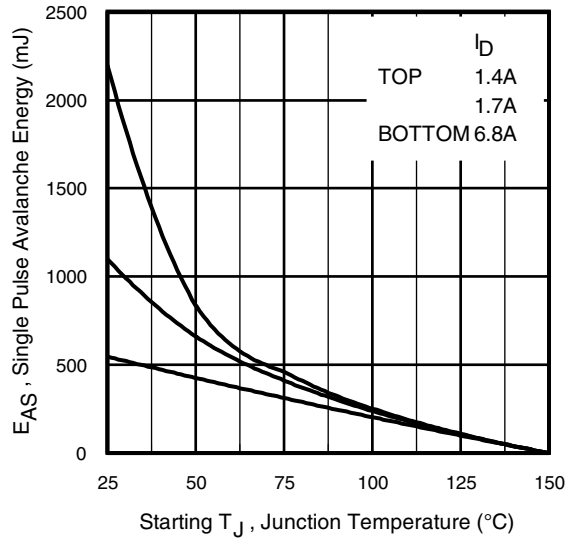


Fig 14. Maximum Avalanche Energy vs. Drain Current

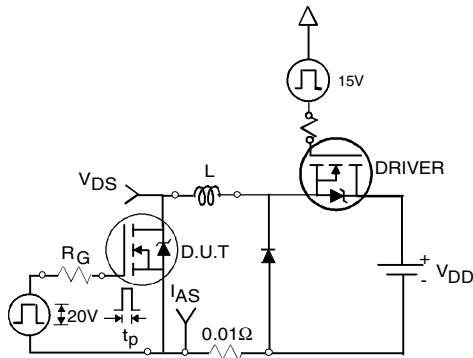


Fig 15a. Unclamped Inductive Test Circuit

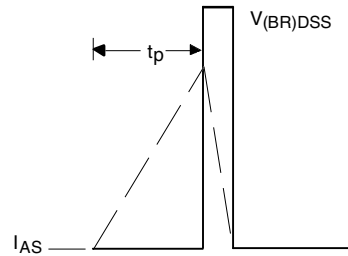


Fig 15b. Unclamped Inductive Waveforms

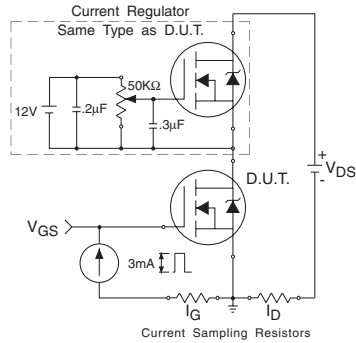


Fig 16a. Gate Charge Test Circuit

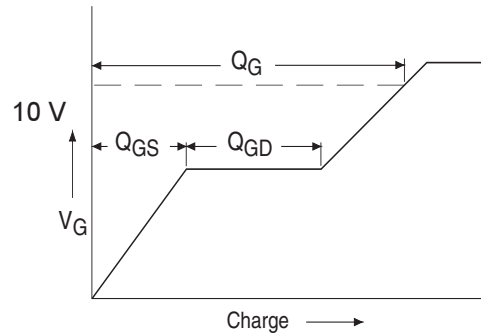
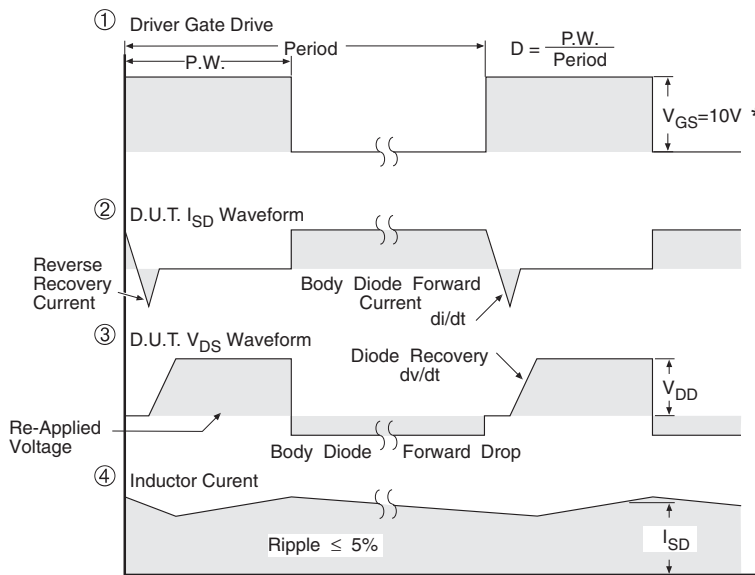
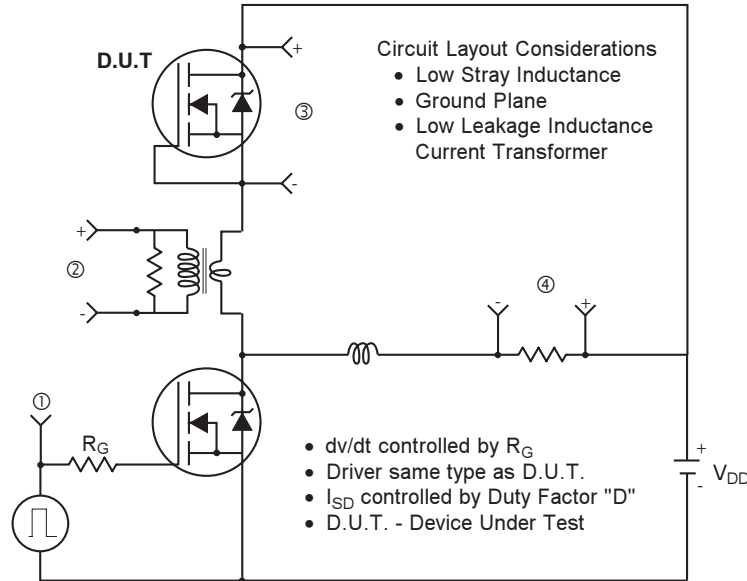


Fig 16b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit

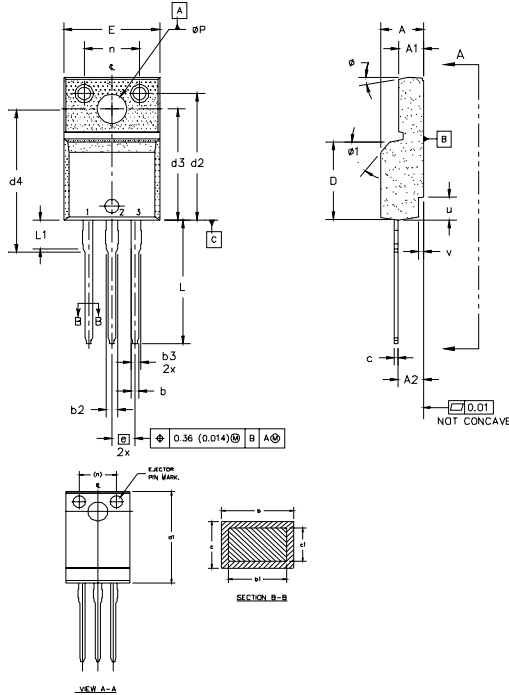


* $V_{GS} = 5V$ for Logic Level Devices

Fig 17. For N-Channel HEXFET® Power MOSFETs

TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



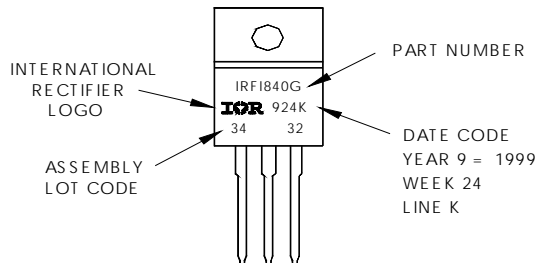
- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
 - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
 - 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	0.180	0.190		
A1	2.57	2.83	0.101	0.114		
A2	2.51	2.85	0.099	0.112		
b	0.622	0.89	0.024	0.035	5	1 - GATE 2 - DRAIN 3 - SOURCE
b1	0.622	0.838	0.024	0.033		
b2	1.229	1.400	0.048	0.055		
b3	1.229	1.400	0.048	0.055		
c	0.440	0.629	0.017	0.025		
c1	0.440	0.584	0.017	0.023	4	IGBTs, CoPACK 1 - GATE 2 - COLLECTOR 3 - EMITTER
D	8.65	9.80	0.341	0.386		
d1	16.80	16.12	0.622	0.635		
d2	13.97	14.22	0.550	0.560		
d3	12.30	12.32	0.484	0.509		
d4	8.64	9.91	0.340	0.390		
E	10.36	10.63	0.408	0.419	4	
e	2.54 BSC		0.100 BSC			
L	13.20	13.73	0.520	0.541	3	
L1	3.10	3.50	0.122	0.138		
n	6.05	6.15	0.238	0.242		
phi P	3.05	3.45	0.120	0.136		
u	2.40	2.50	0.094	0.098	6	
v	0.40	0.50	0.016	0.020		
phi 1	3"	7"	3"	7"		
phi 45	45°		45°			

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
 WITH ASSEMBLY
 LOT CODE 3432
 ASSEMBLED ON WW 24 1999
 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB FullPak package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.



Notice

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