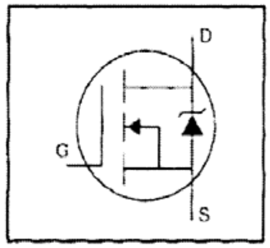
International
IOR Rectifier

IRFP048RPbF

HEXFET® Power MOSFET

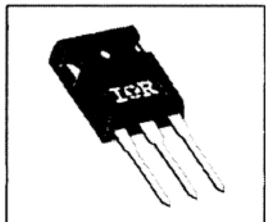
- Dynamic dv/dt Rating
- Isolated Central Mounting Hole
- 175°C Operating Temperature
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



V_{DSS} = 60V

$R_{DS(on)}$ = 0.018Ω

I_D = 70*A



TO-247AC

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial–industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	70*	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	52	
I_{DM}	Pulsed Drain Current ①	290	
P_D @T_C = 25°C	Power Dissipation	190	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	200	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	——	——	0.80	°C/W
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	——	0.24	——	
$R_{θJA}$	Junction-to-Ambient			40	

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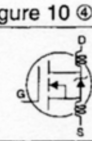
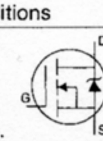
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.060	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.018	Ω	V_{GS}=10V, I_D=44A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, I_D= 250μA
g_{fs}	Forward Transconductance	20	—	—	S	V_{DS}=25V, I_D=44A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=60V, V_{GS}=0V
		—	—	250		V_{DS}=48V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	110	nC	I_D=72A
Q_{gs}	Gate-to-Source Charge	—	—	29		V_{DS}=48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	38		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.1	—	ns	V_{DD}=30V
t_r	Rise Time	—	250	—		I_D=72A
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		R_G=9.1Ω
t_f	Fall Time	—	250	—		R_D=0.34Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	2400	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	1300	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	190	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	70*	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	290		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=73A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	T_J=25°C, I_F=72A
Q_{rr}	Reverse Recovery Charge	—	0.50	0.80	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=25V, starting T_J=25°C, L=43μH R_G=25Ω, I_{AS}=73A (See Figure 12)

③ $I_{SD}\le$72A, di/dt≤200A/μs, $V_{DD}\le V_{(BR)DSS}$, $T_J\le$175°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

* Current limited by the package, (Die Current =73A)

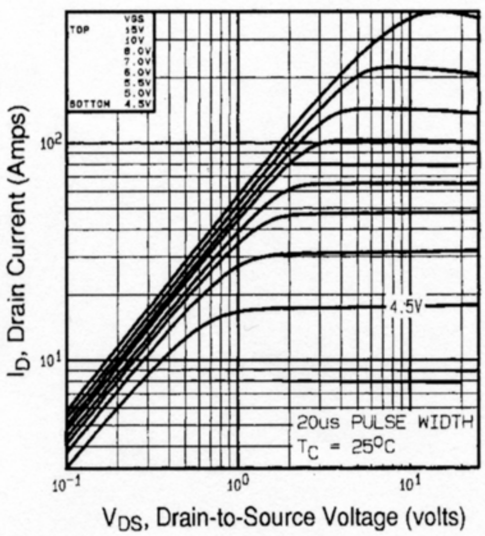


Fig 1. Typical Output Characteristics, T_C=25°C

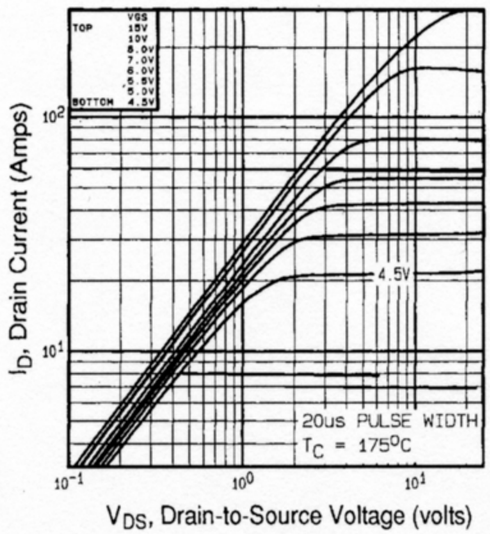


Fig 2. Typical Output Characteristics, T_C=175°C

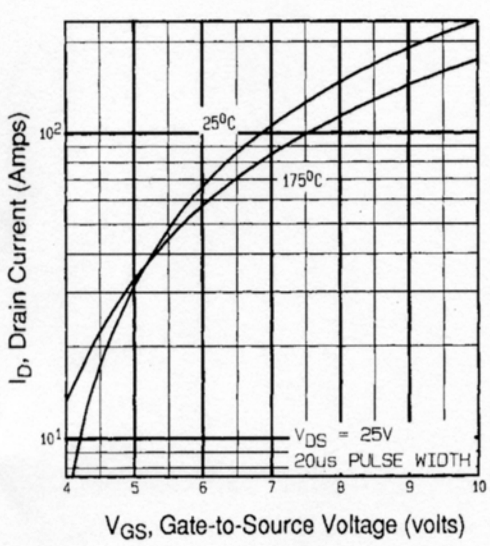


Fig 3. Typical Transfer Characteristics

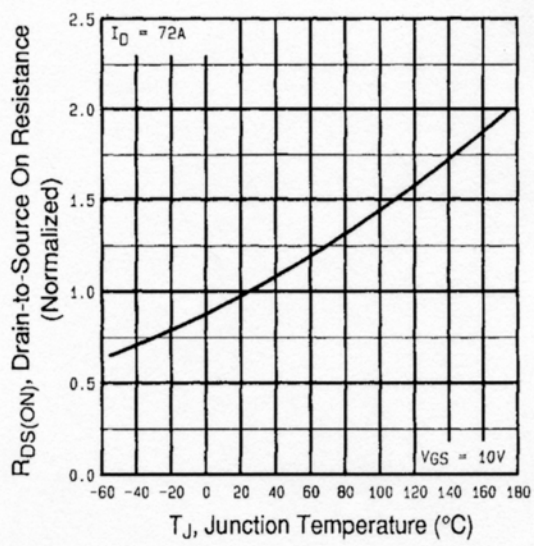


Fig 4. Normalized On-Resistance Vs. Temperature

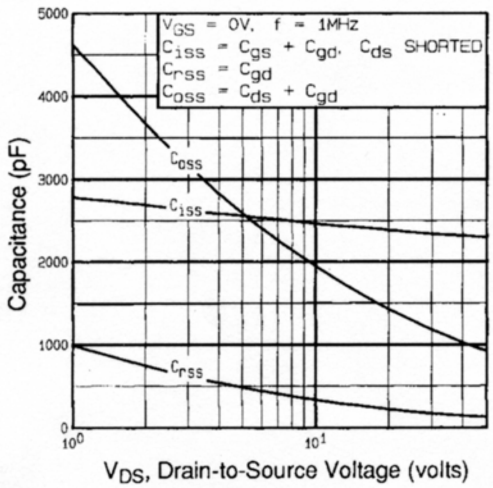


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

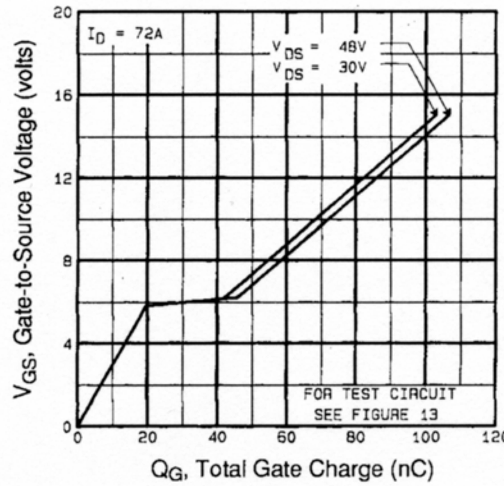


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

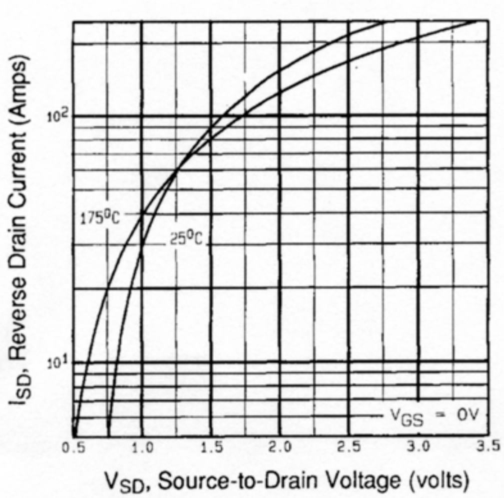


Fig 7. Typical Source-Drain Diode Forward Voltage

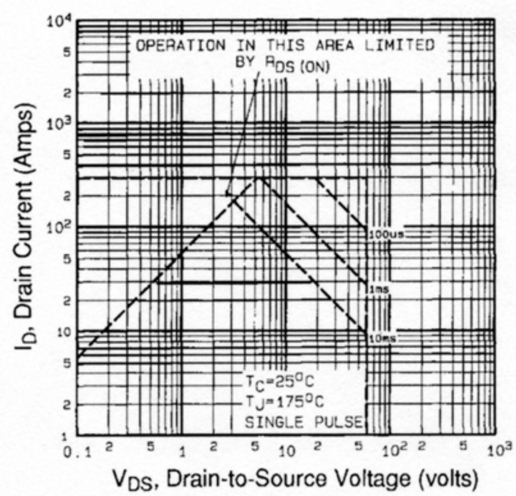


Fig 8. Maximum Safe Operating Area

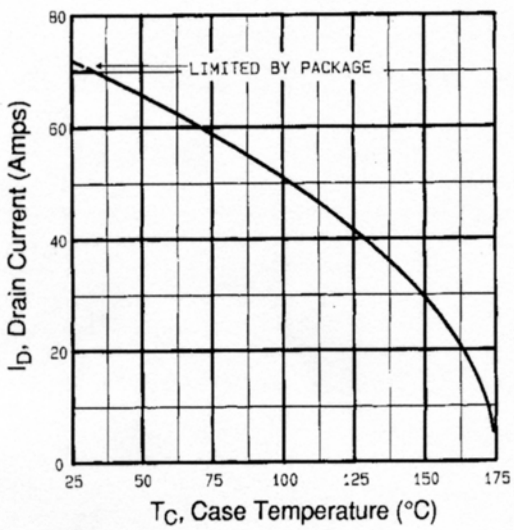


Fig 9. Maximum Drain Current Vs. Case Temperature

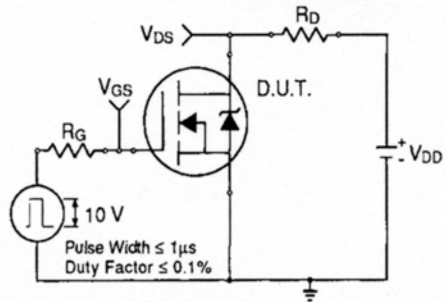


Fig 10a. Switching Time Test Circuit

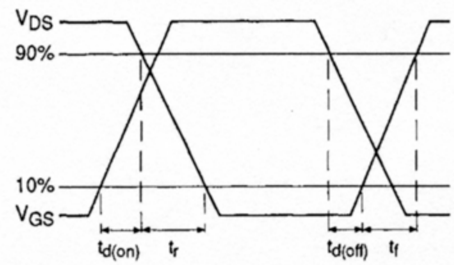


Fig 10b. Switching Time Waveforms

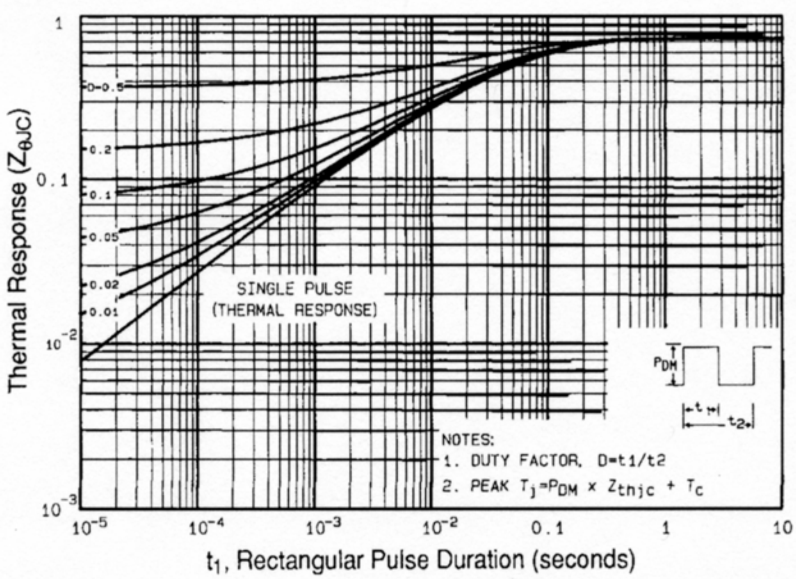


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

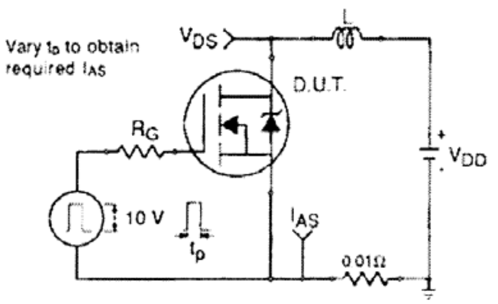


Fig 12a. Unclamped Inductive Test Circuit

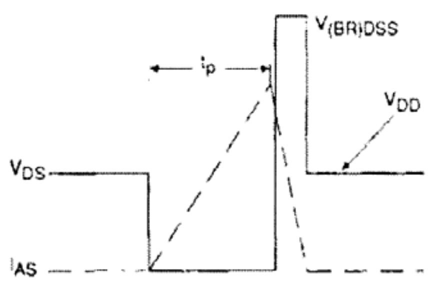


Fig 12b. Unclamped Inductive Waveforms

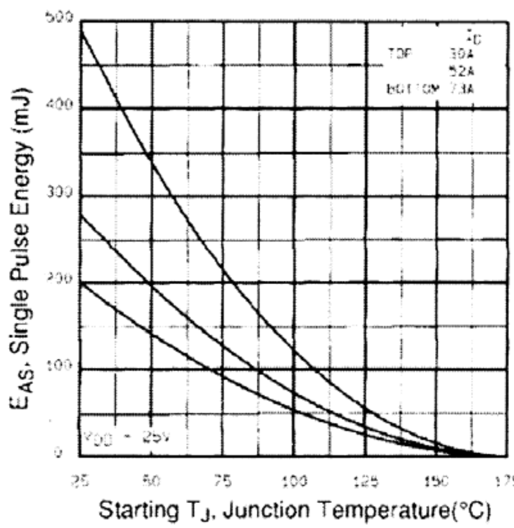


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

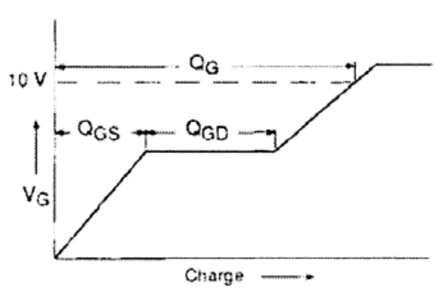


Fig 13a. Basic Gate Charge Waveform

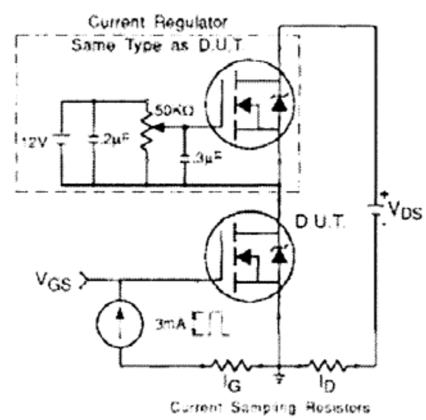
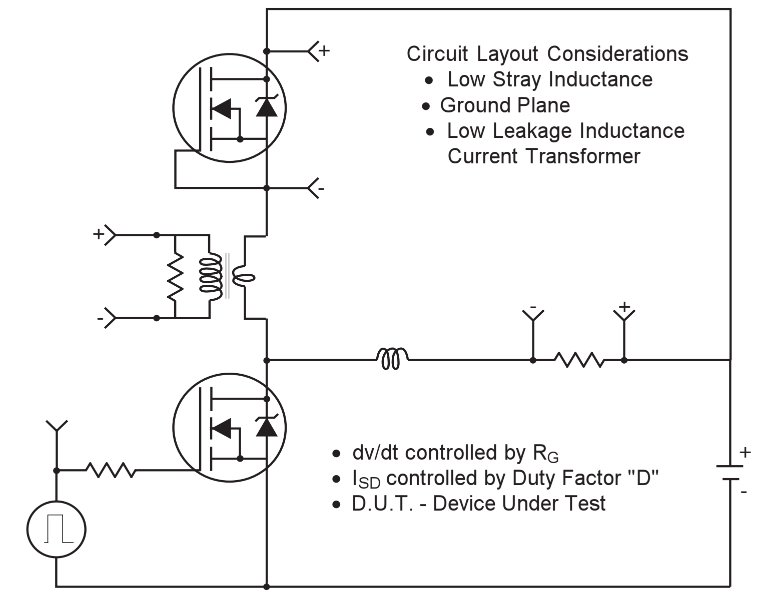
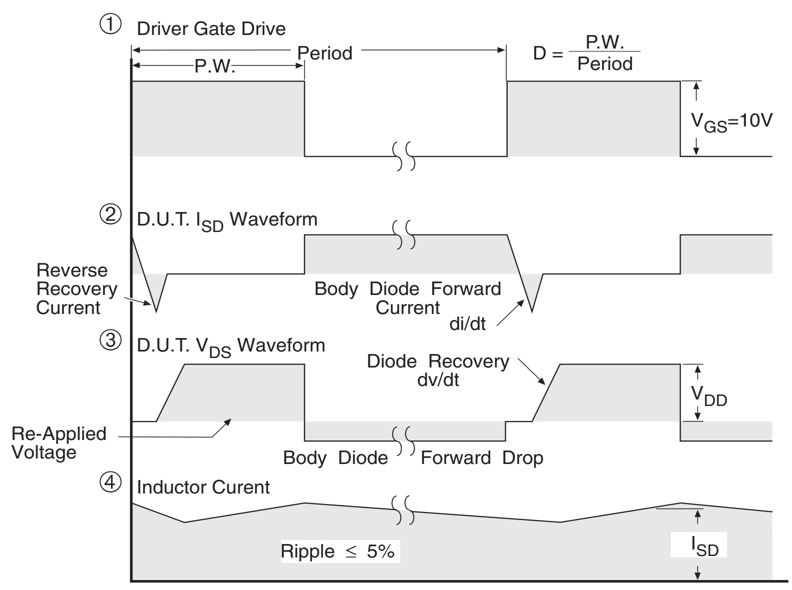


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements

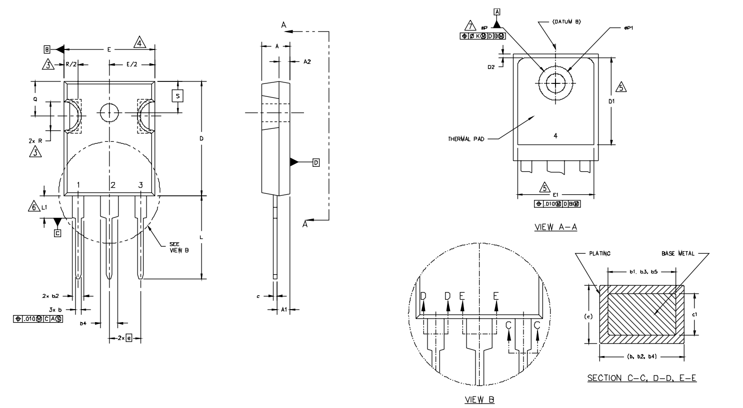


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-Channel HEXFETS

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. (△) CONTOUR OF SLOT OPTIONAL.
4. (△) DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. (△) THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENISONS D1 & E1.
6. (△) LEAD FINISH UNCONTROLLED IN L1.
7. (△) øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91].
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.015	.030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.030	0.51	0.76	
E	.602	.625	15.29	15.87	4
E1	.540	–	15.72	–	
e	.215 BSC		5.46 BSC		
Øk	.010		2.54		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
N	3		7.62 BSC		
øP	.140	.144	3.56	3.66	
øP1	–	.275	–	6.98	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3 – SOURCE
4.– DRAIN

IGBTs, CoPACK

1 – GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

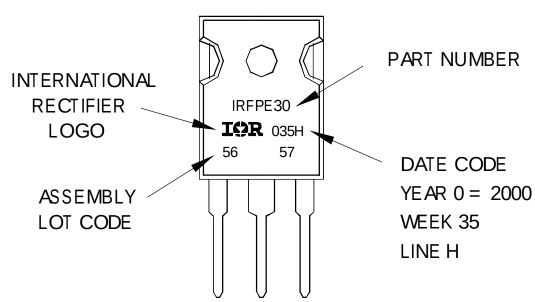
DIODES

1.– ANODE/OPEN
2 – CATHODE
3.– ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International
IOR Rectifier

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07/04

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