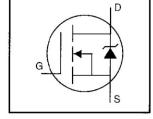
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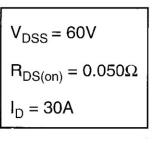
## International **IGR** Rectifier

## IRFZ34PbF

### HEXFET<sup>®</sup> Power MOSFET

- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free

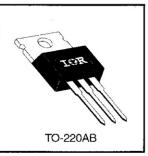




#### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



#### Absolute Maximum Ratings

	Parameter	Max.	Units		
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, V <sub>GS</sub> @ 10 V	30			
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, VGS @ 10 V	21	A		
IDM	Pulsed Drain Current ①	120			
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	88	W		
662669 6646 60	Linear Derating Factor	0.59	W/°C		
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V		
EAS	Single Pulse Avalanche Energy 2	200	mJ		
dv/dt	Peak Diode Recovery dv/dt 3	4.5	V/ns		
TJ Tstg	Operating Junction and Storage Temperature Range	-55 to +175	°C		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)			
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)			

#### **Thermal Resistance**

	Parameter	Min.	Тур.	Max.	Units
Rejc	Junction-to-Case	—	—	1.7	
Recs	Case-to-Sink, Flat, Greased Surface	_	0.50	_	°C/W
Reja	Junction-to-Ambient	—		62	

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### International **TGR** Rectifier

					-		
	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
V(BR)DSS	Drain-to-Source Breakdown Voltage	60	_		V	$V_{GS}=0V, I_{D}=250\mu A$	
ΔV(BR)DSS/ΔTJ	Breakdown Voltage Temp. Coefficient		0.065	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA	
RDS(on)	Static Drain-to-Source On-Resistance	_		0.050	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =18A ④	
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0		4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250µA	
g <sub>fs</sub>	Forward Transconductance	9.3	-	_	S	V <sub>DS</sub> =25V, I <sub>D</sub> =18A ④	
	Durin to Original Landance Original		-	25	μA	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	
DSS	Drain-to-Source Leakage Current		-	250	μА	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	
. <u></u>	Gate-to-Source Forward Leakage	-	-	100	nA	V <sub>GS</sub> =20V	
GSS	Gate-to-Source Reverse Leakage		-	-100		V <sub>GS</sub> =-20V	
Qg	Total Gate Charge	_	-	46		ID=30A	
Q <sub>gs</sub>	Gate-to-Source Charge	-		11	nC	V <sub>DS</sub> =48V	
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	_	-	22		V <sub>GS</sub> =10V See Fig. 6 and 13 @	
t <sub>d(on)</sub>	Turn-On Delay Time		13	—		V <sub>DD</sub> =30V	
tr	Rise Time	-	100	—	ns	ID=30A	
td(off)	Turn-Off Delay Time		29	—	115	$R_G=12\Omega$	
tr	Fall Time	-	52	—		R <sub>D</sub> =1.0Ω See Figure 10 ④	
Lo	Internal Drain Inductance	_	4.5	_	nH	Between lead, 6 mm (0.25in.)	
Ls	Internal Source Inductance		7.5	—		from package and center of die contact	
Ciss	Input Capacitance	—	1200	_		V <sub>GS</sub> =0V	
Coss	Output Capacitance		600	_	pF	V <sub>DS</sub> =25V	
Crss	Reverse Transfer Capacitance	-	100			f=1.0MHz See Figure 5	

#### Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

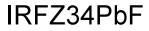
#### **Source-Drain Ratings and Characteristics**

	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current (Body Diode)	-	_	30		MOSFET symbol showing the
ISM	Pulsed Source Current (Body Diode) ①	-	_	120	A	integral reverse p-n junction diode.
VSD	Diode Forward Voltage	-		1.6	V	T_=25°C, Is=30A, VGS=0V @
trr	Reverse Recovery Time	_	120	230	ns	T_=25°C, I <sub>F</sub> =30A
Qrr	Reverse Recovery Charge	-	0.70	1.4	μC	di/dt=100A/µs ④
ton	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by LS+LD)				

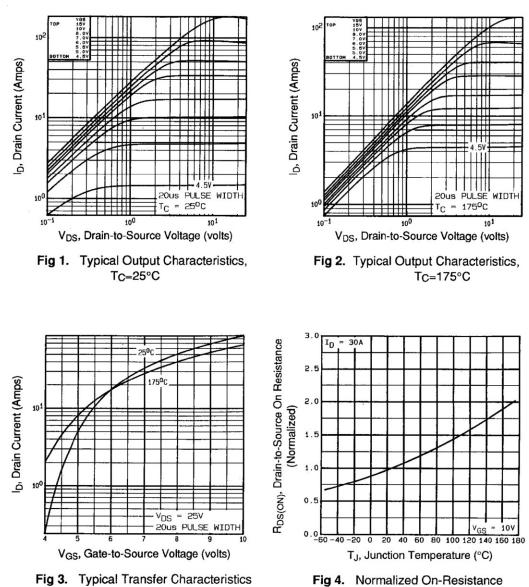
#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ③ I<sub>SD</sub>≤30A, di/dt≤200A/ $\mu$ s, V<sub>DD</sub>≤V(BR)DSS, T<sub>J</sub>≤175°C
- ② V<sub>DD</sub>=25V, starting T<sub>J</sub>=25°C, L=259μH R<sub>G</sub>=25Ω, I<sub>AS</sub>=30A (See Figure 12)
- ④ Pulse width  $\leq$  300 µs; duty cycle  $\leq$ 2%.

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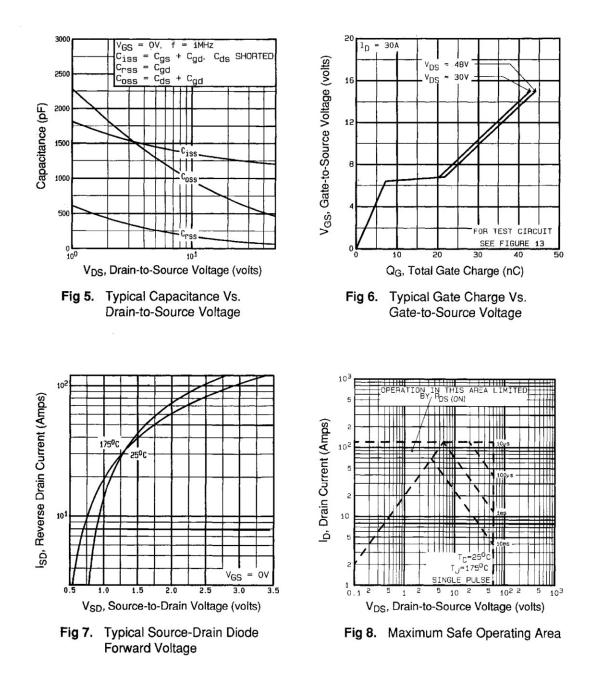
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Vs. Temperature

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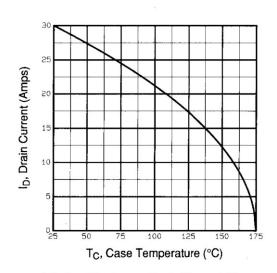
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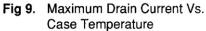


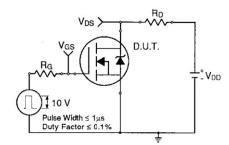
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# International









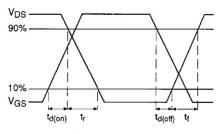


Fig 10b. Switching Time Waveforms

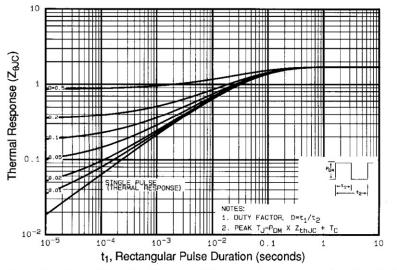


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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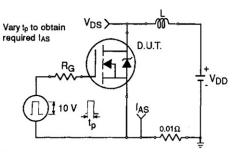


Fig 12a. Unclamped Inductive Test Circuit

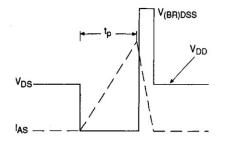


Fig 12b. Unclamped Inductive Waveforms

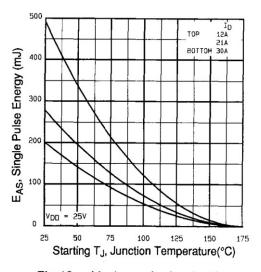


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

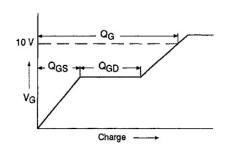


Fig 13a. Basic Gate Charge Waveform

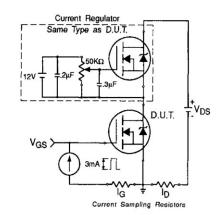


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505 Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix E: Optional Leadforms- See page 1525

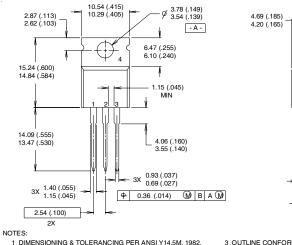


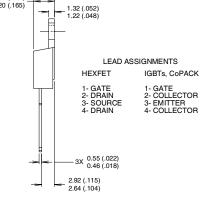
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### **TO-220AB** Package Outline

Dimensions are shown in millimeters (inches)



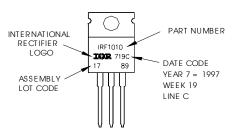


1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982. 2 CONTROLLING DIMENSION : INCH 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB. 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

- B -

### TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010 LOT CODE 1789 ASSEMBLED ON WW 19, 1997 IN THE ASSEMBLY LINE "C" Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

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