N-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
150	0.018 at V_{GS} = 10 V	90[d]	64

FEATURES

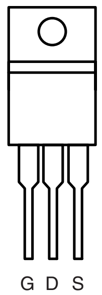
- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- 100 % R_g and UIS Tested

RoHS
COMPLIANT

APPLICATIONS

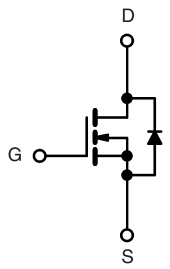
- Primary Side Switch
- Industrial

TO-220AB



Top View

Ordering Information: SUP90N15-18P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	90[d]	A
	T_C = 70 °C		75	
Pulsed Drain Current		I_{DM}	180	
Avalanche Current		I_{AS}	50	
Single Avalanche Energy[a]	L = 0.1 mH	E_{AS}	125	mJ
Maximum Power Dissipation[a]	T_C = 25 °C	P_D	375[b]	W
	T_A = 25 °C[c]		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount)[c]	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.4	

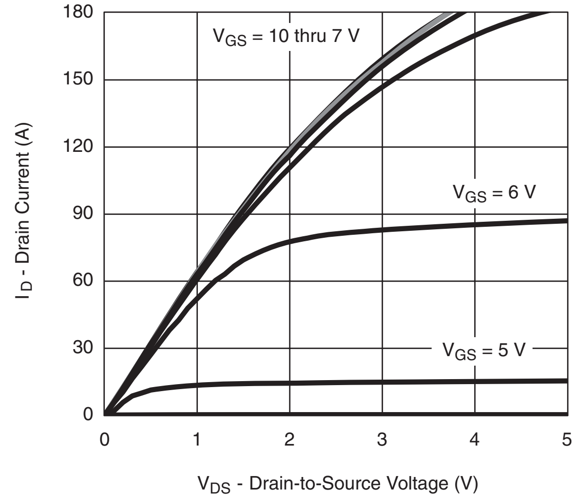
Notes:
a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When Mounted on 1" square PCB (FR-4 material).
d. Package limited.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

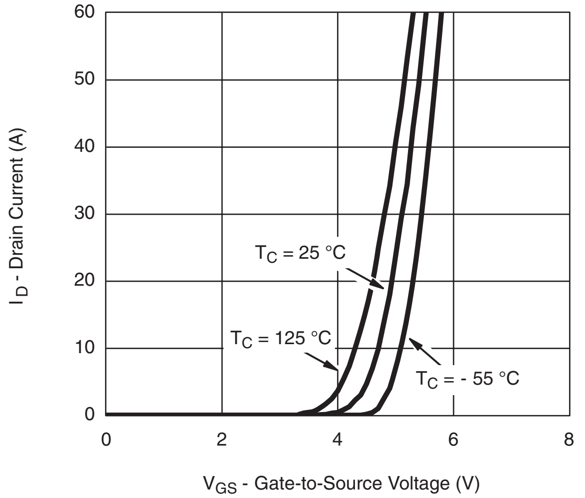
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{DS} = 0 V, I_D = 250 µA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 150 V, V_{GS} = 0 V			1	µA
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 150 °C			250	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 10 V, V_{GS} = 10 V	120			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0145	0.018	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 °C		0.029	0.036	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		55		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 75 V, f = 1 MHz		4180		pF
Output Capacitance	C_{oss}			235		
Reverse Transfer Capacitance	C_{rss}			83		
Total Gate Charge[c]	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_D = 85 A		64	100	nC
Gate-Source Charge[c]	Q_{gs}			23		
Gate-Drain Charge[c]	Q_{gd}			16		
Gate Resistance	R_g	f = 1 MHz		2.1	4.2	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 75 V, R_L = 0.88 Ω $I_D \cong$ 85 A, V_{GEN} = 10 V, R_g = 1 Ω		15	25	ns
Rise Time[c]	t_r			10	15	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	40	
Fall Time[c]	t_f			8	15	
Source-Drain Diode Ratings and Characteristics T_C = 25 °C[b]						
Continuous Current	I_S				90	A
Pulsed Current	I_{SM}				180	
Forward Voltage[a]	V_{SD}	I_F = 30 A, V_{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, di/dt = 100 A/µs		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	Q_{rr}			0.52	1.2	µC

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

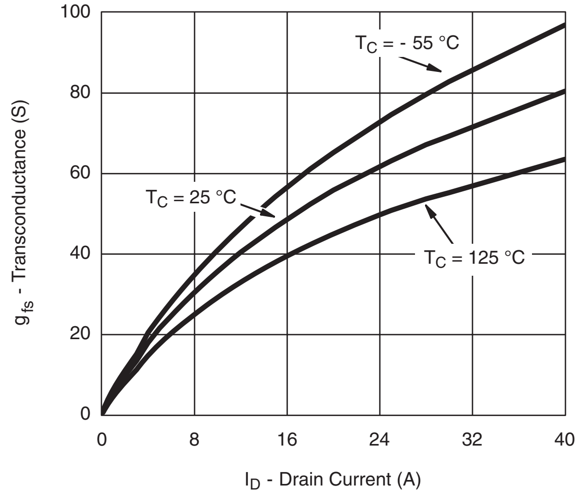
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



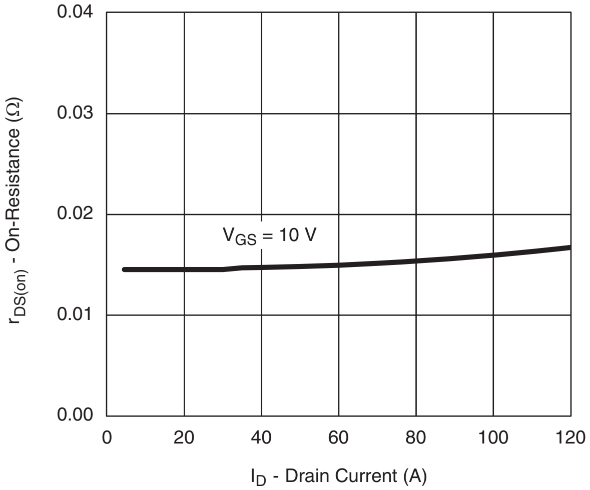
Output Characteristics



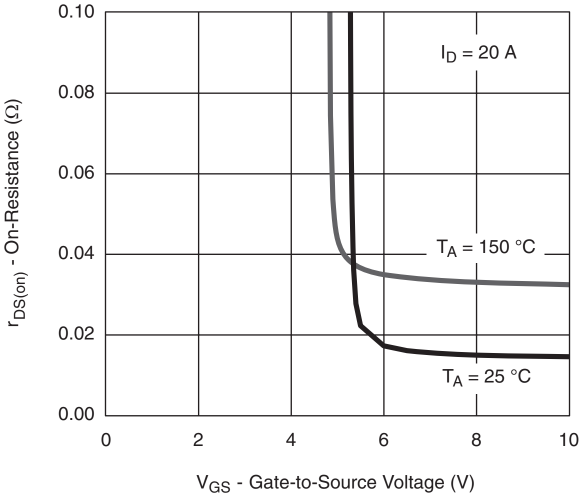
Transfer Characteristics



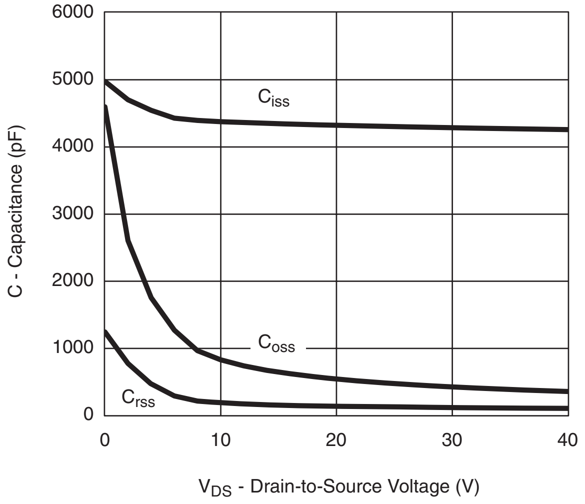
Transconductance



On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage



Capacitance

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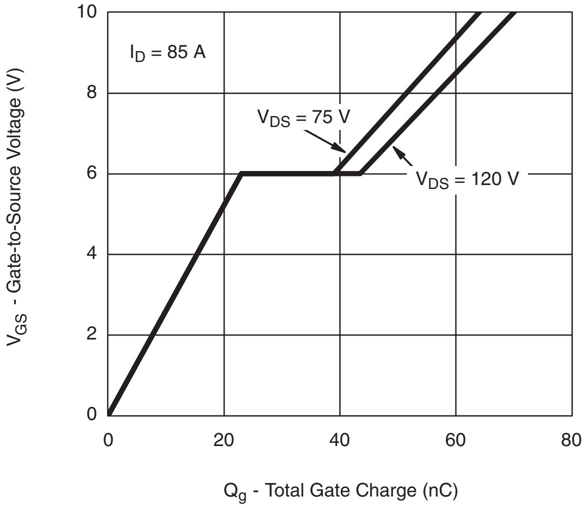
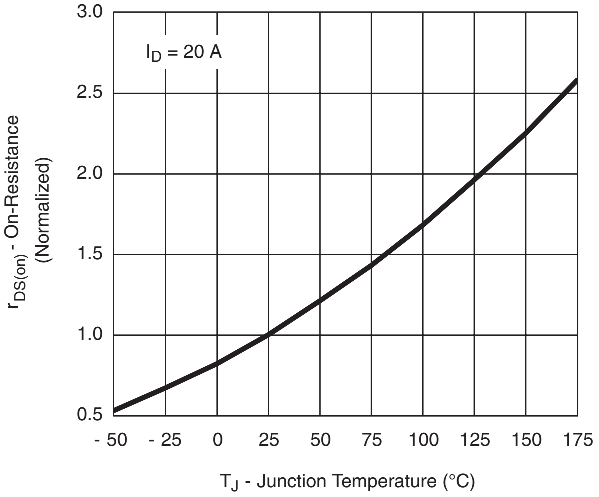
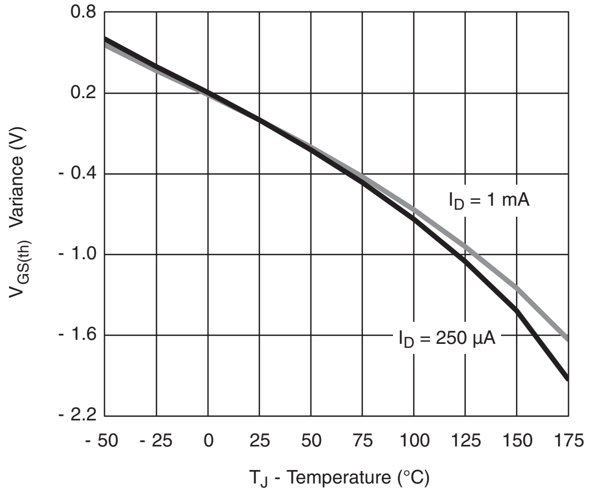


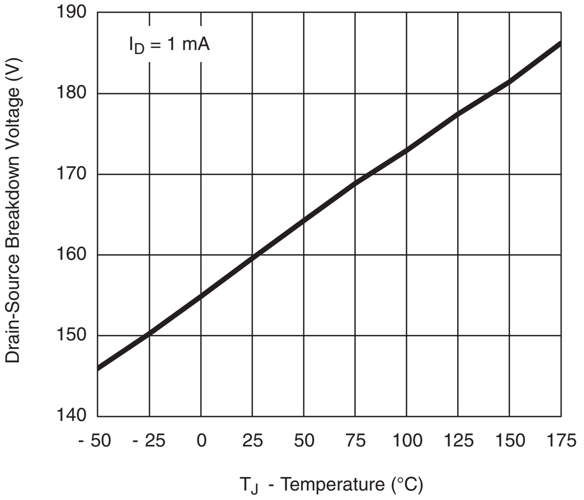
Gate Charge



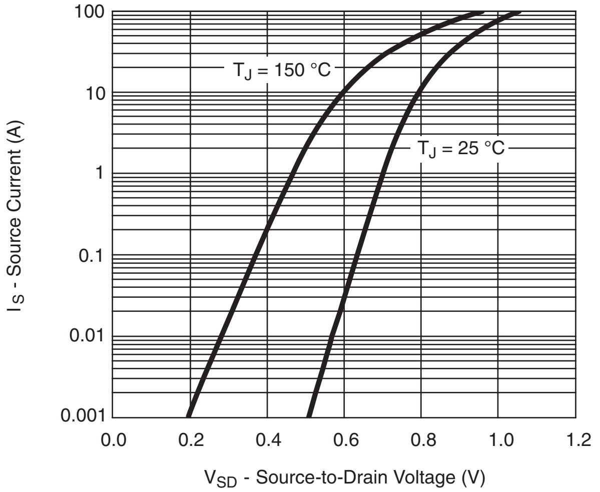
On-Resistance vs. Junction Temperature



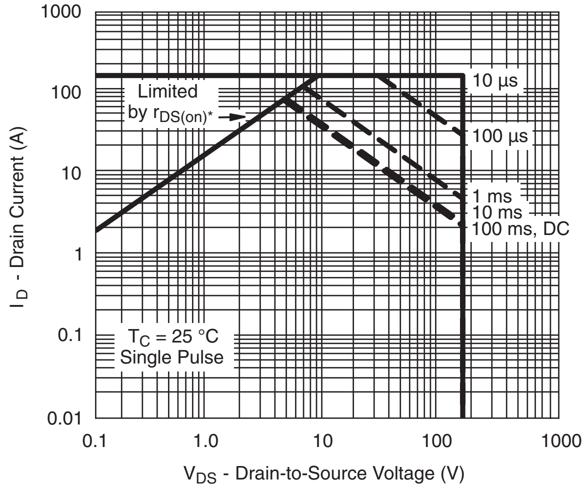
Threshold Voltage



Drain-Source Breakdown vs. Junction Temperature



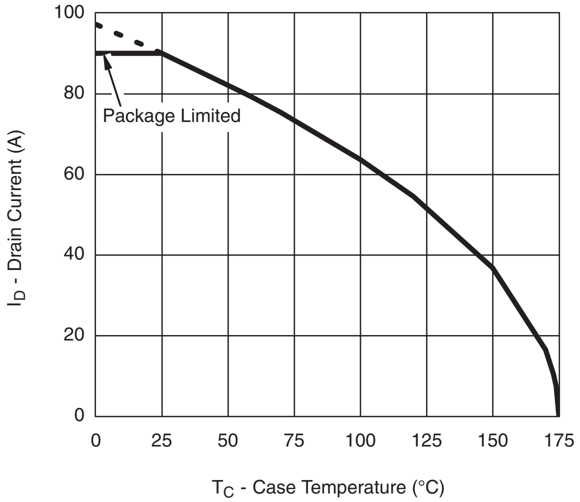
Source-Drain Diode Forward Voltage



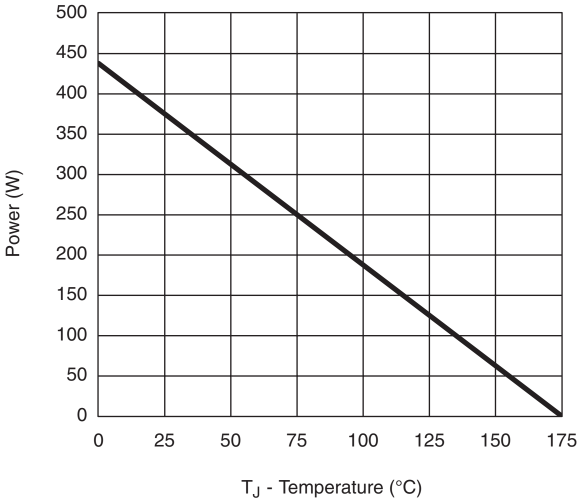
* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

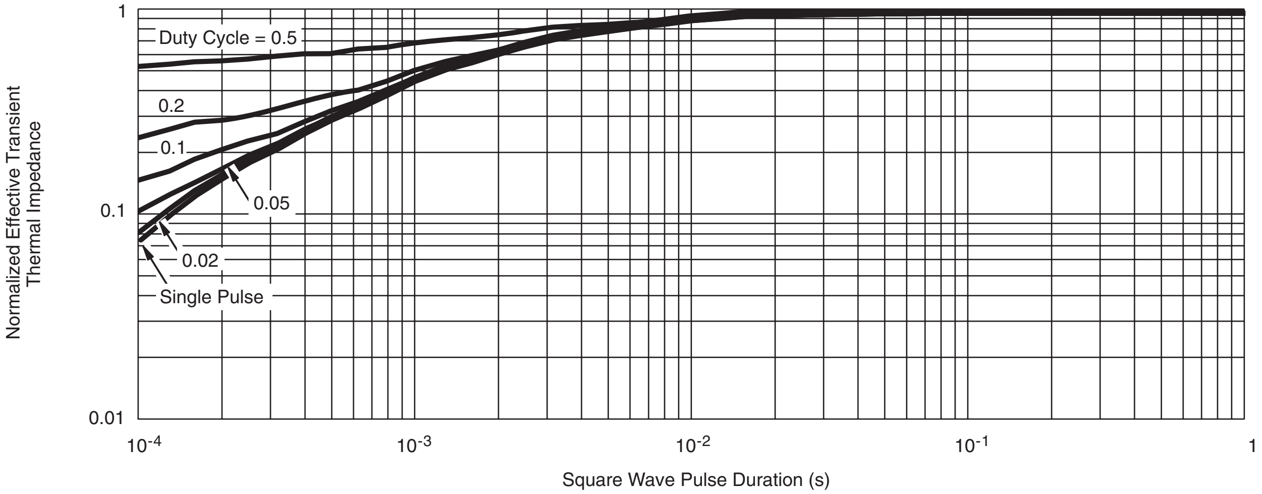
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*, Junction-to-Case



Power Derating*, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Notice