



N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
25	0.004 at V _{GS} = 10 V	28.6	29 nC
	0.0052 at V _{GS} = 4.5 V	25.6	

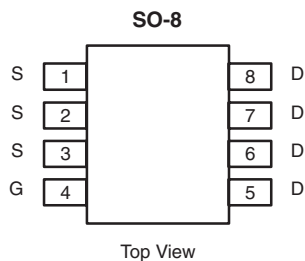
FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested

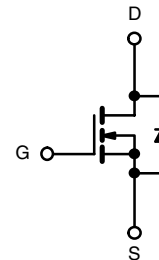
RoHS
COMPLIANT

APPLICATIONS

- Synchronous Buck-Low Side
- Notebook, Game Console
- Synchronous Rectifier-POL



Ordering Information: Si4654DY-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	25	V
Gate-Source Voltage		V _{GS}	± 16	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	28.6	A
	T _C = 70 °C		23	
	T _A = 25 °C		18.6 ^{b, c}	
	T _A = 70 °C		14.9 ^{b, c}	
Pulsed Drain Current		I _{DM}	70	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	5.1	
	T _A = 25 °C		2.2 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	30	
Avalanche Energy		E _{AS}	45	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	5.9	W
	T _C = 70 °C		3.8	
	T _A = 25 °C		2.5 ^{b, c}	
	T _A = 70 °C		1.6 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	37	50	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 85 °C/W.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		26		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		0.0032	0.004	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.004	0.0052	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		100		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3770		pF
Output Capacitance	C_{oss}			560		
Reverse Transfer Capacitance	C_{rss}			255		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		63	100	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		29	45	
Gate-Source Charge	Q_{gs}			8.5		
Gate-Drain Charge	Q_{gd}		7.2			
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.9	1.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		30	50	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			50	90	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		12	24	
Rise Time	t_r			8	16	
Turn-Off Delay Time	$t_{d(off)}$			38	70	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			5.1	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 3\text{ A}$		0.73	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		32	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			26	55	nC
Reverse Recovery Fall Time	t_a			16		ns
Reverse Recovery Rise Time	t_b			16		

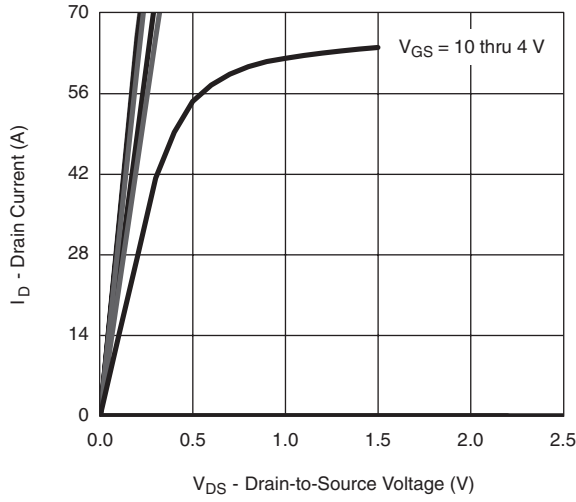
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

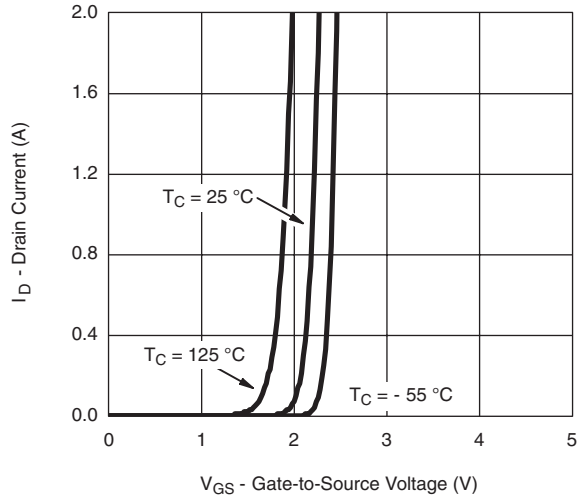
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



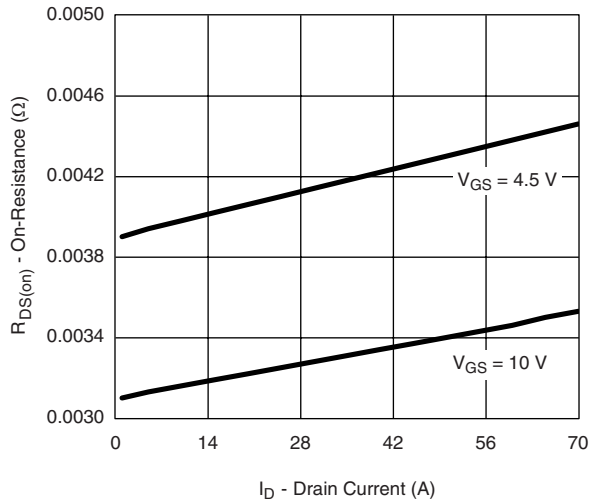
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



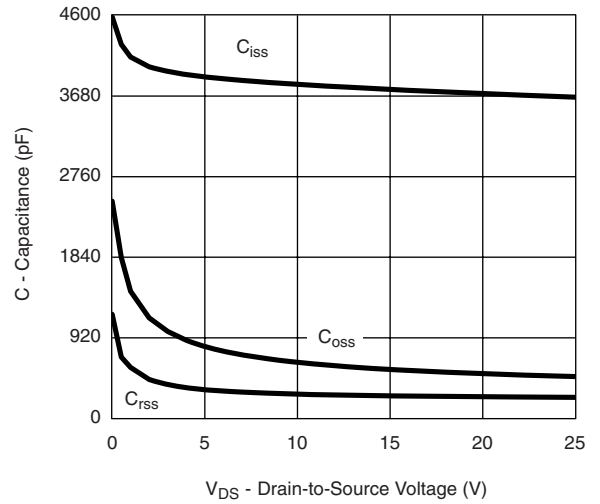
Output Characteristics



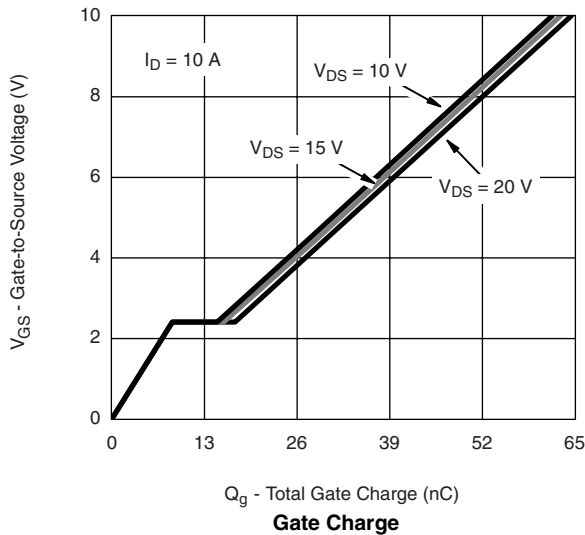
Transfer Characteristics



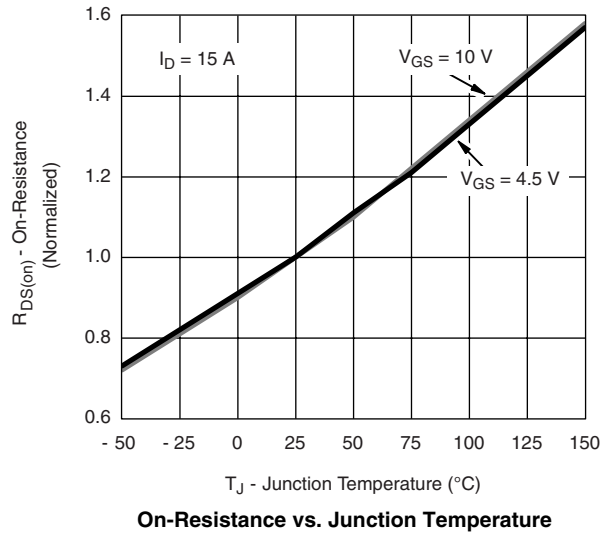
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



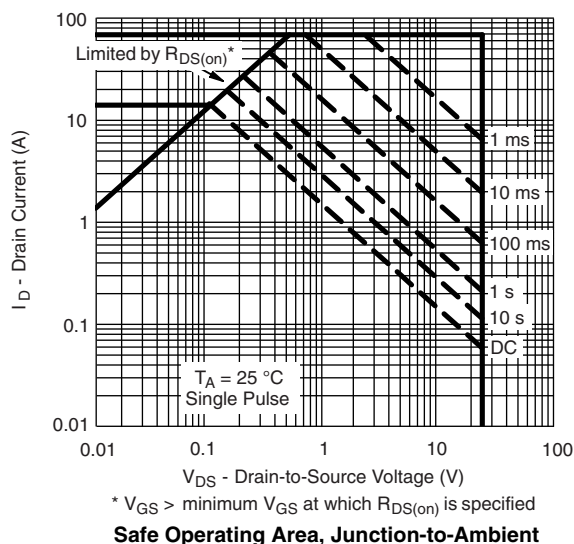
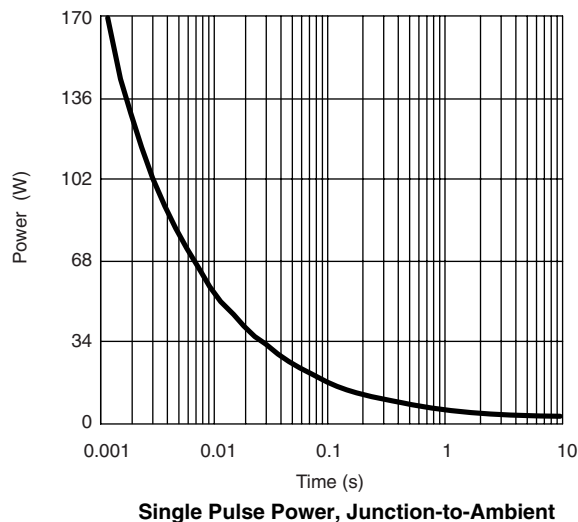
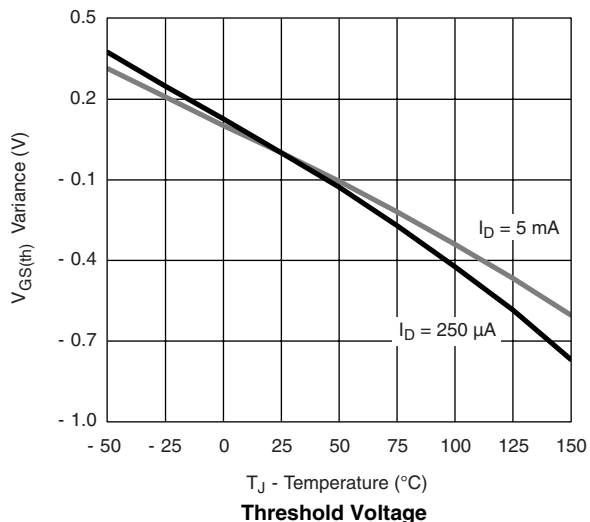
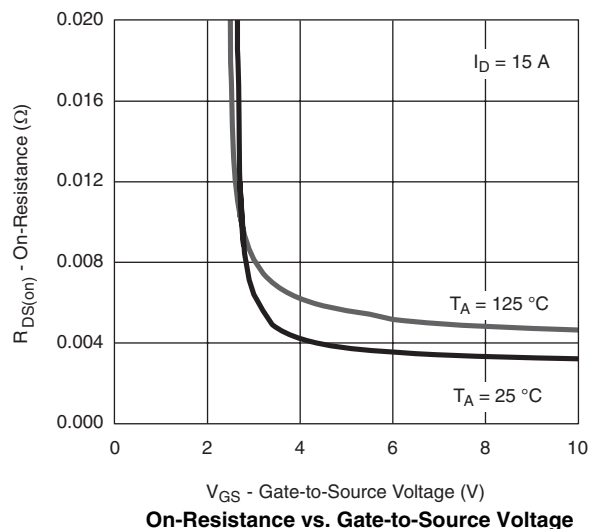
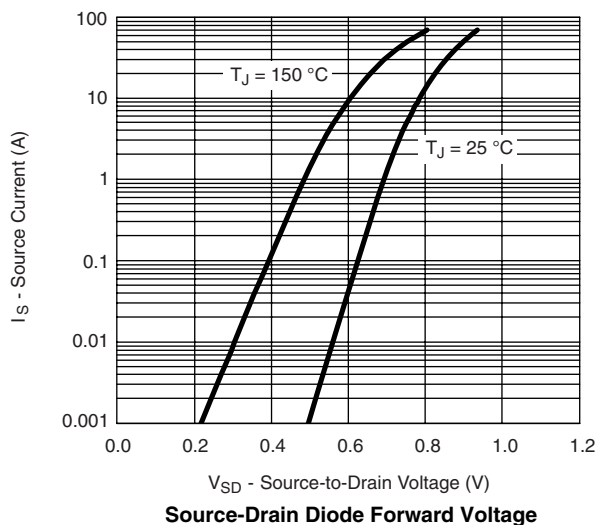
Gate Charge



On-Resistance vs. Junction Temperature

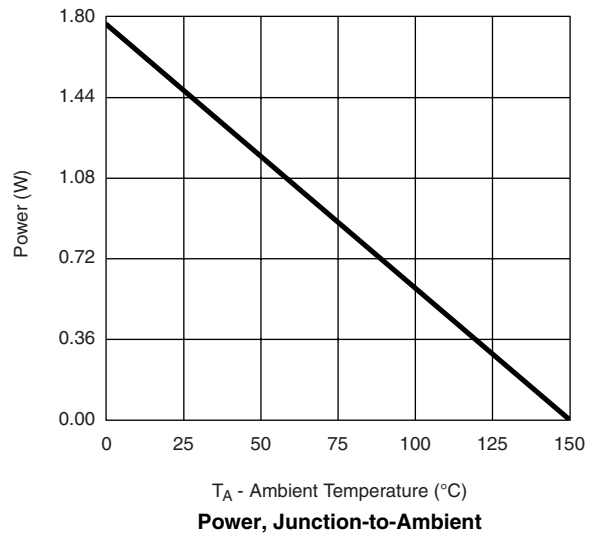
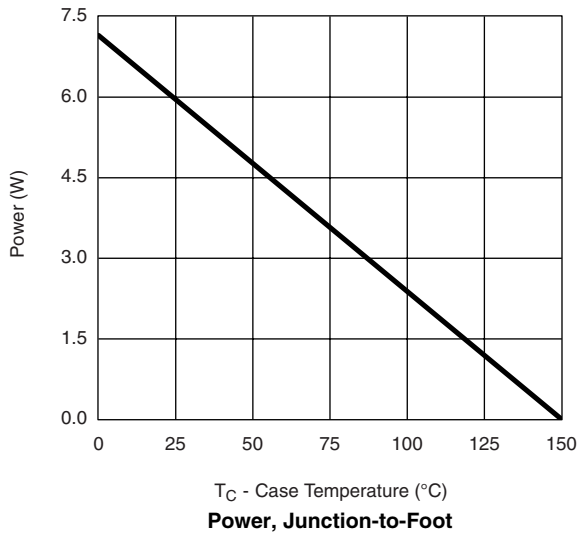
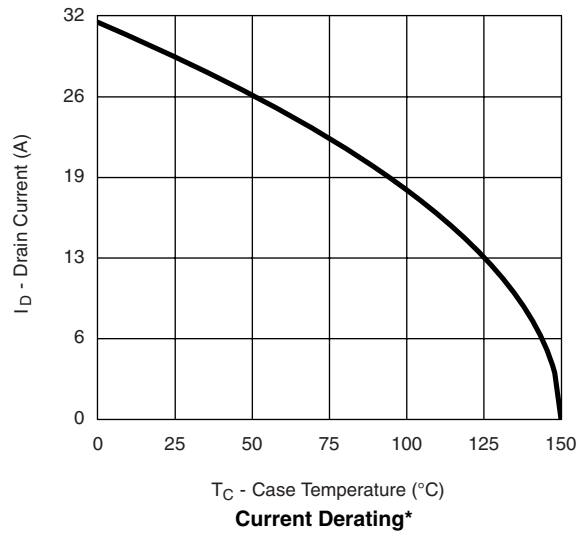


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





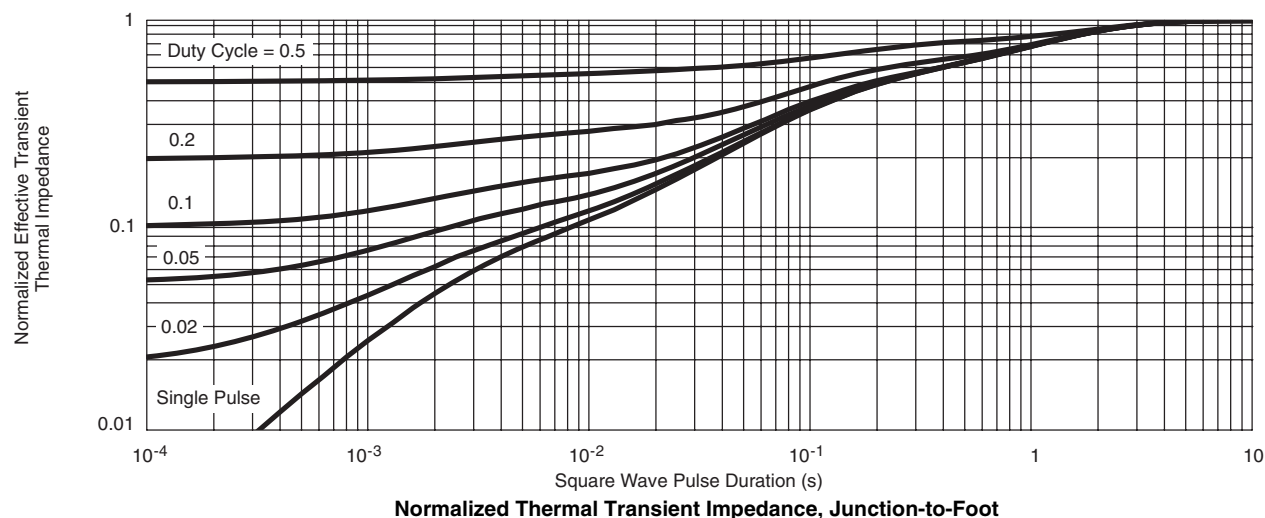
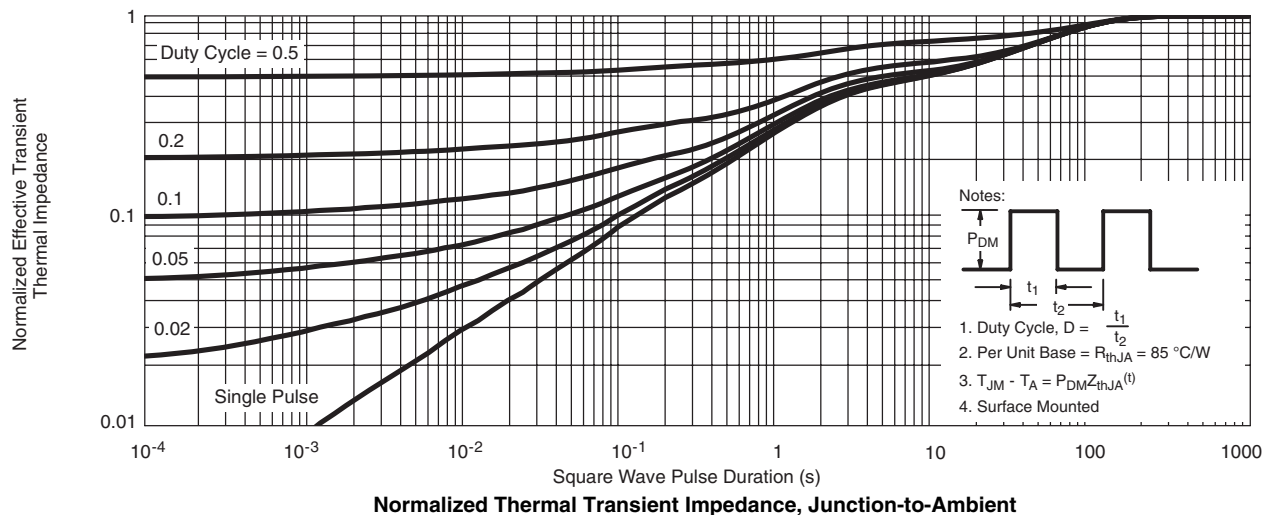
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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