N-Channel 20-V (D-S) MOSFET with Schottky Diode

MOSFET PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ)
20	0.039 @ V_{GS} = 4.5 V	6	6 nC
	0.045 @ V_{GS} = 2.5 V	6	
	0.055 @ V_{GS} = 1.8 V	6	

SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A)[a]
20	0.375 @ 1 A	1

FEATURES

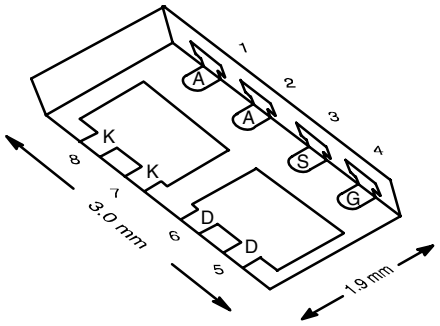
- LITTLE FOOT® *Plus* Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
  - Small Footprint Area
  - Low On–Resistance
  - Thin 0.8mm Profile

Pb-free
RoHS COMPLIANT

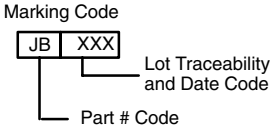
APPLICATIONS

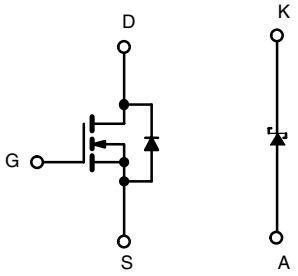
- Load Switch for Portable Applications
  - Ideal for Boost Circuits

PowerPAK® ChipFET® Dual



Bottom View





N-Channel MOSFET

Ordering Information: Si5858DU-T1–E3 (Lead (Pb) Free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage (MOSFET)		V_{DS}	20	V
Reverse Voltage (Schottky)		V_{KA}	20	
Gate-Source Voltage (MOSFET)		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C) (MOSFET)	T_C = 25°C	I_D	6[a]	A
	T_C = 70°C		6[a]	
	T_A = 25°C		7.2[b, c]	
	T_A = 70°C		5.8[b, c]	
Pulsed Drain Current (MOSFET)		I_{DM}	20	
Continuous Source Current (MOSFET Diode Conduction)	T_C = 25°C	I_S	6.9	
	T_A = 25°C		1.9[b, c]	
Average Foward Current (Schottky)		I_F	1[b]	
Pulsed Foward Current (Schottky)		I_{FM}	7	
Maximum Power Dissipation (MOSFET)	T_C = 25°C	P_D	8.3	W
	T_C = 70°C		5.3	
	T_A = 25°C		2.3[b, c]	
	T_A = 70°C		1.5[b, c]	
Maximum Power Dissipation (Schottky)	T_C = 25°C	P_D	7.8	W
	T_C = 70°C		5	
	T_A = 25°C		2.1	
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Soldering Recommendation (Peak Temperature)[d, e]			260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[b, f]	R_{thJA}	45	55	°C/W
Maximum Junction-to-Case (Drain) (MOSFET)	R_{thJC}	12	15	
Maximum Junction-to-Ambient (Schottky)	R_{thJA}	49	61	°C/W
Maximum Junction-to-Case (Drain) (Schottky)	R_{thJC}	13	16	

Notes
a. Package limited.
b. Surface Mounted on FR4 Board.
c. t ≤ 5 sec.
d. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions for MOSFETS is 105 °C/W.
g. Maximum under Steady state conditions for Schottky is 110 °C/W.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS/TJ}$	I_D = 250 µA		17.4		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)/TJ}$			–2.6		
Gate–Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	ns
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			–1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C			–10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ 5 V, V_{GS} = 4.5 V	–20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.4 A		0.032	0.039	Ω
		V_{GS} = 2.5 V, I_D = 4.1 A		0.037	0.045	
		V_{GS} = 1.8 V, I_D = 1.8 A		0.0455	0.055	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.4 A		22		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		520		pF
Output Capacitance	C_{oss}			100		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 8 V, I_D = 4.4 A		10.5	16	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.4 A		6	9	
Gate-Source Charge	Q_{gs}			0.91		
Gate-Drain Charge	Q_{gd}			0.7		
Gate Resistance	R_g	f = 1 MHz		1.9		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 2.8 Ω I_D ≅ 3.6 A, V_{GEN} = 4.5 V, R_g = 1 Ω		20	30	ns
Rise Time	t_r			65	100	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time				10	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 2.8 Ω I_D ≅ 3.6 A, V_{GEN} = 8 V, R_g = 1 Ω		5	10	
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			26	40	
Fall Time	t_f			8	15	

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			14.8	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	I_S = 1.2 A, V_{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = –2 A, di/dt = 100 A/µs, T_J = 25 °C		45	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}			21	32	nC
Reverse Recovery Fall Time	t_a			29		ns
Reverse Recovery Rise Time	t_b			16		

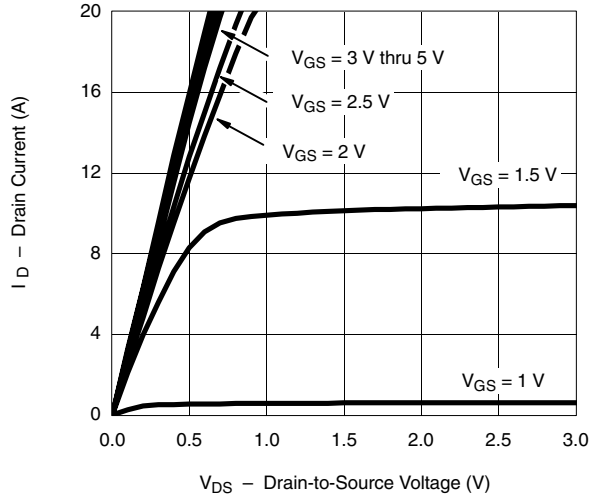
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

SCHOTTKY SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Forward Voltage Drop	V_F	I_F = 1 A		0.34	0.375	V
		I_F = 1 A, T_J = 125°C		0.255	0.290	
Maximum Reverse Leakage Current	I_{rm}	V_r = 20 V		0.05	0.500	mA
		V_r = 20 V, T_J = 85°C		2	20	
		V_r = 20 V, T_J = 125°C		10	100	
Junction Capacitance	C_T	V_r = 10 V		90		pF

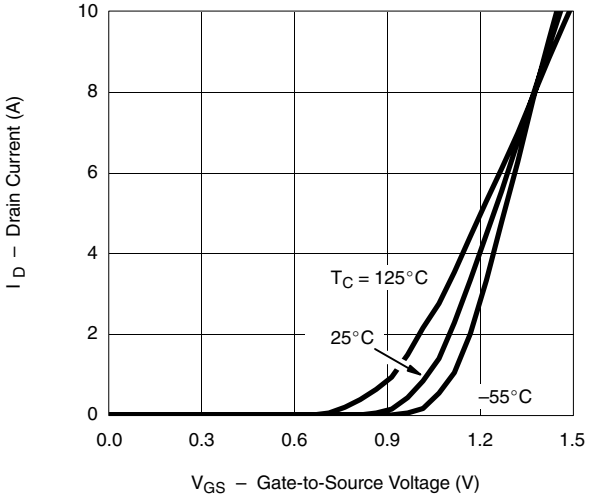
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) MOSFET

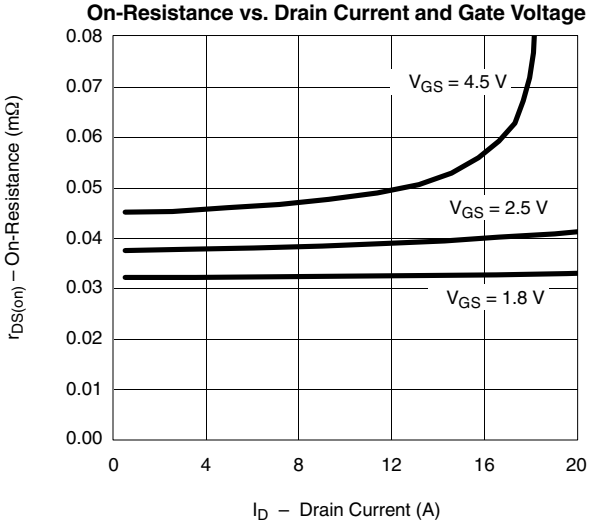
Output Characteristics



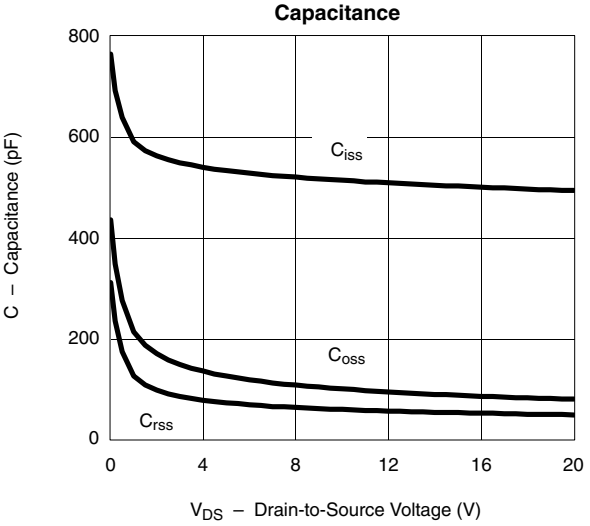
Transfer Characteristics



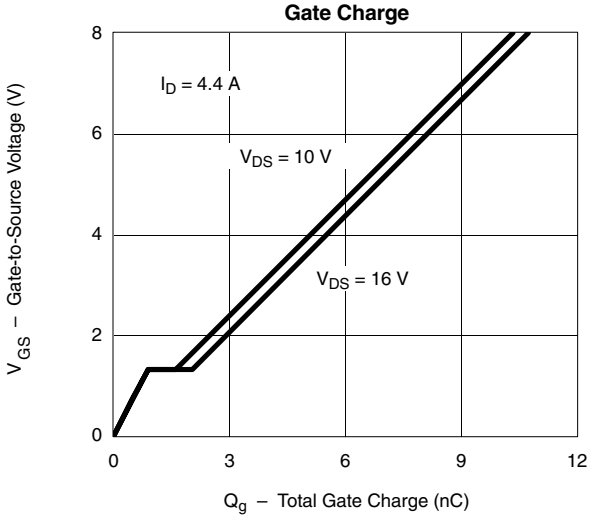
On-Resistance vs. Drain Current and Gate Voltage



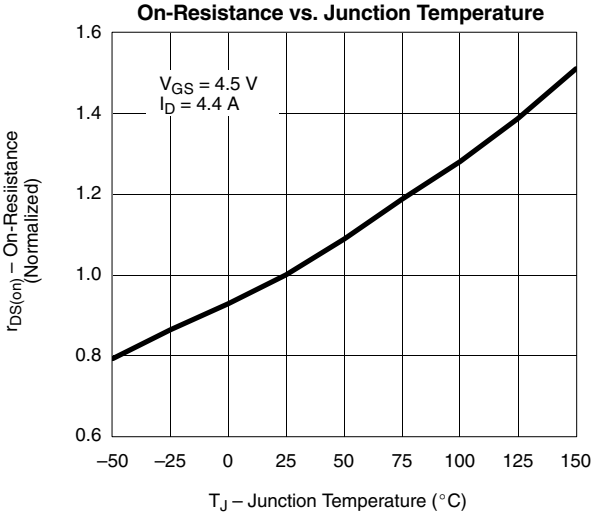
Capacitance



Gate Charge

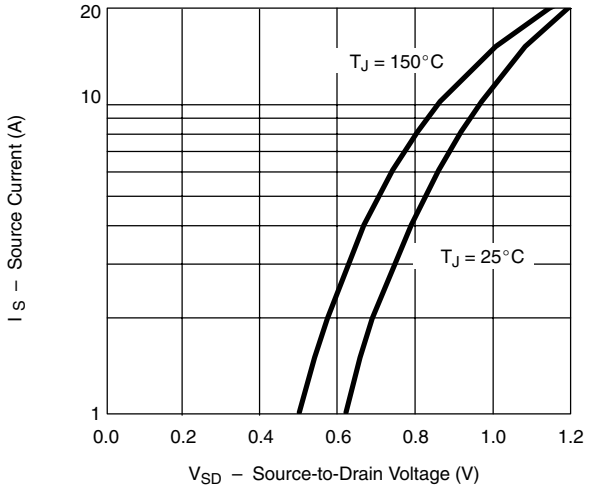


On-Resistance vs. Junction Temperature

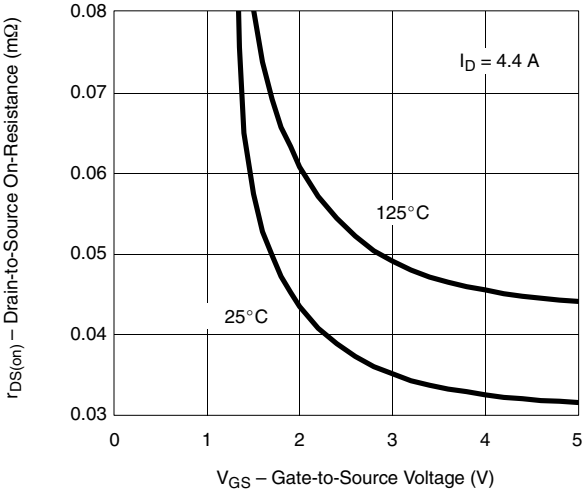


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) MOSFET

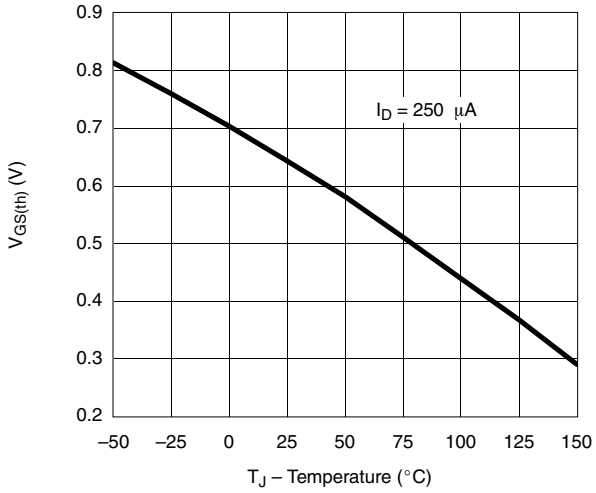
Source-Drain Diode Forward Voltage



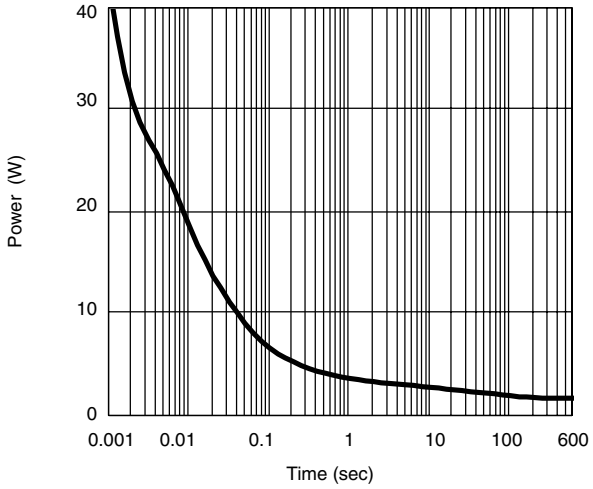
On-Resistance vs. Gate-to-Source Voltage



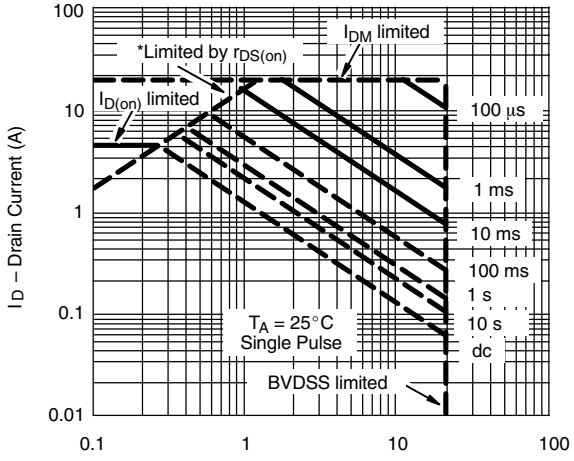
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



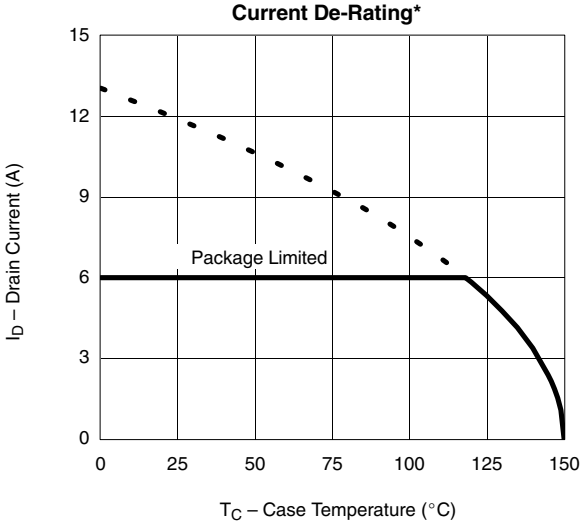
Safe Operating Area, Junction-to-Ambient



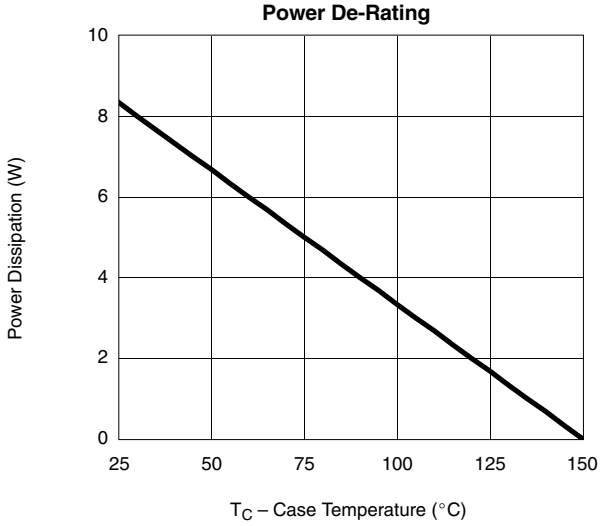
*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) MOSFET

Current De-Rating*



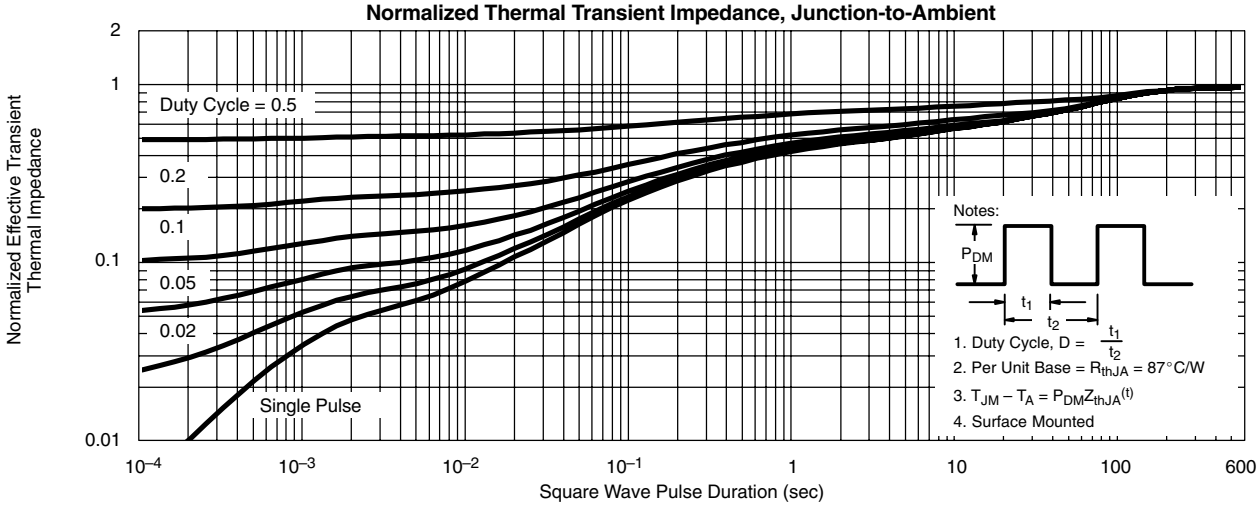
Power De-Rating



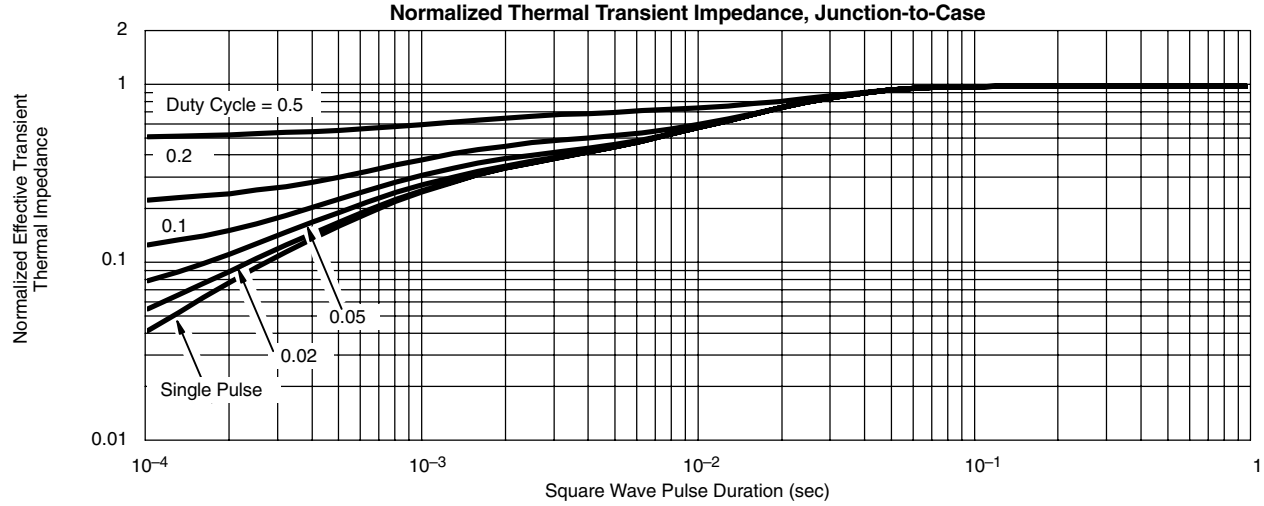
*The power dissipation P_D is based on $T_{J(max)}$ = 150°C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) MOSFET

Normalized Thermal Transient Impedance, Junction-to-Ambient

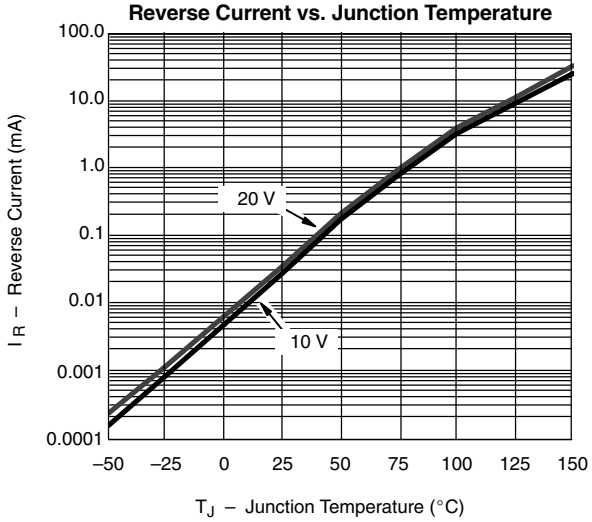


Normalized Thermal Transient Impedance, Junction-to-Case

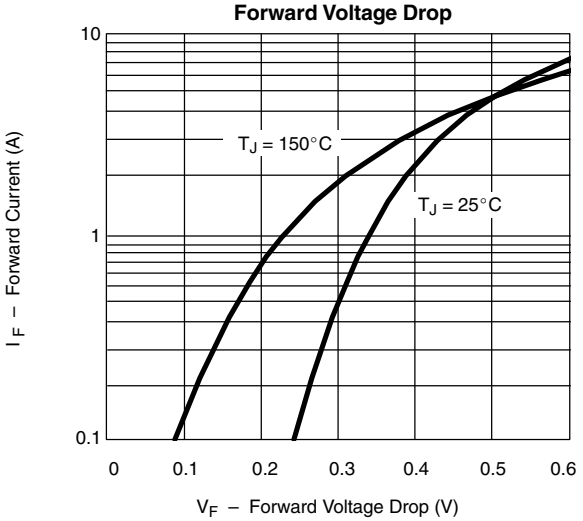


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) SCHOTTKY

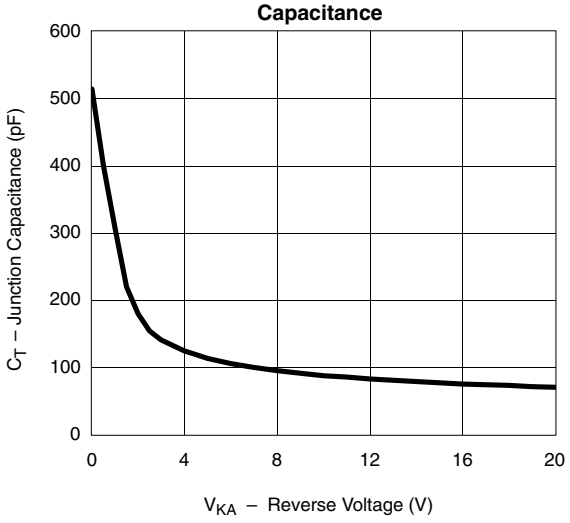
Reverse Current vs. Junction Temperature



Forward Voltage Drop

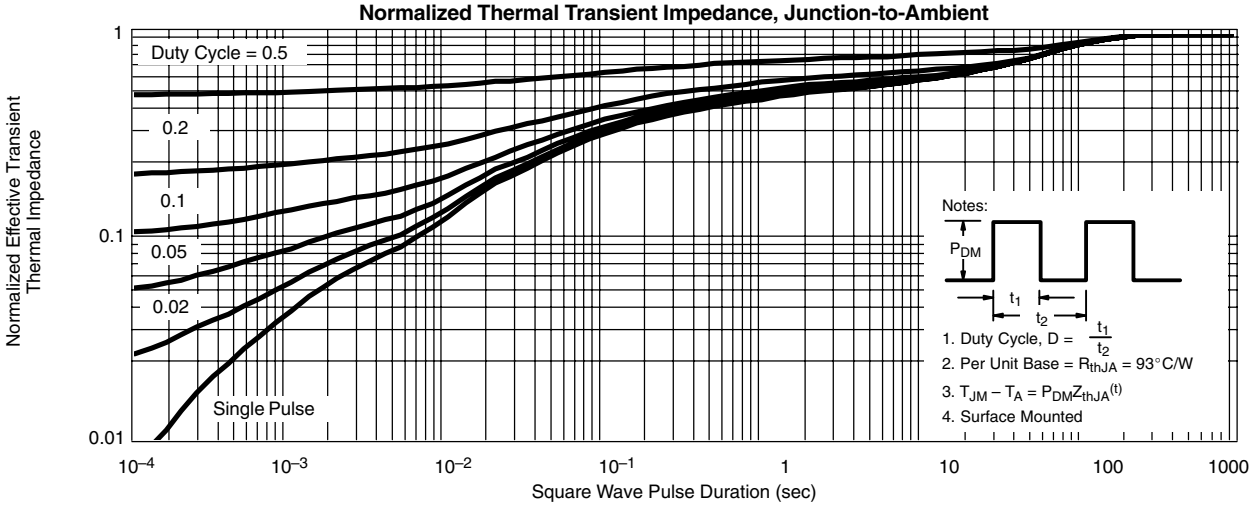


Capacitance

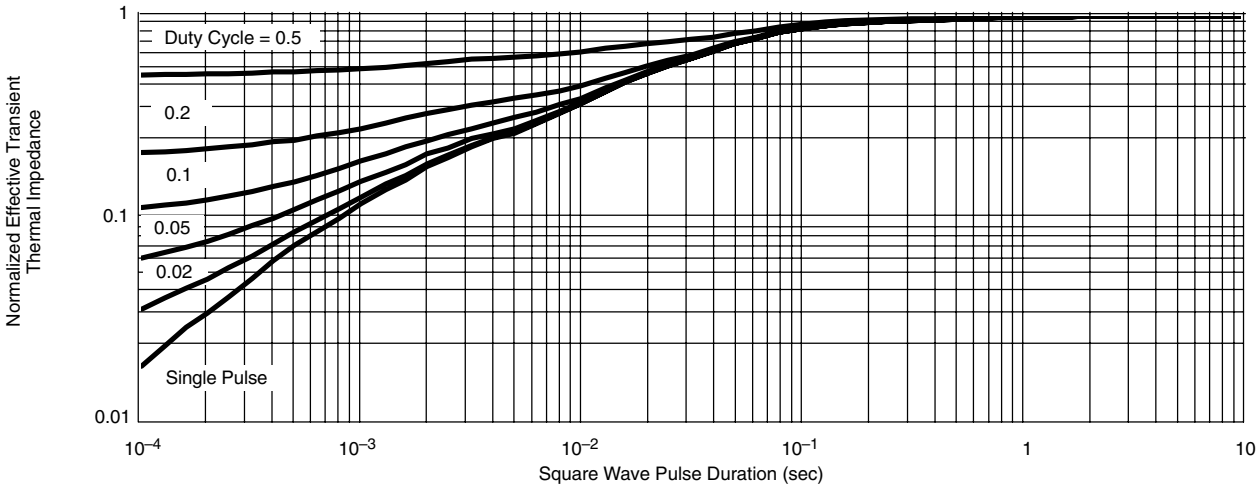


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) SCHOTTKY

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



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