

N-Channel 20-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
20	0.0049 at V _{GS} = 10 V	22	20
	0.0061 at V _{GS} = 4.5 V	19.7	

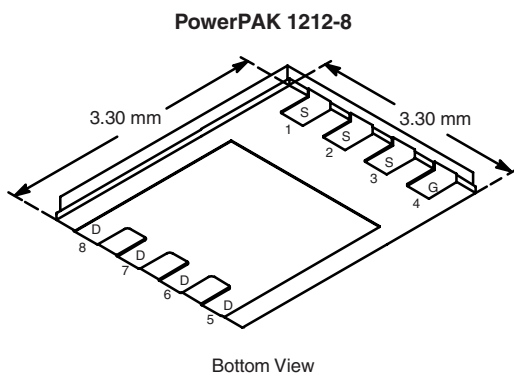
FEATURES

- Halogen-free Option Available
- TrenchFET[®] Gen II Power MOSFET for Ultra Low On-Resistance
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g Tested



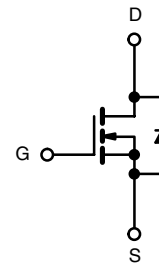
APPLICATIONS

- Synchronous Rectification
- Point-of-Load Converters
- Protection Devices
- Hot Swap



Bottom View

Ordering Information: Si7108DN-T1-E3 (Lead (Pb)-free)
Si7108DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V _{DS}	20		V
Gate-Source Voltage	V _{GS}	± 16		
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	22	14
		T _A = 70 °C	17.6	11.2
Pulsed Drain Current	I _{DM}	60		A
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3	
Single Avalanche Current	I _{AS}	22		mJ
Single Avalanche Energy	E _{AS}	24		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8	1.5
		T _A = 70 °C	2.0	0.8
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	24	33
		Steady State	65	81
Maximum Junction-to-Case (Drain)	R _{thJC}	1.9	2.4	°C/W

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Reliability Manual for profile. The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



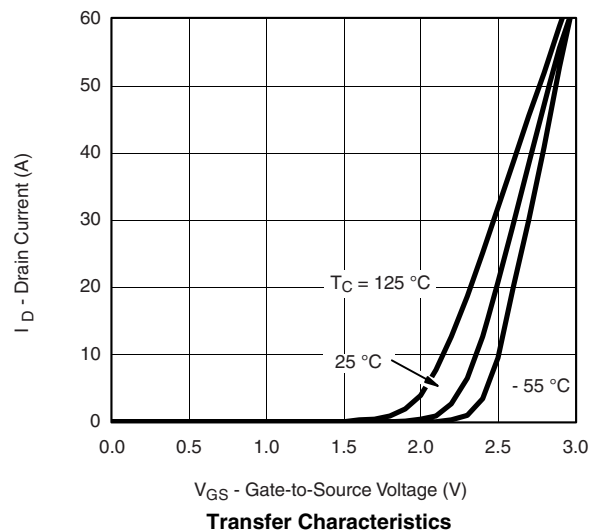
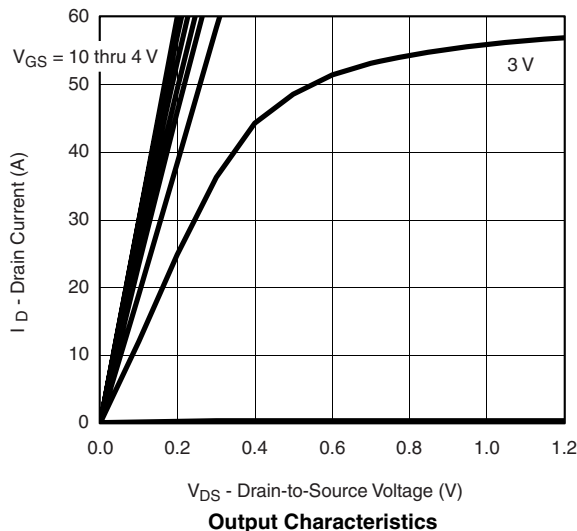
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1		2	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 22 \text{ A}$		0.0041	0.0049	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 19.7 \text{ A}$		0.005	0.0061	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 22 \text{ A}$		88		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 22 \text{ A}$		20	30	nC
Gate-Source Charge	Q_{gs}			6.3		
Gate-Drain Charge	Q_{gd}			4.9		
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.7	1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20 \text{ V}, R_L = 20 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		10	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			60	130	
Fall Time	t_f			10	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		30	60	nC
Reverse Recovery Charge	Q_{rr}			20	36	

Notes:

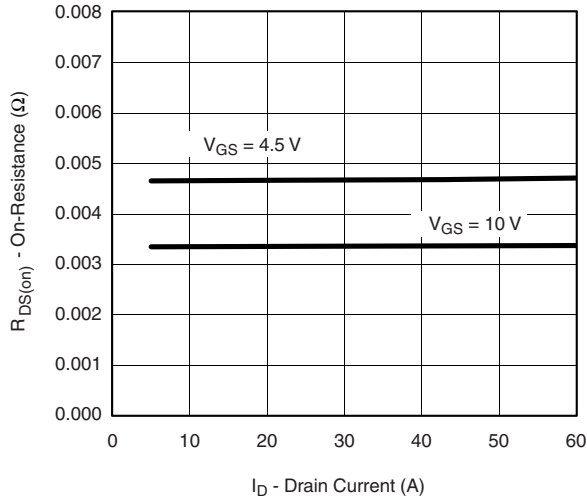
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

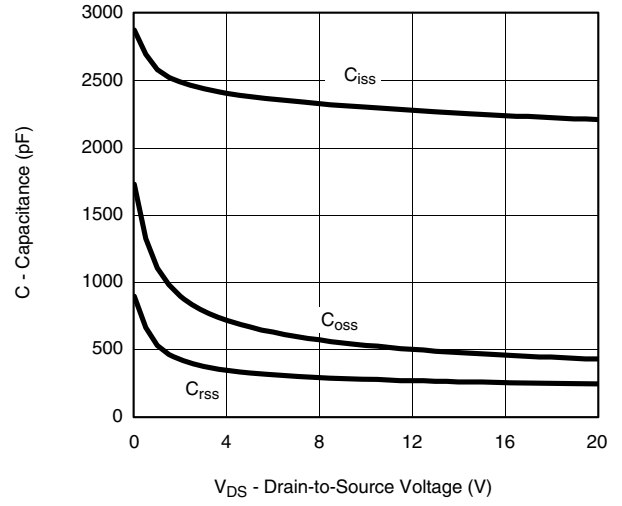
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted



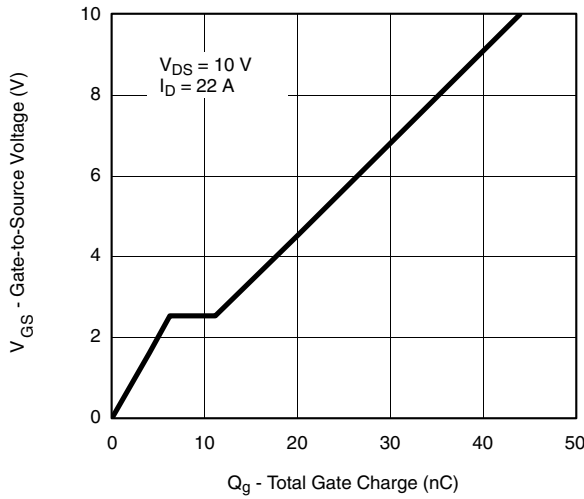
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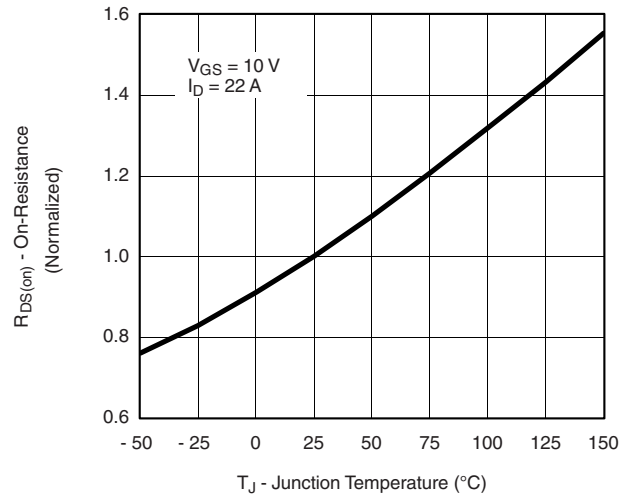
On-Resistance vs. Drain Current



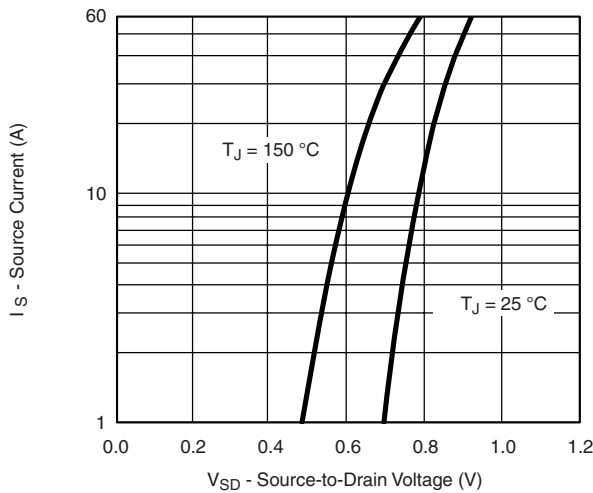
Capacitance



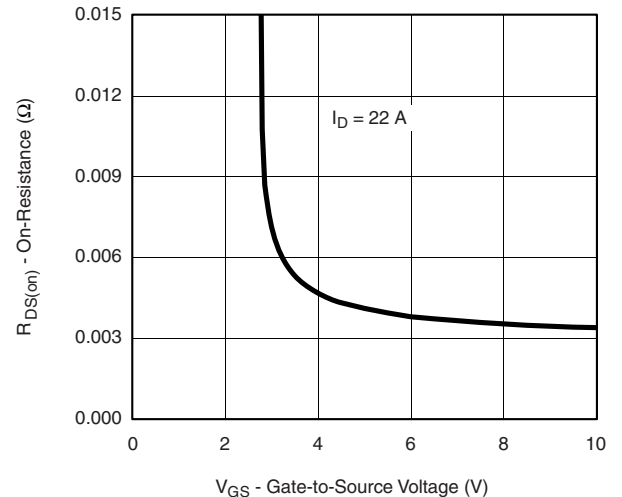
Gate Charge



On-Resistance vs. Junction Temperature

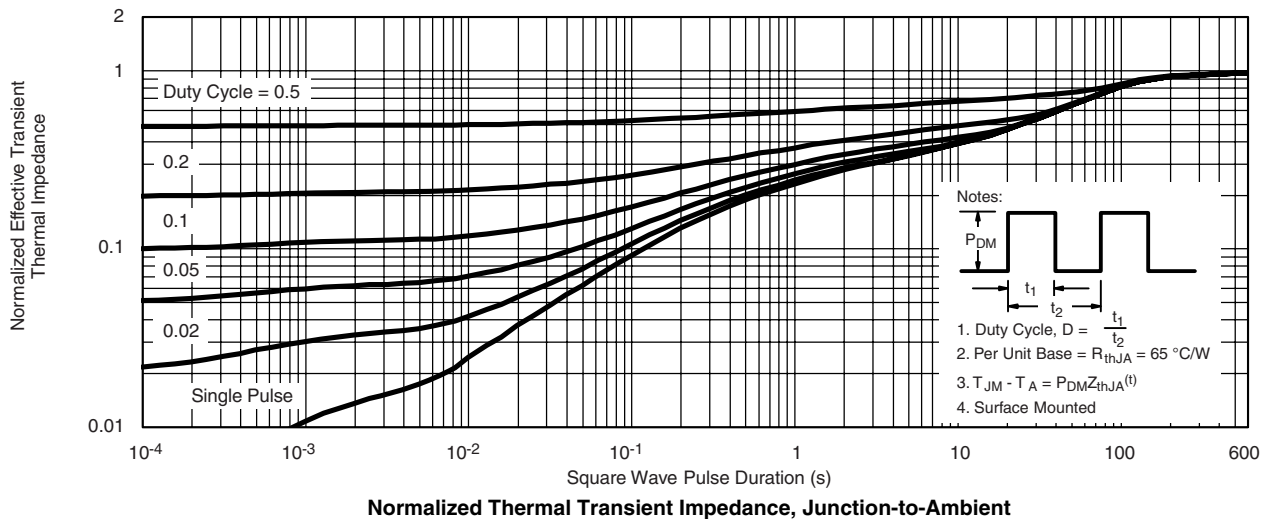
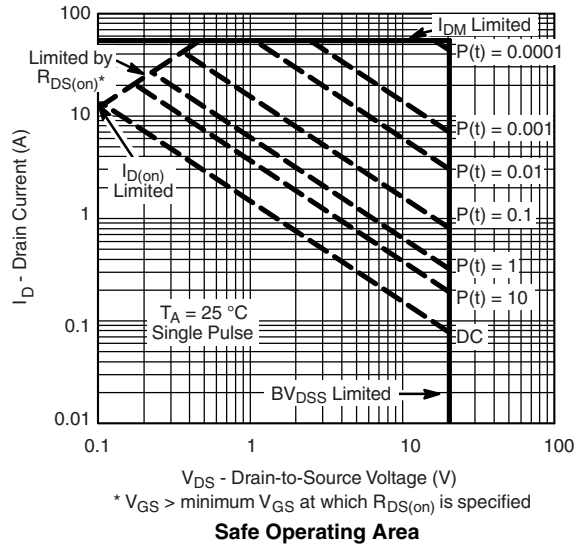
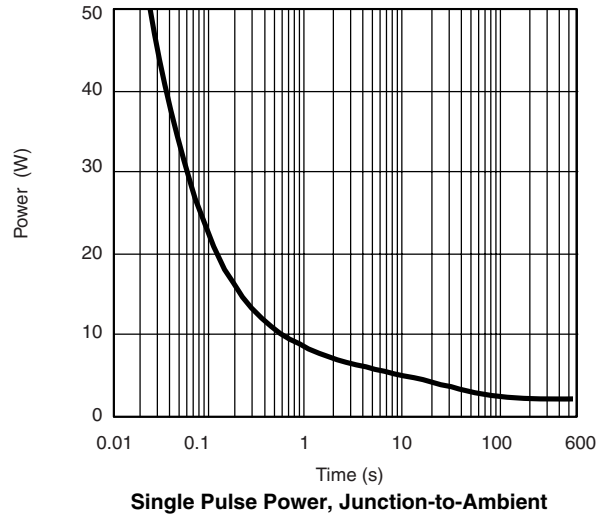
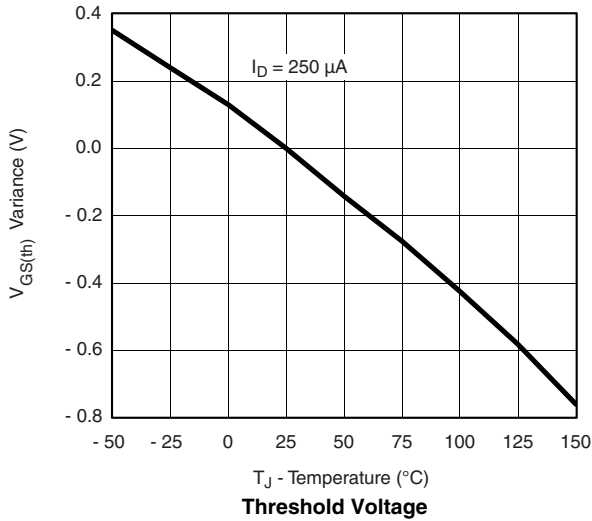


Source-Drain Diode Forward Voltage

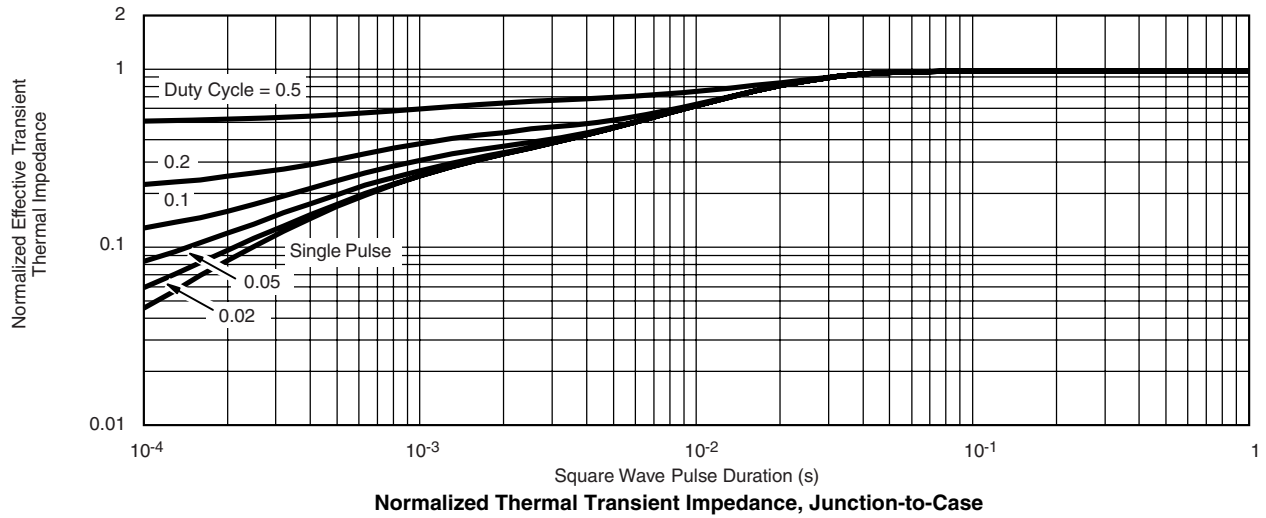


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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