

N-Channel 20-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
20	0.0053 at V _{GS} = 10 V	21.1	14 nC
	0.0078 at V _{GS} = 4.5 V	17.4	

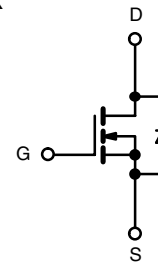
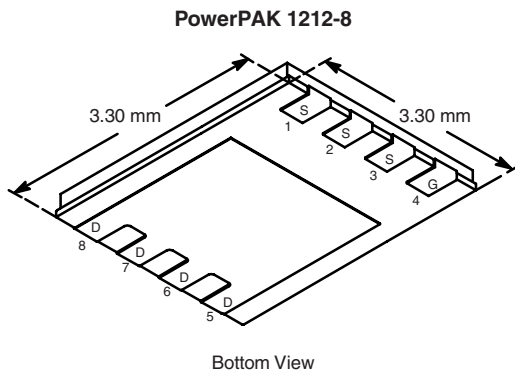
FEATURES

- Halogen-free Option Available
- TrenchFET[®] Gen II Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- PWM Optimized
- 100 % R_g Tested



APPLICATIONS

- Synchronous Rectification
- Synchronous Buck



N-Channel MOSFET

Ordering Information: Si7110DN-T1-E3 (Lead (Pb)-free)
Si7110DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V _{DS}	20		V
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	21.1	13.5
		T _A = 70 °C	16.9	10.8
Pulsed Drain Current	I _{DM}	60		A
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3	
Single Avalanche Current	L = 0.1 mH	I _{AS}	35	
Single Avalanche Energy			E _{AS}	61
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8	1.5
		T _A = 70 °C	2.0	0.8
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	24	33
		Steady State	65	81
Maximum Junction-to-Case (Drain)	R _{thJC}	1.9	2.4	°C/W

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

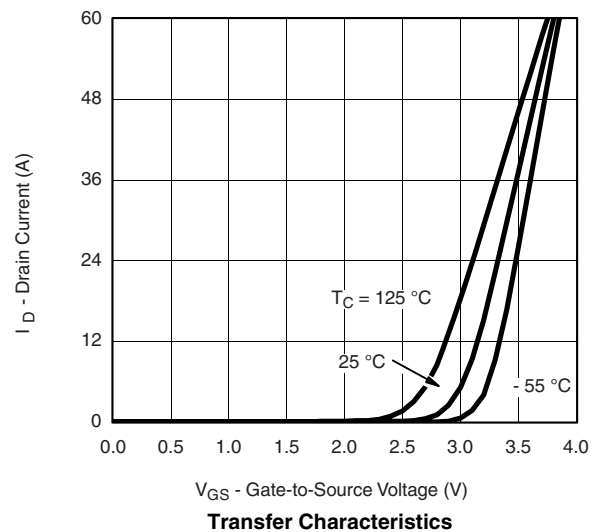
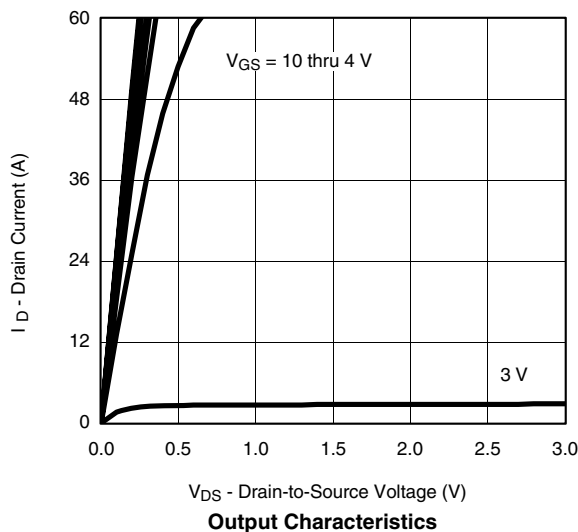
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5		2.5	V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA	
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55\text{ }^\circ\text{C}$			5		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	40			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 21.1\ \text{A}$		0.0044	0.0053	Ω	
		$V_{GS} = 4.5\ \text{V}, I_D = 17.4\ \text{A}$		0.0064	0.0078		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 21.1\ \text{A}$		71		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	1.2	V	
Dynamic^b							
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 21.1\ \text{A}$		14	21	nC	
Gate-Source Charge	Q_{gs}			7			
Gate-Drain Charge	Q_{gd}			4.5			
Gate Resistance	R_g	$f = 1\ \text{MHz}$	0.7	1.4	2.1	Ω	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_g = 6\ \Omega$		12	20	ns	
Rise Time	t_r			10	15		
Turn-Off Delay Time	$t_{d(off)}$			36	55		
Fall Time	t_f			10	15		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3.2\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		30	60	nC	
Body Diode Reverse Recovery Charge	Q_{rr}			25	50		
Reverse Recovery Fall Time	t_a			14			ns
Reverse Recovery Rise Time	t_b			16			

Notes:

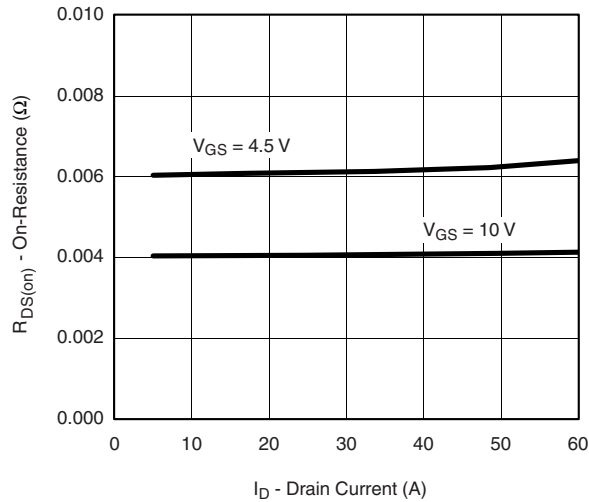
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

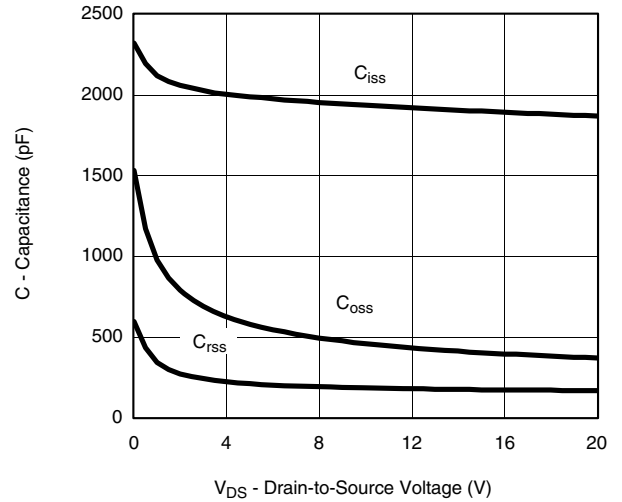
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



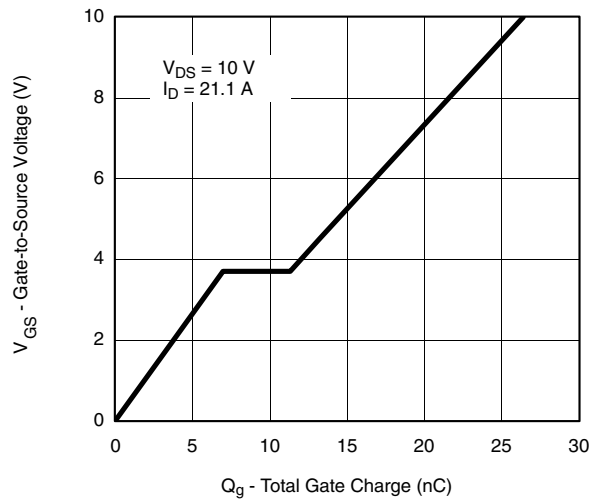
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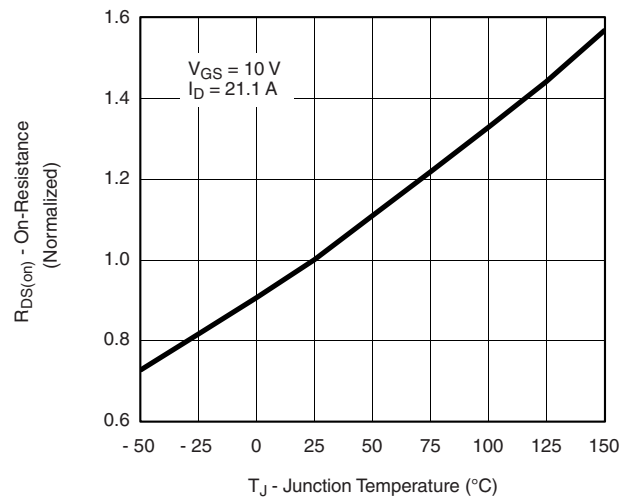
On-Resistance vs. Drain Current



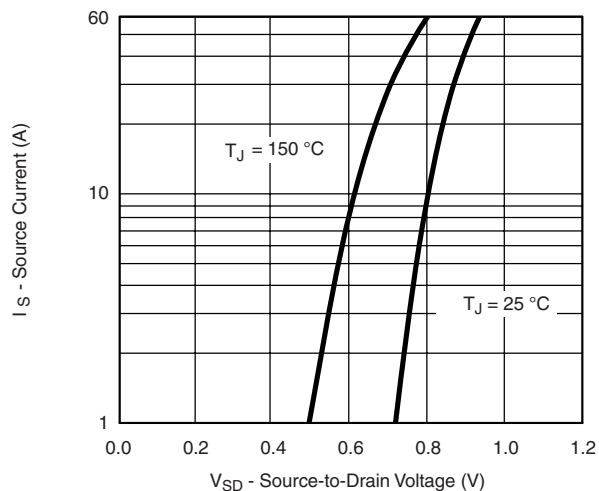
Capacitance



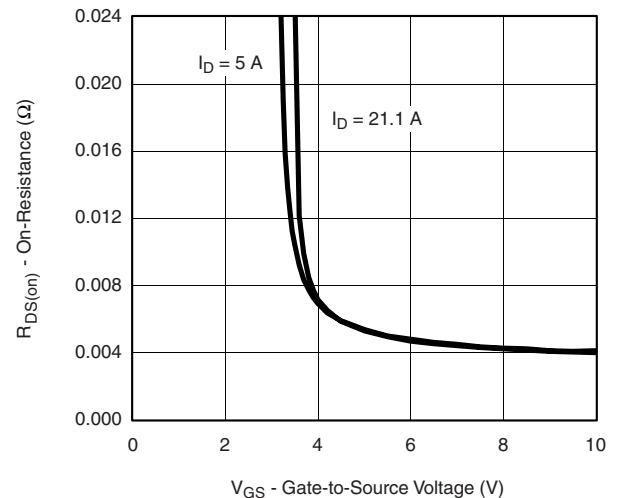
Gate Charge



On-Resistance vs. Junction Temperature

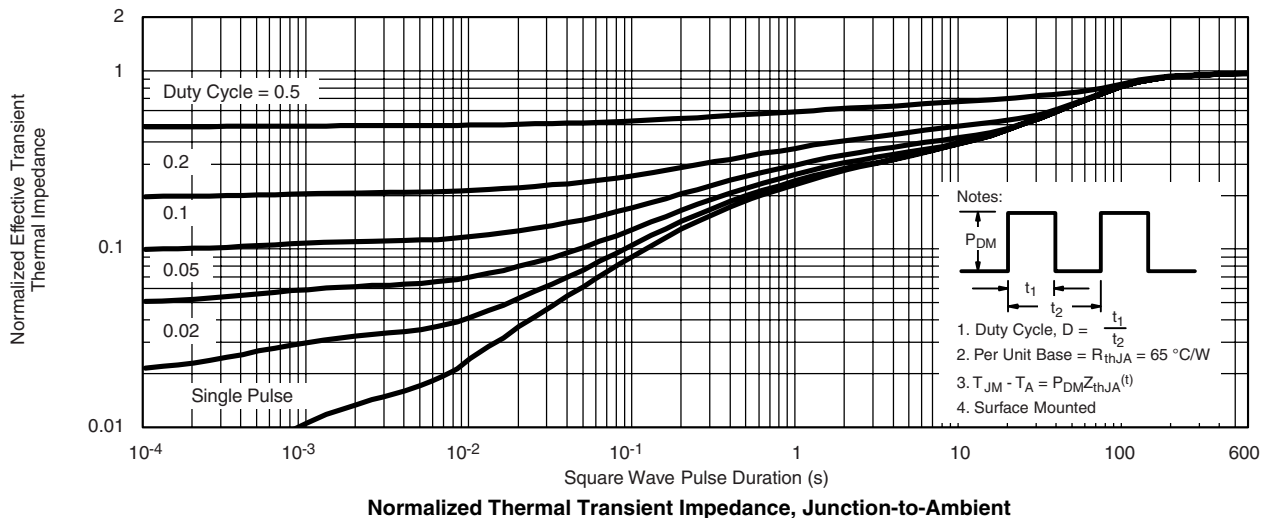
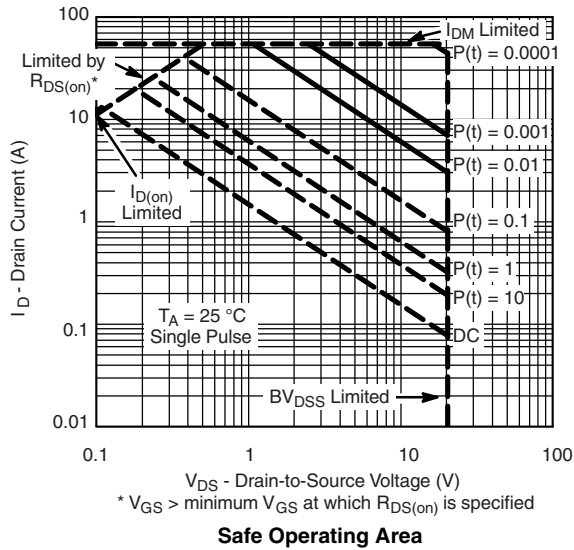
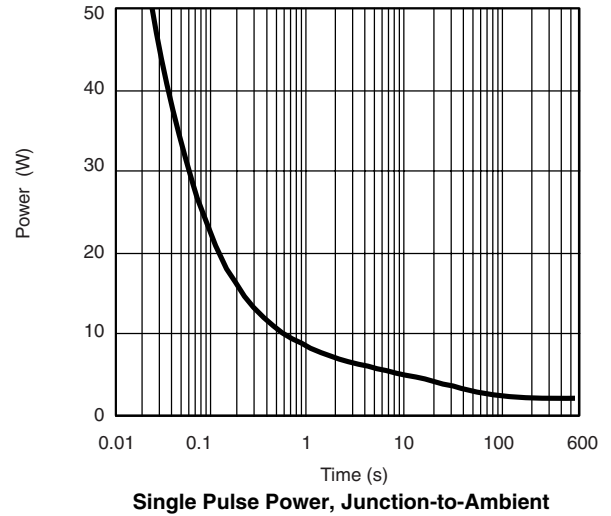
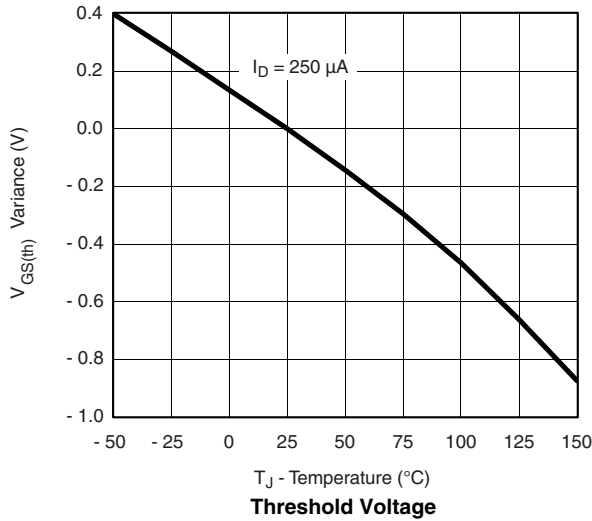


Source-Drain Diode Forward Voltage



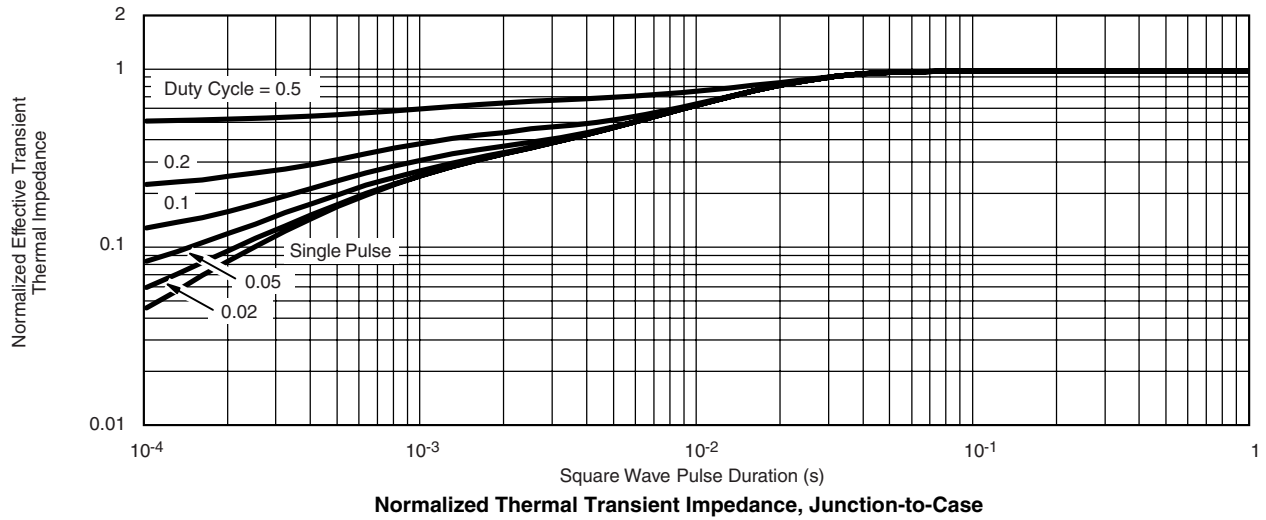
On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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