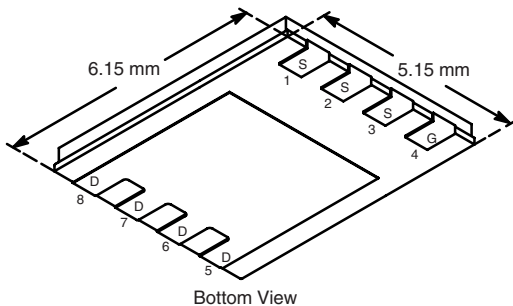




## P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
- 20	0.00195 at $V_{GS} = - 10$ V	- 60 <sup>d</sup>	183 nC
	0.0025 at $V_{GS} = - 4.5$ V	- 60 <sup>d</sup>	
	0.0039 at $V_{GS} = - 2.5$ V	- 60 <sup>d</sup>	

PowerPAK SO-8



Bottom View

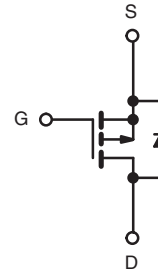
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Gen III P-Channel Power MOSFET
- 100 %  $R_g$  Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Adaptor Switch
- Battery Switch
- Load Switch



P-Channel MOSFET

**Ordering Information:** Si7137DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	- 20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$		
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	- 60 <sup>d</sup>	A
		$T_C = 70$ °C	- 60 <sup>d</sup>	
		$T_A = 25$ °C	- 42 <sup>a, b</sup>	
		$T_A = 70$ °C	- 33.7 <sup>a, b</sup>	
Pulsed Drain Current	$I_{DM}$	- 100		
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	- 60 <sup>d</sup>	
		$T_A = 25$ °C	- 5.6 <sup>a, b</sup>	
Avalanche Current	$I_{AS}$	L = 0.1 mH	- 50	
Single-Pulse Avalanche Energy			$E_{AS}$	
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	104	W
		$T_C = 70$ °C	66.6	
		$T_A = 25$ °C	6.25 <sup>a, b</sup>	
		$T_A = 70$ °C	4.0 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>		260		

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c</sup>	$R_{thJA}$	15	20	°C/W
Maximum Junction-to-Case	$R_{thJC}$	0.9	1.2	

#### Notes:

- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- Maximum under Steady State conditions is 54 °C/W.
- Package limited.
- See Solder Profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-14.5		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.1			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.5		-1.4	V	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-5		
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	-40			A	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -25\text{ A}$		0.0016	0.00195	$\Omega$	
		$V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		0.002	0.0025		
		$V_{GS} = -2.5\text{ V}, I_D = -15\text{ A}$		0.0031	0.0039		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -25\text{ A}$		95		S	
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		20 000		pF	
Output Capacitance	$C_{oss}$			2150			
Reverse Transfer Capacitance	$C_{rss}$			2650			
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -20\text{ A}$		390	585	nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		188	282		
Gate-Drain Charge	$Q_{gd}$			33.6			
Gate Resistance	$R_g$			46			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		0.9	1.8	3.6	ns
Rise Time	$t_r$			20	40		
Turn-Off Delay Time	$t_{d(off)}$			14	28		
Fall Time	$t_f$			230	400		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		100	170		
Rise Time	$t_r$			150	255		
Turn-Off Delay Time	$t_{d(off)}$			230	390		
Fall Time	$t_f$			110	190		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-60	A	
Pulse Diode Forward Current	$I_{SM}$				-100		
Body Diode Voltage	$V_{SD}$	$I_S = -5\text{ A}, V_{GS} = 0\text{ V}$		-0.64	-1.1	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		88	140	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			105	160	nC	
Reverse Recovery Fall Time	$t_a$			25		ns	
Reverse Recovery Rise Time	$t_b$			63			

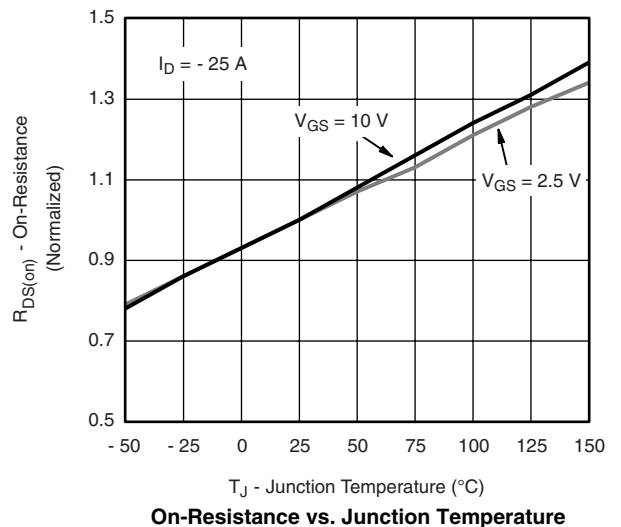
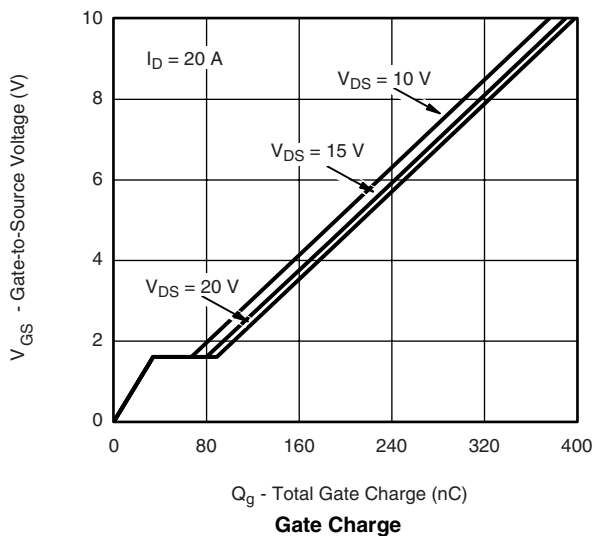
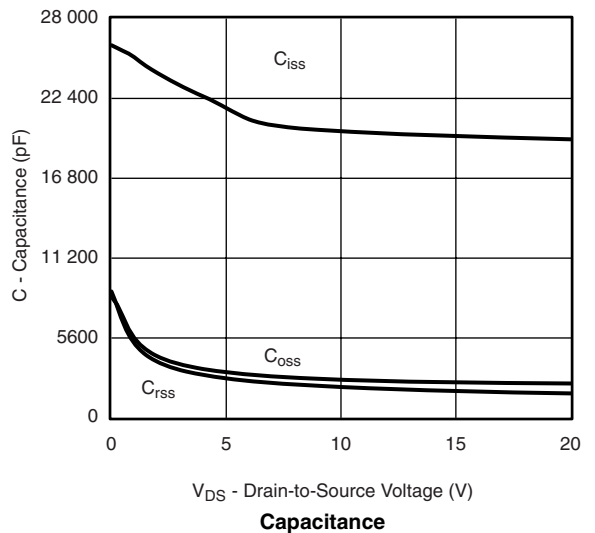
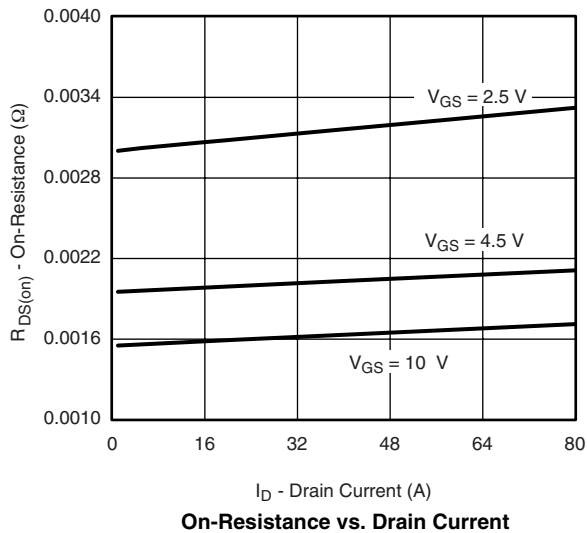
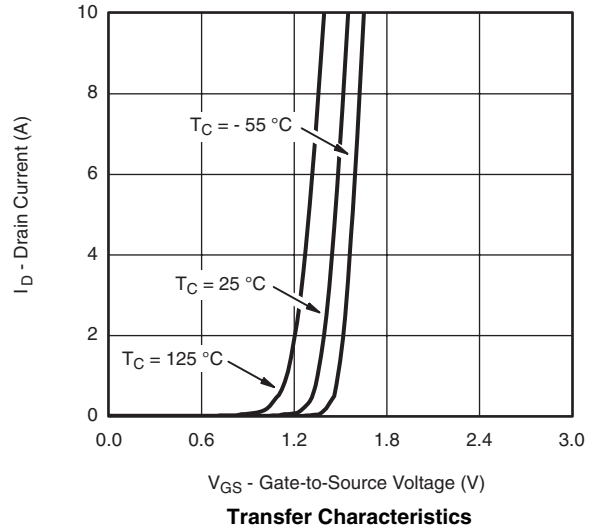
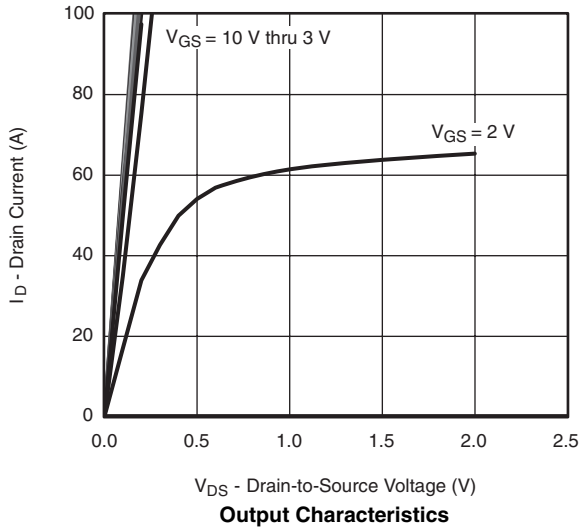
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

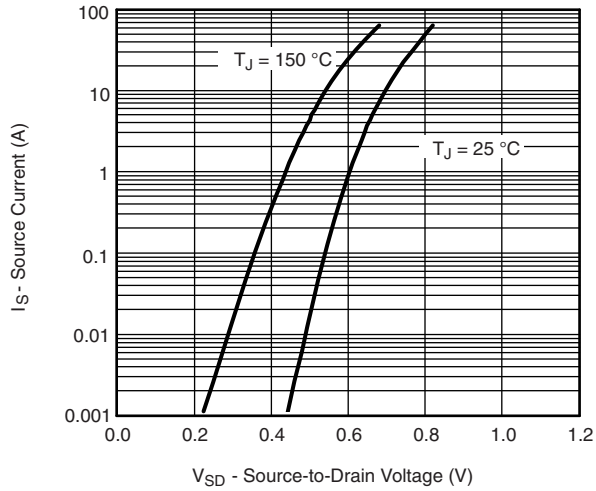


# Si7137DP

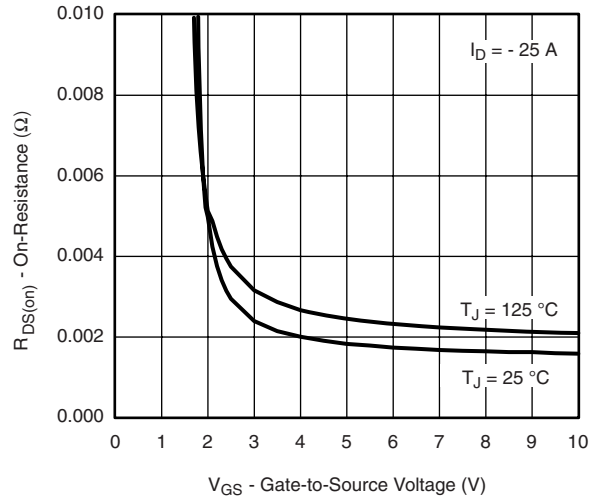
Vishay Siliconix



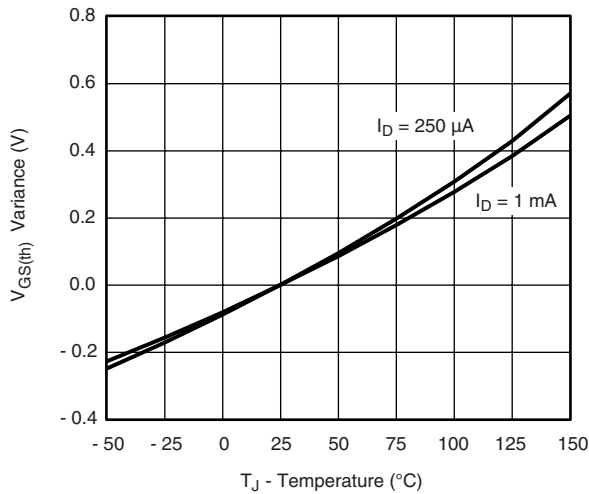
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



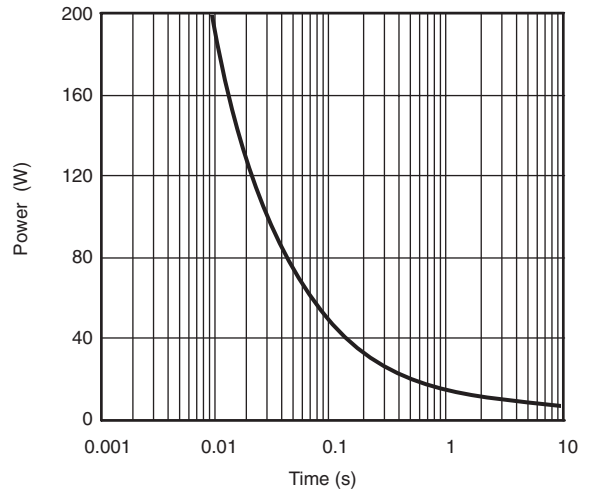
Source-Drain Diode Forward Voltage



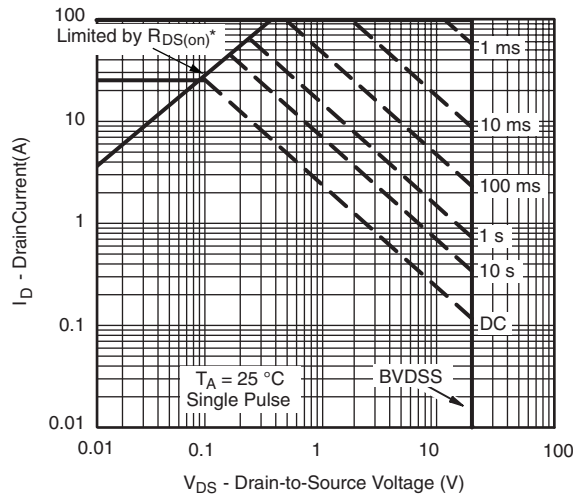
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

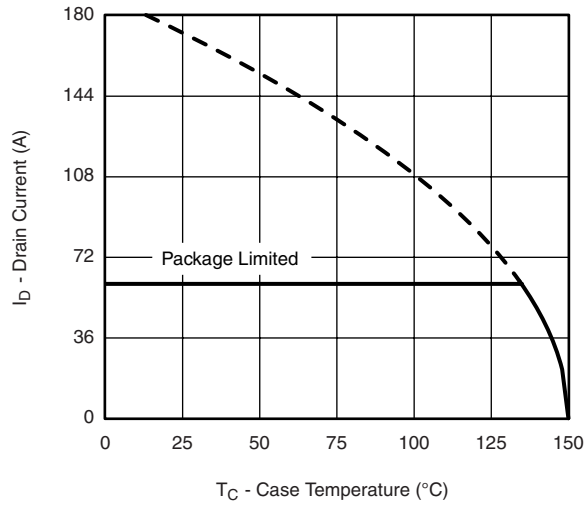


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

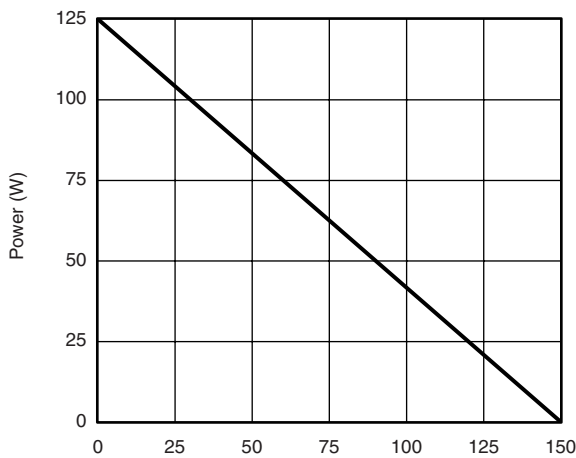
Safe Operating Area



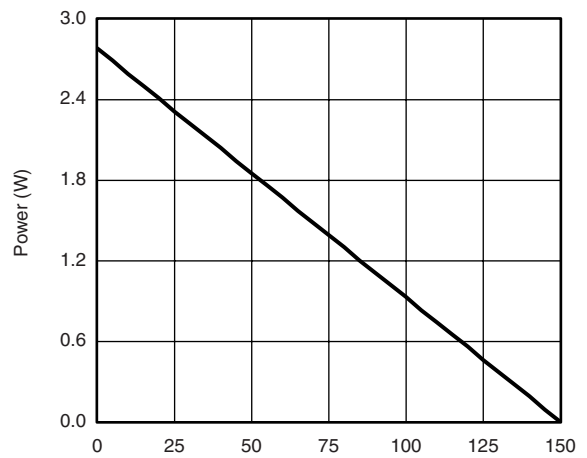
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\***



**Power, Junction-to-Case**



**Power Derating, Junction-to-Ambient**

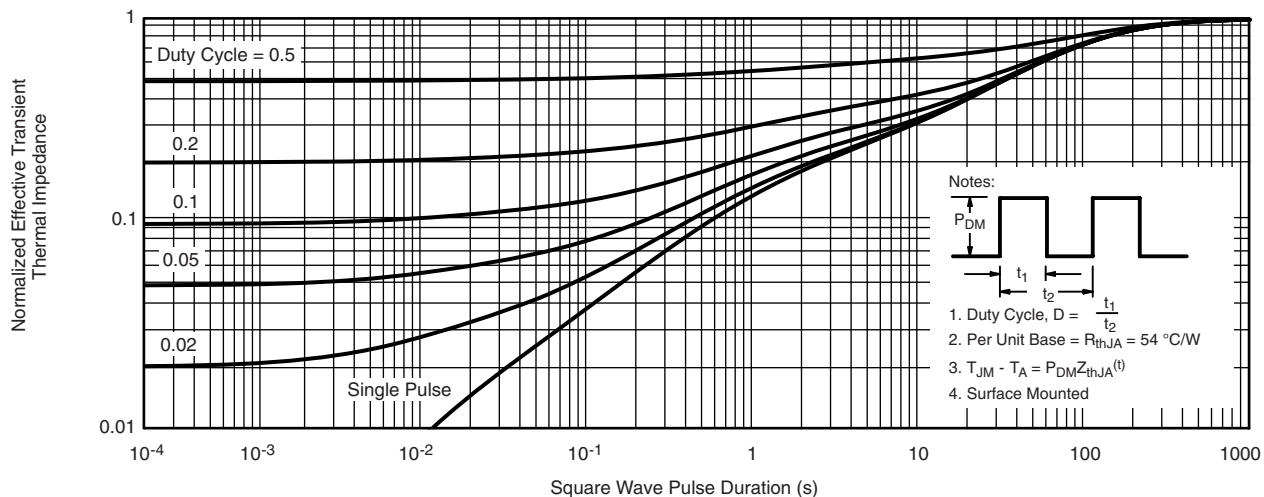
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# Si7137DP

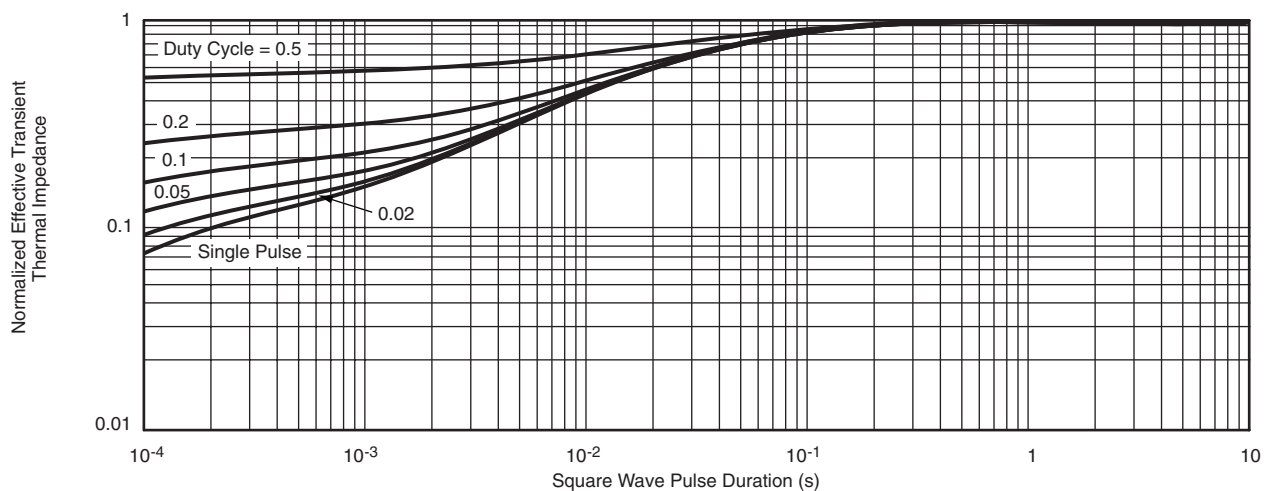
Vishay Siliconix



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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