



N-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
150	0.135 @ V _{GS} = 10 V	3.4	20 nC
	0.142 @ V _{GS} = 6 V	3.3	

FEATURES

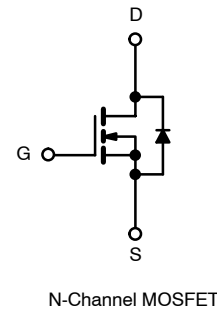
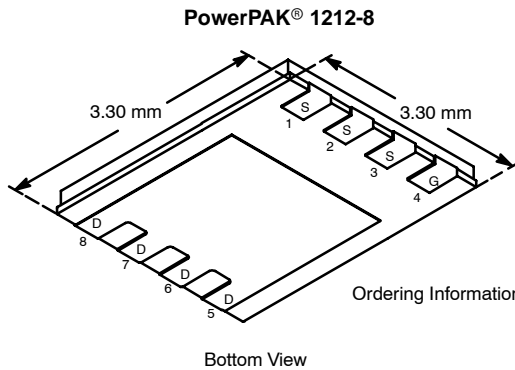
- PWM-Optimized TrenchFET® Power MOSFET
- 100% R_g Tested
- Avalanche Tested



RoHS
COMPLIANT

APPLICATIONS

- Primary Side Switching Circuits



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	150		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	3.4	2.2	A
		T _A = 70 °C	2.7	1.7	
Pulsed Drain Current	I _{DM}	10			
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3		
Single Avalanche Current	I _{AS}	9		mJ	
Single Avalanche Energy		E _{AS}	4		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8	1.5	W
		T _A = 70 °C	2.0	0.8	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	26	33	°C/W
		Steady State	65	81	
Maximum Junction-to-Case (Drain)	R _{thJC}	1.9	2.4		

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

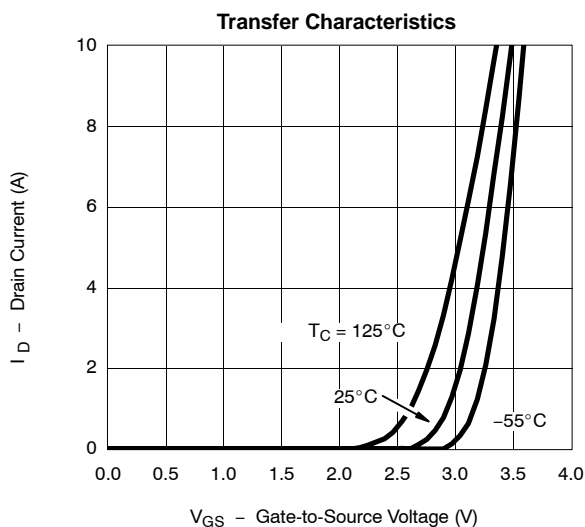
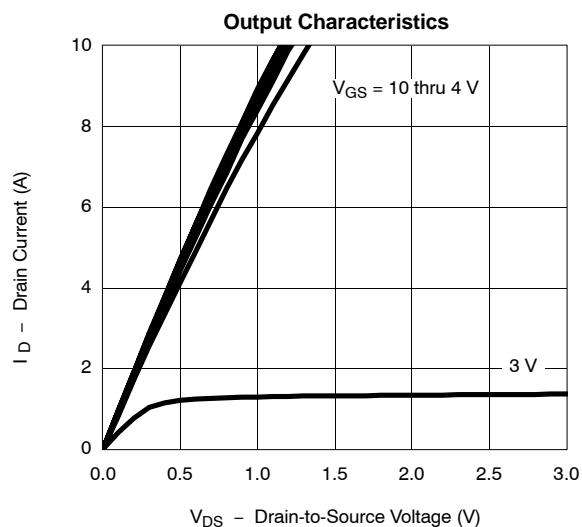
MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$		0.112	0.135	Ω
		$V_{GS} = 6 \text{ V}, I_D = 3.3 \text{ A}$		0.117	0.142	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 3.4 \text{ A}$		17		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2 \text{ A}, V_{GS} = 0 \text{ V}$		0.78	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$		20	30	nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			4.7		
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.8	1.7	2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}, R_L = 100 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		10	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		50	75	nC
Reverse Recovery Charge	Q_{rr}			100	150	

Notes

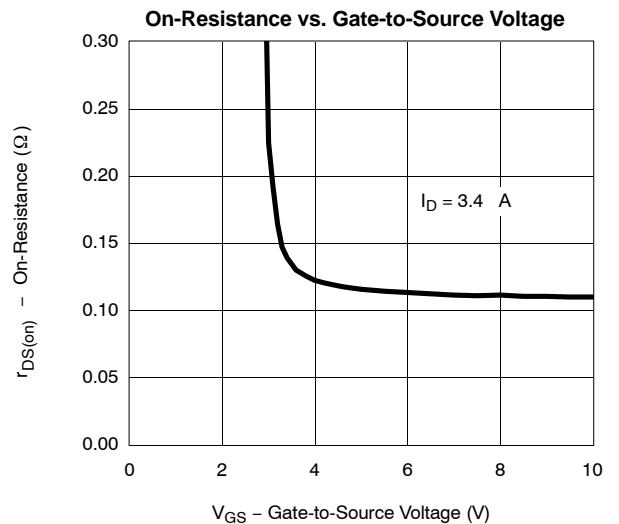
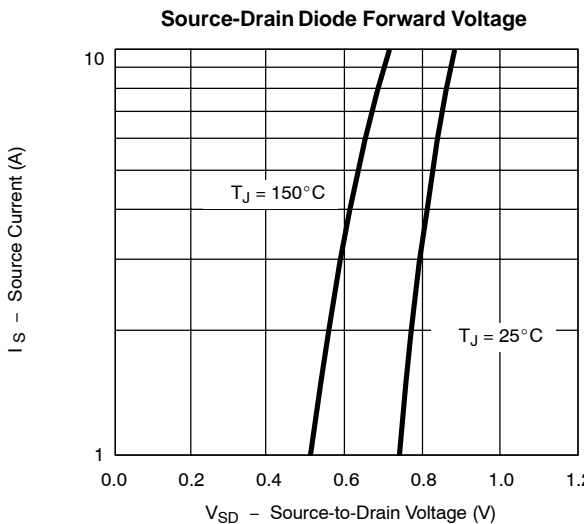
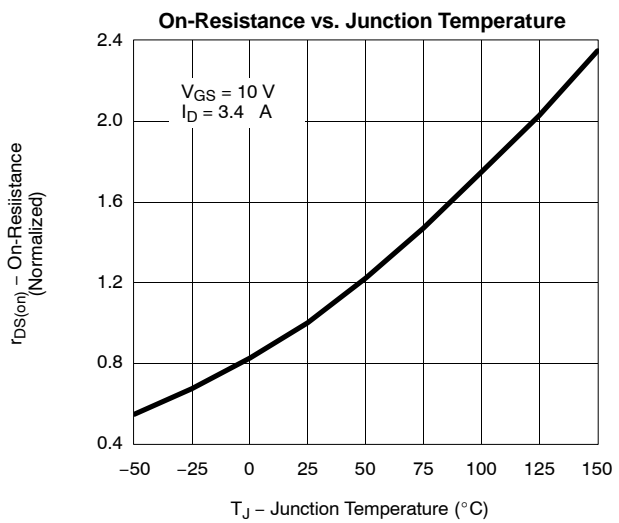
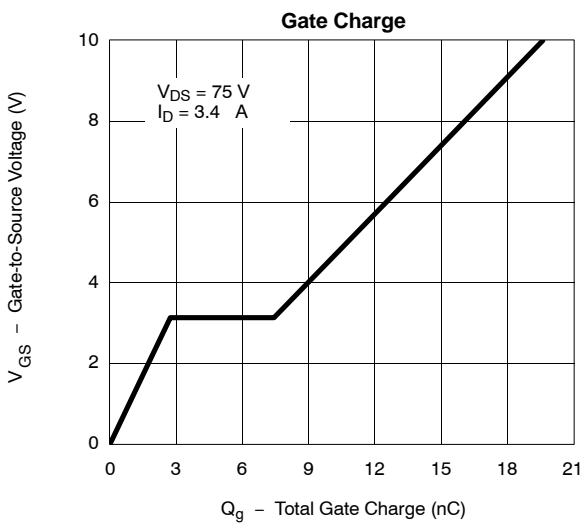
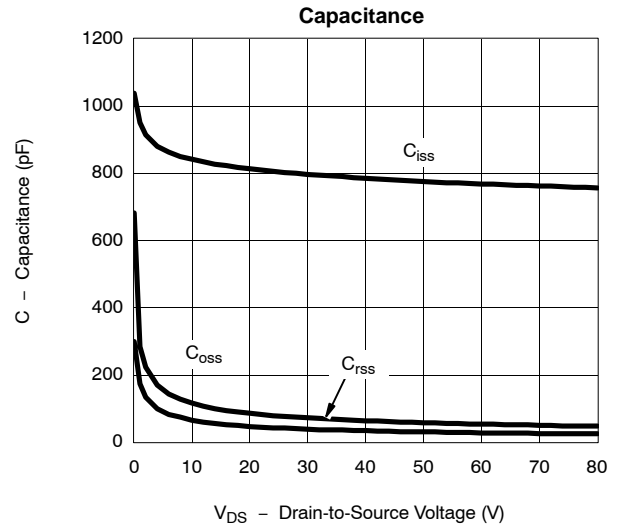
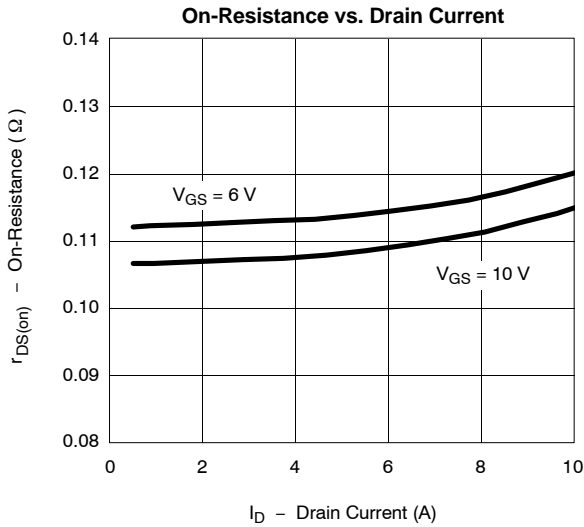
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

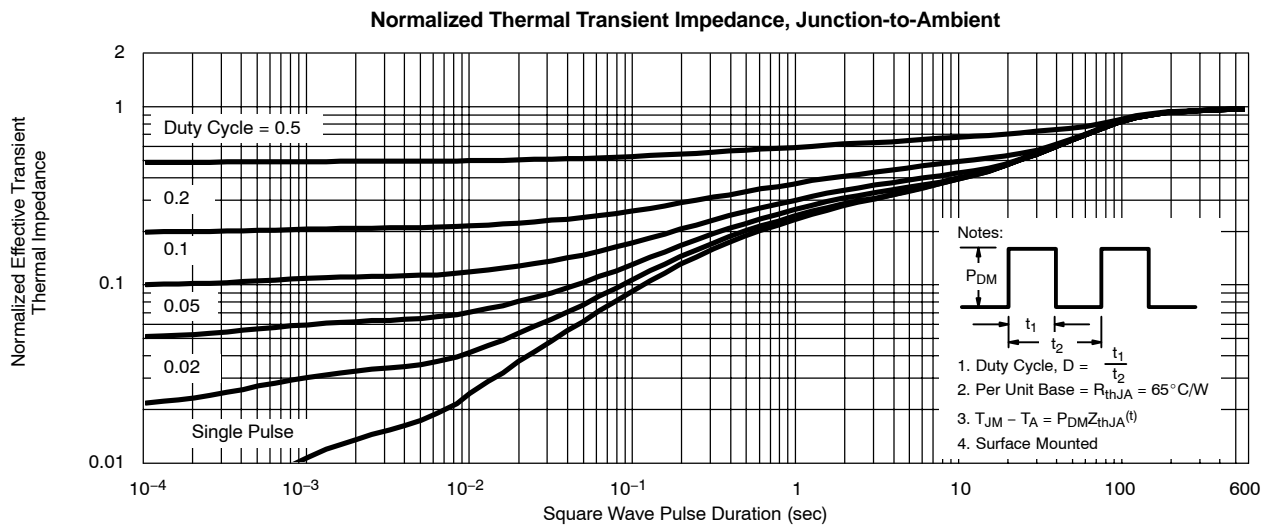
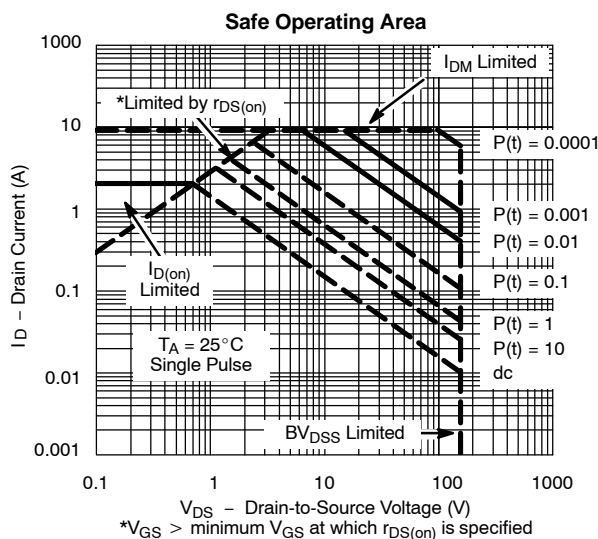
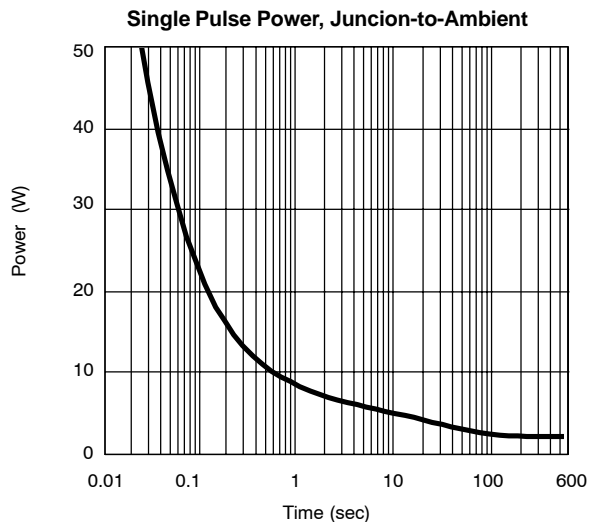
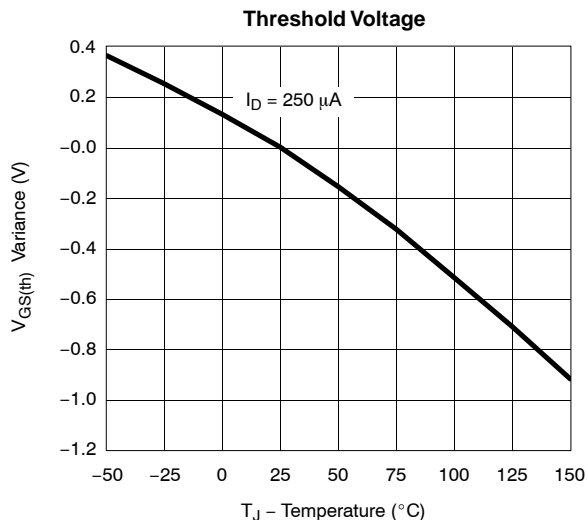
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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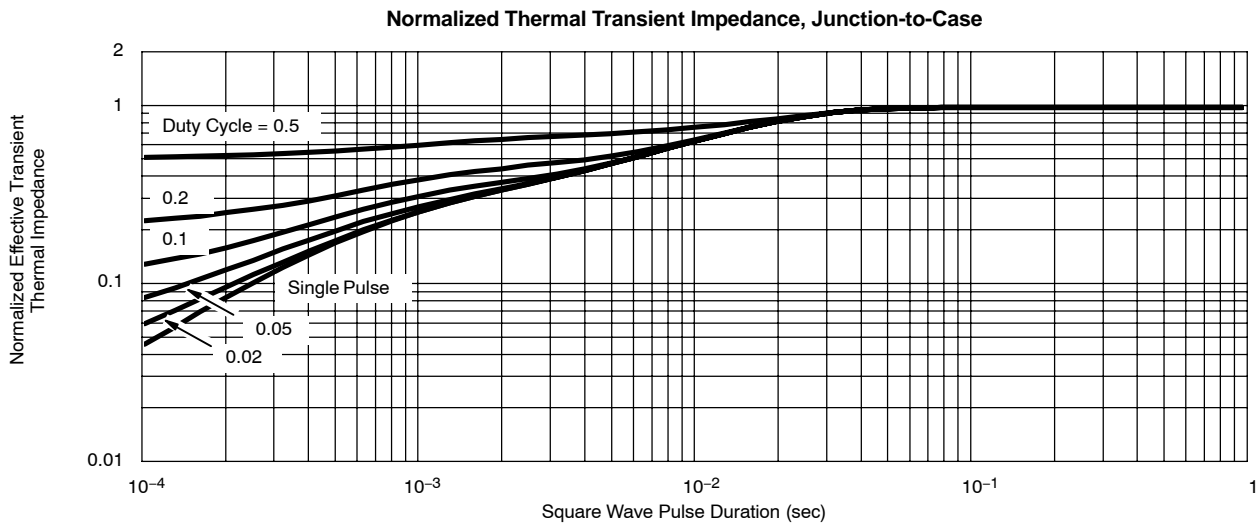


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