

Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
100	0.195 at $V_{GS} = 10$ V	2.5
	0.230 at $V_{GS} = 6$ V	2.3

FEATURES

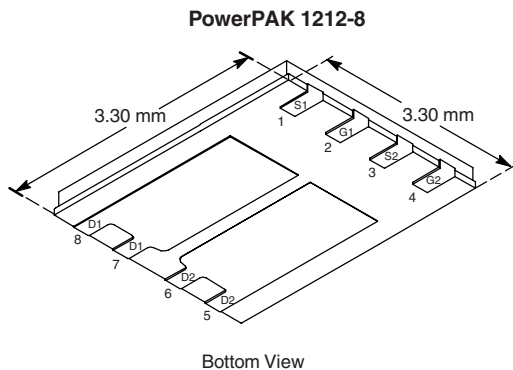
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package, 1/3 the Space of An SO-8 While Thermally Comparable
- PWM Optimized



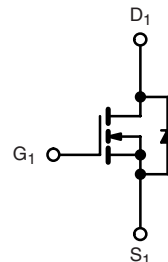
RoHS
COMPLIANT

APPLICATIONS

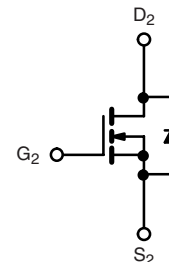
- DC/DC Primary-Side Switch
- 48 V Battery Monitoring



Ordering Information: Si7922DN-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	100		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	2.5	1.8	A
		$T_A = 85$ °C	1.8	1.3	
Pulsed Drain Current	I_{DM}	10			
Avalanche Current	I_{AS}	5		mJ	
Single Avalanche Energy		E_{AS}	1.25		
Continuous Source Current (Diode Conduction) ^a	I_S	2.2	1.1	A	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	2.6	1.3	W
		$T_A = 85$ °C	1.4	0.69	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	
Soldering Recommendations ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ s	R_{thJA}	38	48	°C/W
	Steady State		77	94	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.3	5.4	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

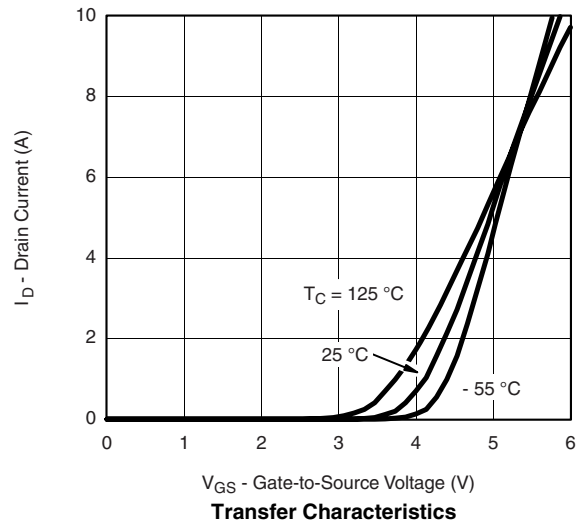
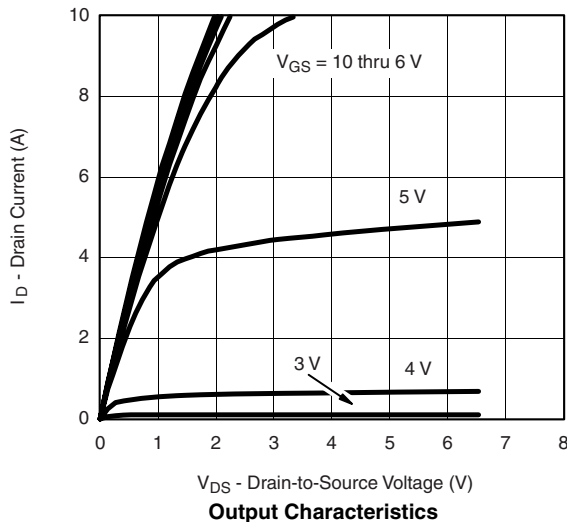
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		3.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	10			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.162	0.195	Ω
		$V_{GS} = 6\text{ V}, I_D = 2.3\text{ A}$		0.190	0.230	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 2.5\text{ A}$		5.3		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.2\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		5.2	8	nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.9		
Gate Resistance	R_g			1.7		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 50\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_G = 6\text{ }\Omega$		7	15	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			8	15	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		40	80	

Notes:

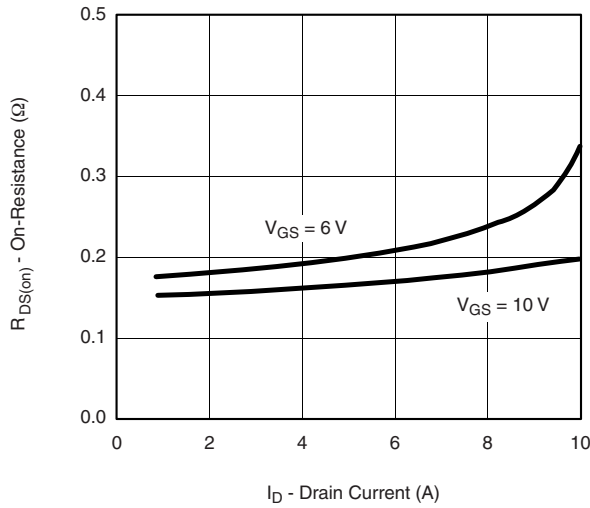
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

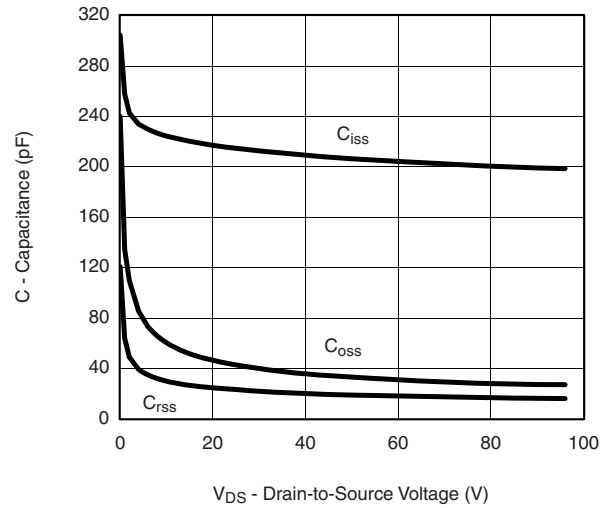
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



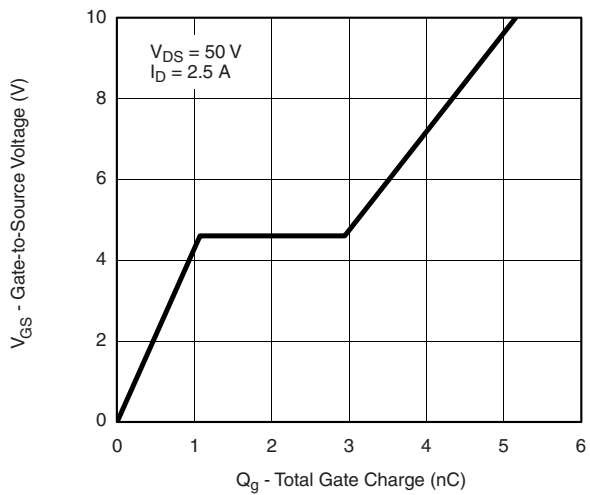
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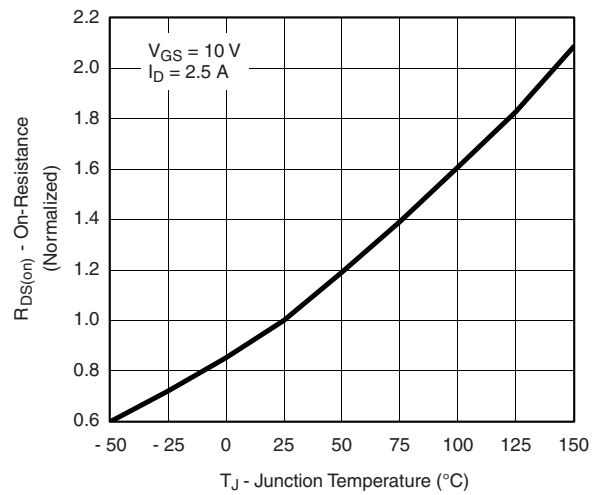
On-Resistance vs. Drain Current



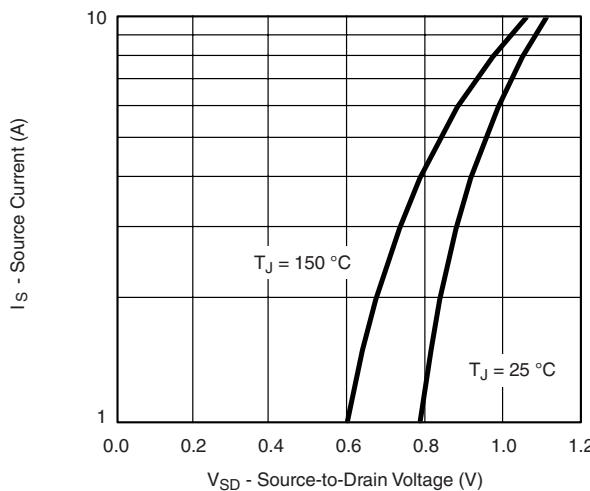
Capacitance



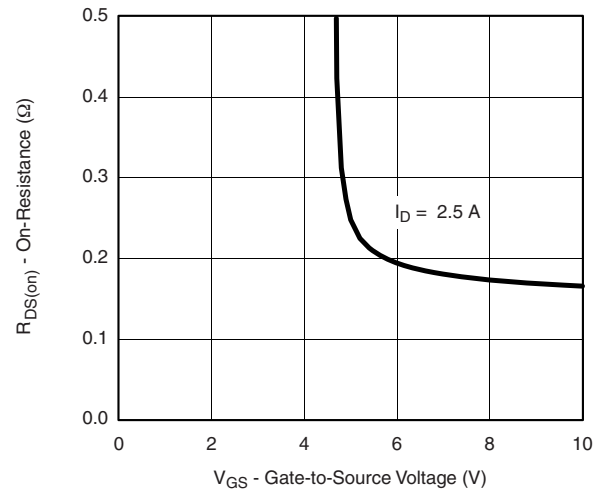
Gate Charge



On-Resistance vs. Junction Temperature

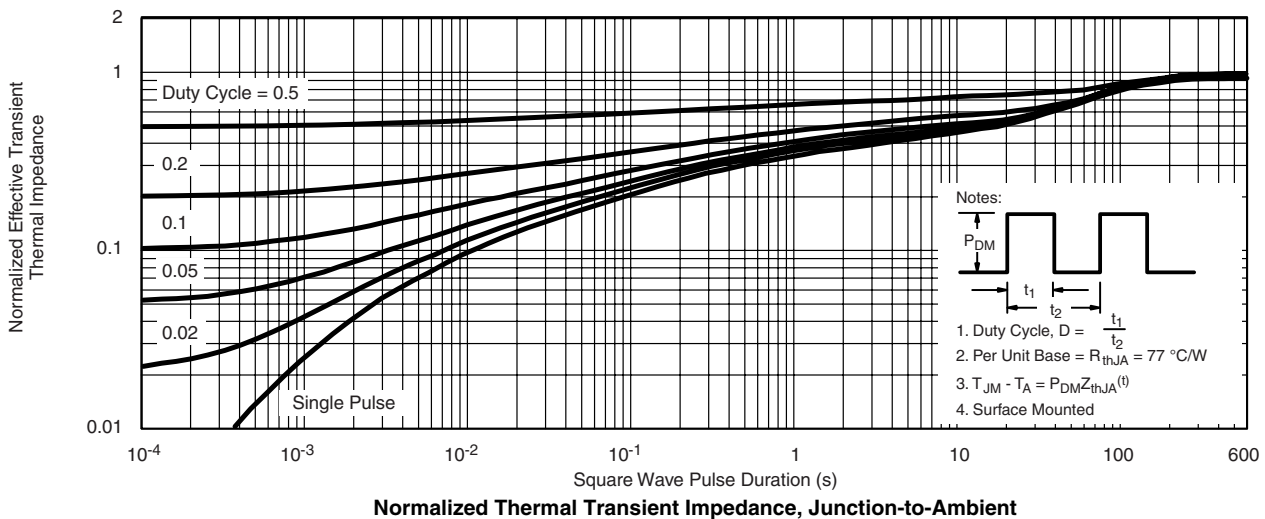
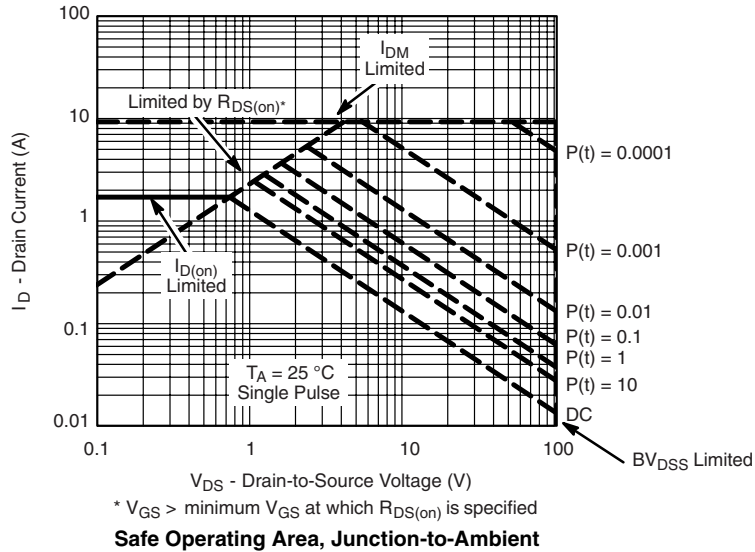
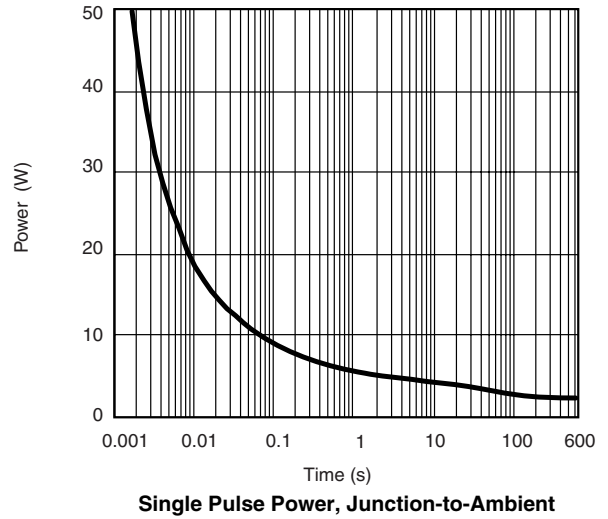
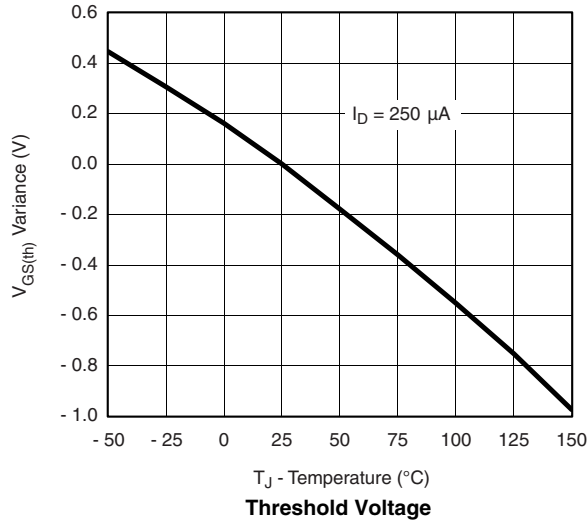


Source-Drain Diode Forward Voltage

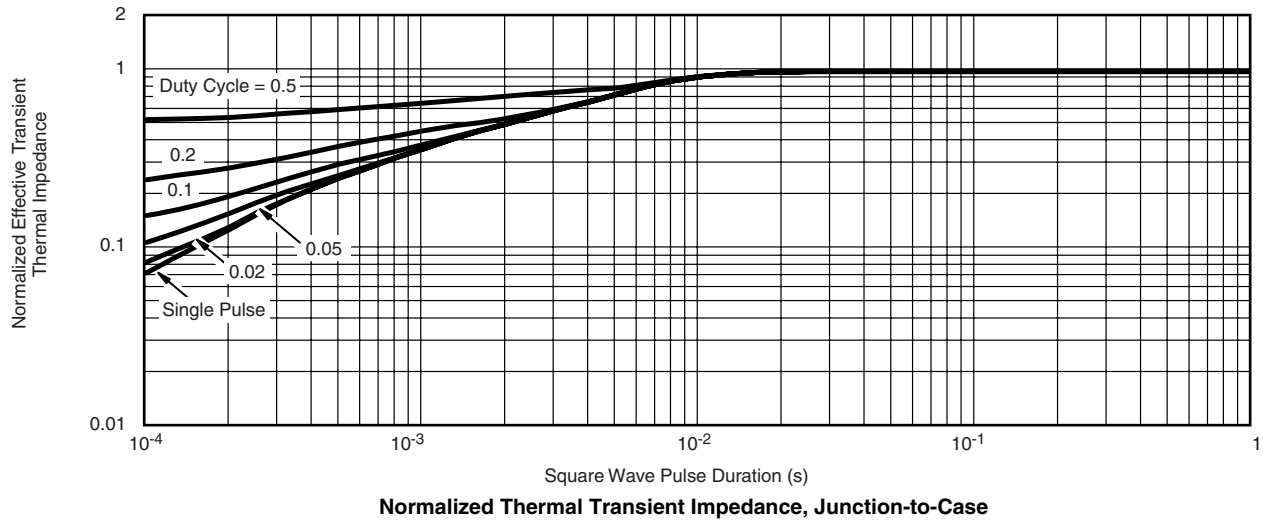


On-Resistance vs. Gate-to-Source Voltage

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