

## Bi-Directional N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>S1S2</sub> (V)	r <sub>S1S2(on)</sub> (Ω)	I <sub>S1S2</sub> (A)
30	0.045 @ V <sub>GS</sub> = 4.5 V	4.9
	0.060 @ V <sub>GS</sub> = 2.5 V	4.2

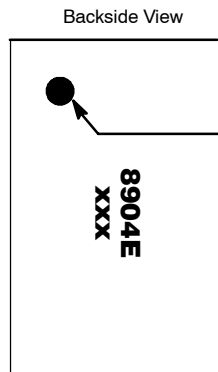
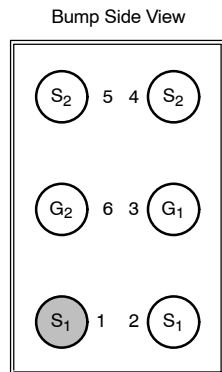
### FEATURES

- TrenchFET® Power MOSFET
- Ultra-Low r<sub>SS(on)</sub> and 22.5-mΩ Maximum Effective On-Resistance
- ESD Protected: 4000 V
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area, Profile (0.65 mm) and On-Resistance Per Footprint Area

### APPLICATIONS

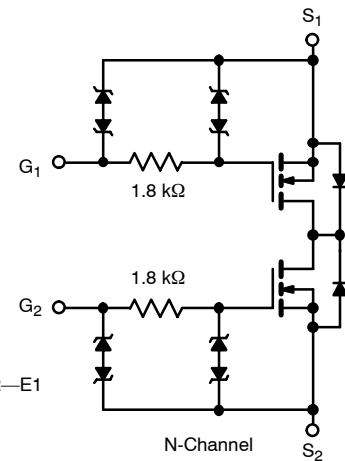
- Battery Protection Circuit
  - 1-2 Cell Li+/LiP Battery Pack for Portable Devices

### MICRO FOOT



Device Marking:  
8904E = P/N Code  
xxx = Date/Lot Traceability Code

Ordering Information: Si8904EDB-T2—E1



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Source1—Source2 Voltage		V <sub>S1S2</sub>	30		V
Gate-Source Voltage		V <sub>GS</sub>	±12		
Continuous Source1—Source2 Current (T <sub>J</sub> = 150°C) <sup>a</sup>	T <sub>A</sub> = 25°C	I <sub>S1S2</sub>	4.9	3.8	A
	T <sub>A</sub> = 85°C		3.5	2.7	
Pulsed Source1—Source2 Current		I <sub>SM</sub>	25		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.7	1	W
	T <sub>A</sub> = 85°C		0.8	0.5	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C
Package Reflow Conditions <sup>c</sup>	VPR		215		
	IR/Convection		220		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 5 sec	R <sub>thJA</sub>	60	75	°C/W
	Steady State		95	120	
Maximum Junction-to-Foot <sup>b</sup>	Steady State	R <sub>thJF</sub>	18	22	

#### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- The Foot is defined as the top surface of the package.
- Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.

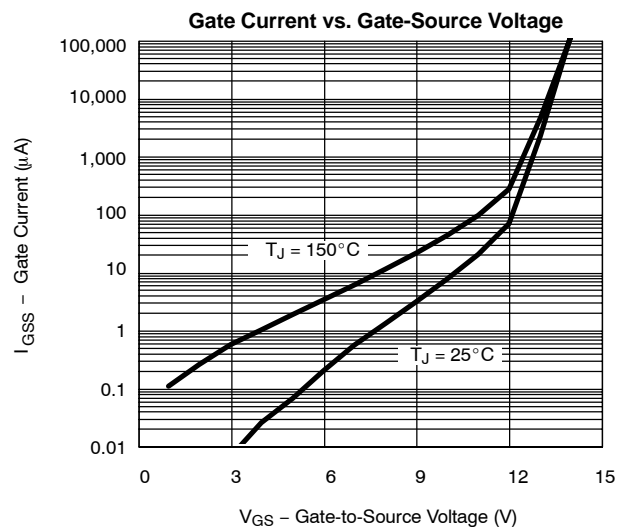
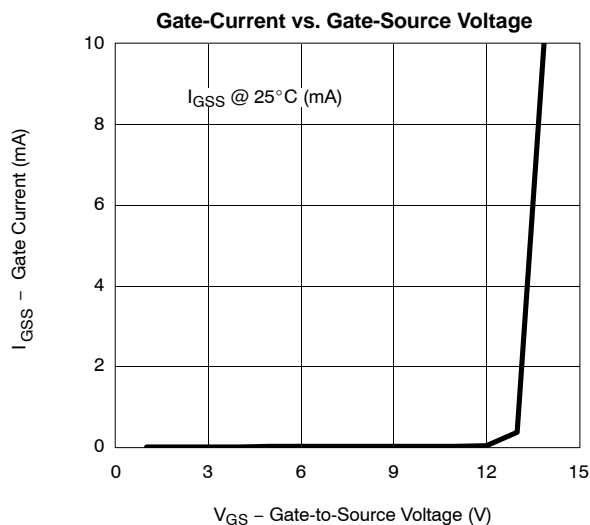
**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>SS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6		1.6	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>SS</sub> = 0 V, V <sub>GS</sub> = ±4.5 V			±4	μA
		V <sub>SS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±10	mA
Zero Gate Voltage Source Current	I <sub>S1S2</sub>	V <sub>SS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>SS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			5	
On-State Source Current <sup>a</sup>	I <sub>S(on)</sub>	V <sub>SS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	5			A
Source1—Source2 On-State Resistance <sup>a</sup>	r <sub>S1S2(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>SS</sub> = 1 A		0.037	0.045	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>SS</sub> = 1 A		0.048	0.060	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>SS</sub> = 10 V, I <sub>SS</sub> = 1 A		12		S
<b>Dynamic<sup>b</sup></b>						
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>SS</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>SS</sub> = 1 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 6 Ω		1.6	2.4	μS
Rise Time	t <sub>r</sub>			2	3	
Turn-Off Delay Time	t <sub>d(off)</sub>			1.5	2.3	
Fall Time	t <sub>f</sub>			3.7	5.6	

## Notes

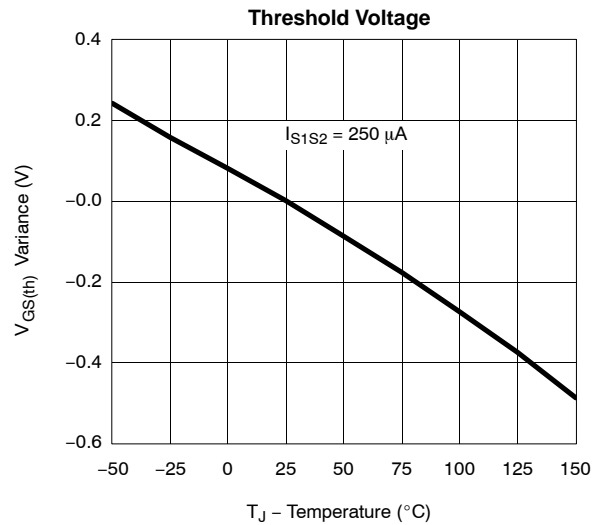
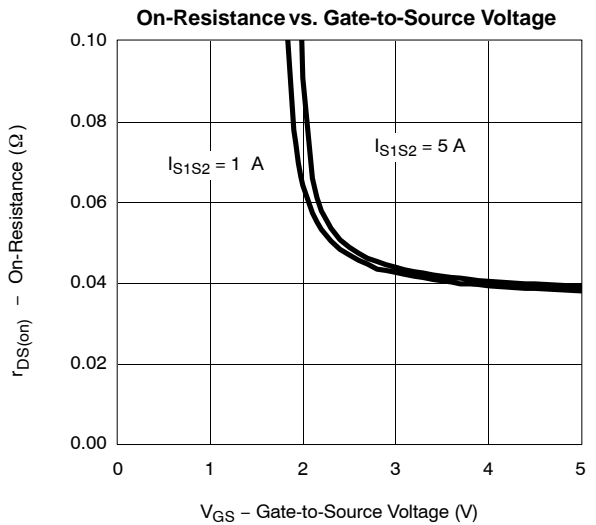
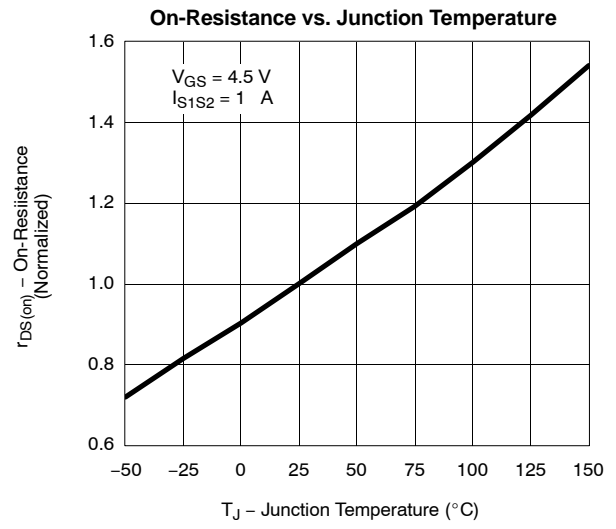
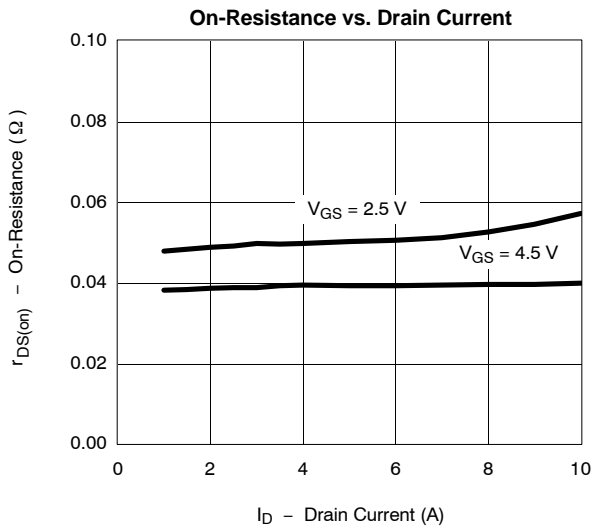
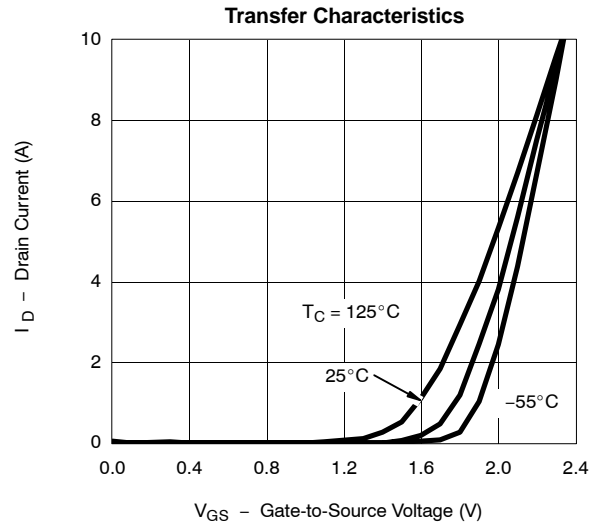
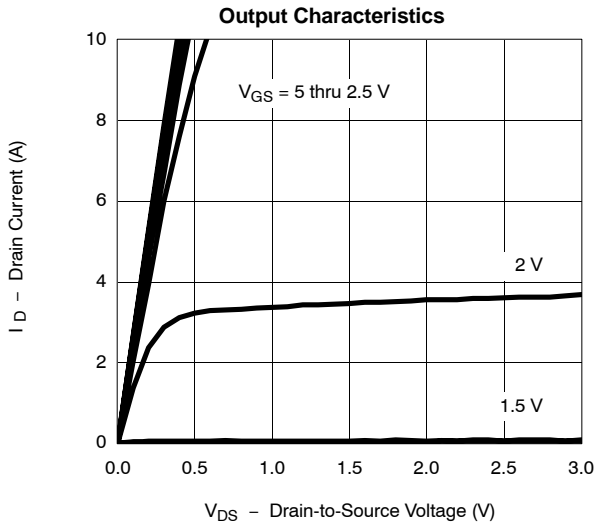
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

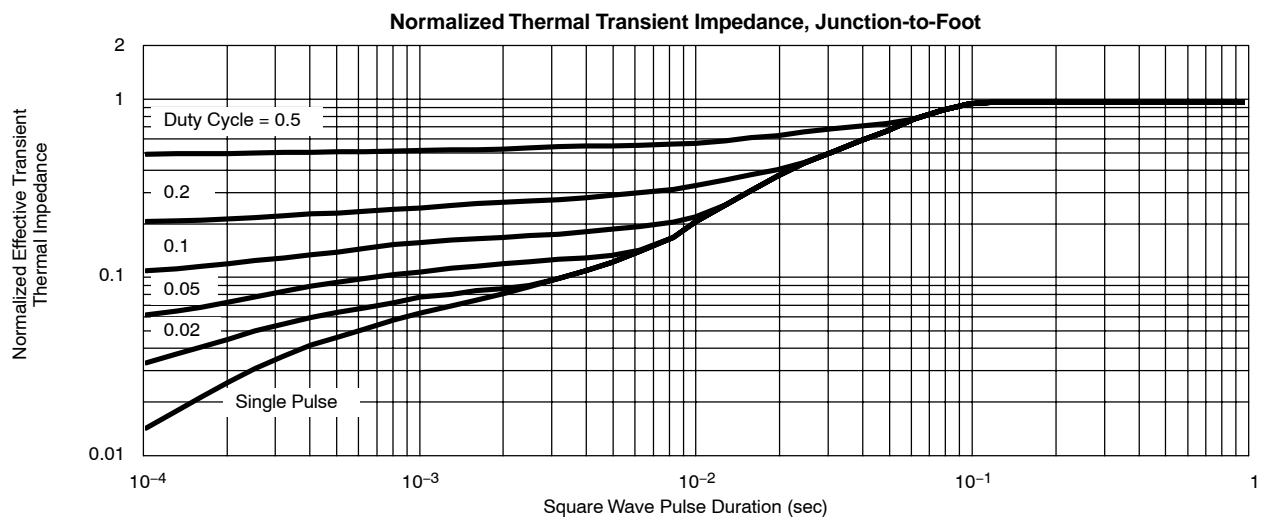
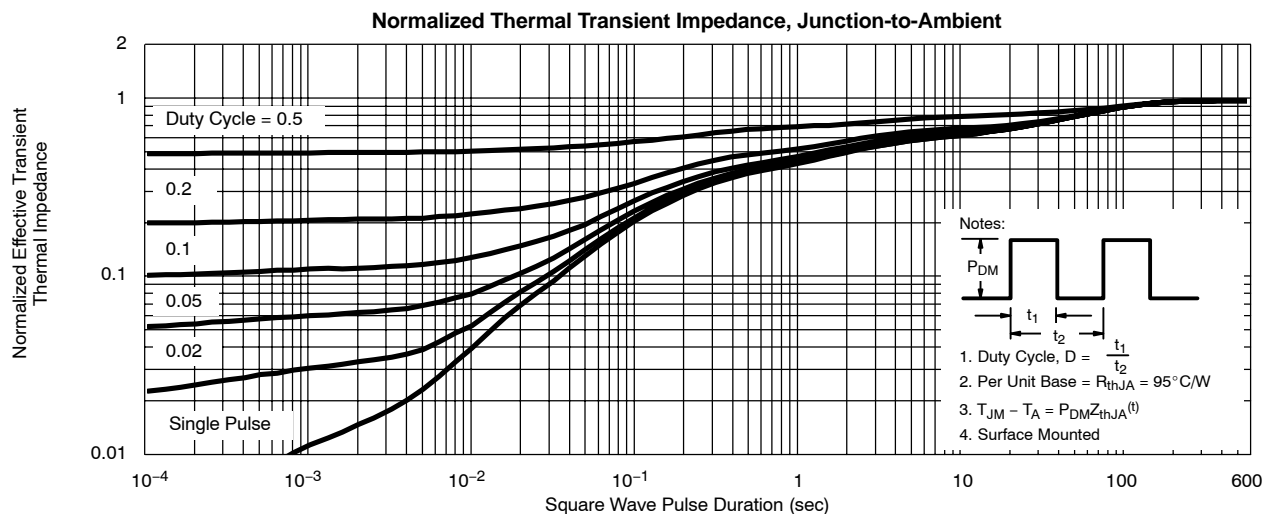
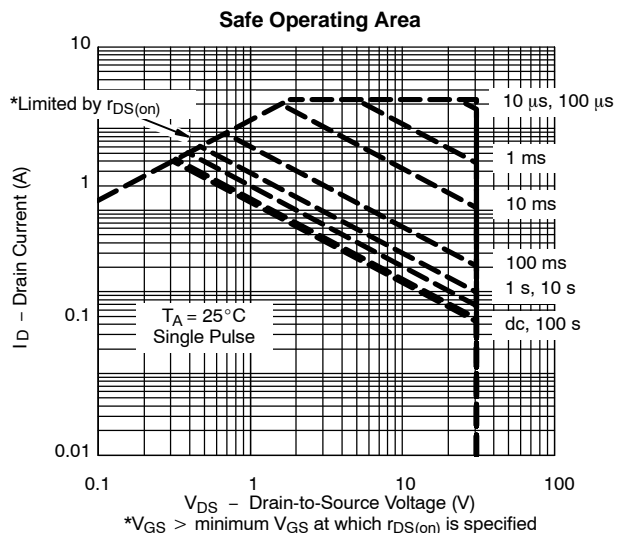
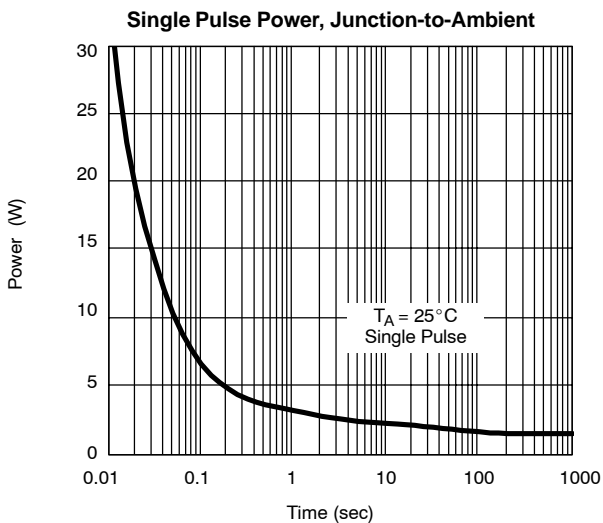
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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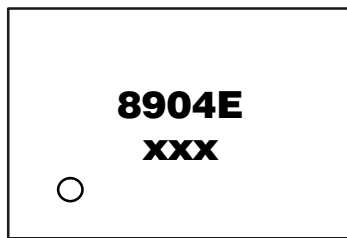
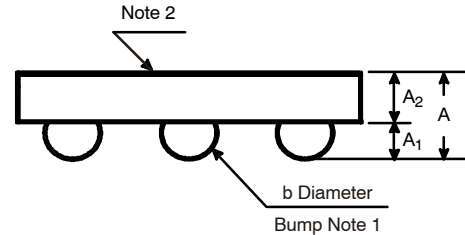
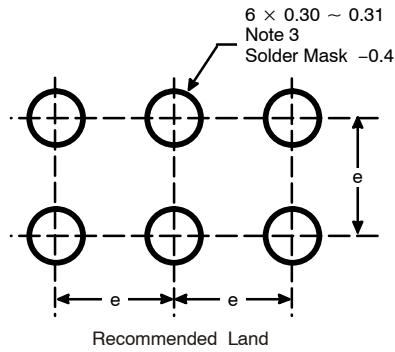


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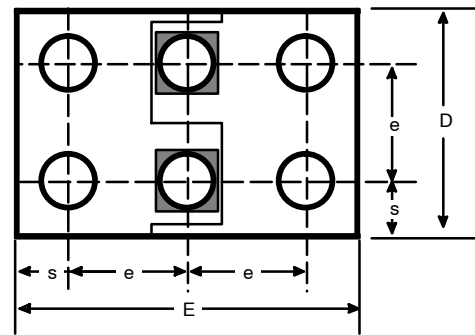


**PACKAGE OUTLINE**

**MICRO FOOT: 6-BUMP (2 X 3, 0.8-mm PITCH)**



Mark on Backside of Die



NOTES (Unless Otherwise Specified):

1. 6 solder bumps are Eutetic 63Sn/37Pb with diameter 0.37 – 0.41 mm
2. Backside surface is coated with a Ag/Ni/Ti layer
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A <sub>1</sub>	0.260	0.290	0.102	0.114
A <sub>2</sub>	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
s	0.380	0.400	0.0150	0.0157

\* Use millimeters as the primary measurement.

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