



N-Channel 20-V (D-S) MOSFETs

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel-1	20	0.0086 at V _{GS} = 10 V	16 ^a	9.5 nC
		0.0108 at V _{GS} = 4.5 V	16 ^a	
Channel-2	20	0.0058 at V _{GS} = 10 V	16 ^a	27 nC
		0.0066 at V _{GS} = 4.5 V	16 ^a	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

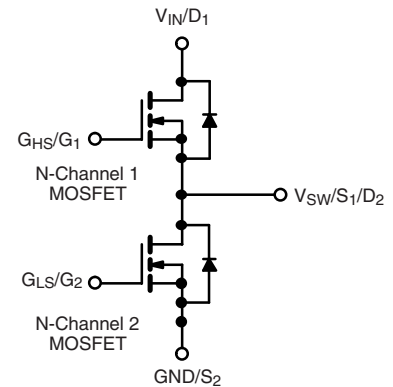
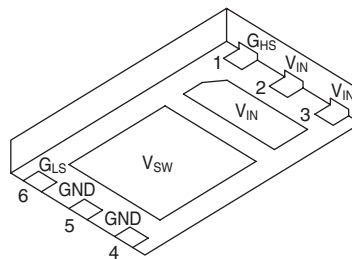
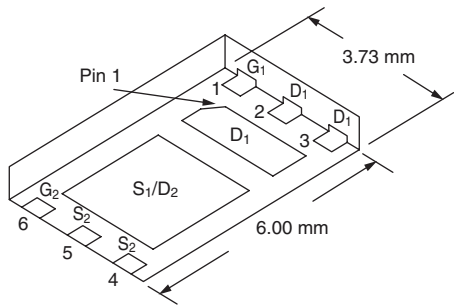


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook System Power

PowerPAIR™ 6 x 3.7



Ordering Information: SiZ700DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V _{DS}	20	20	V
Gate-Source Voltage	V _{GS}	± 16		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	16 ^a	16 ^a
		T _C = 70 °C	16 ^a	16 ^a
		T _A = 25 °C	13.1 ^{b, c}	17.3 ^{b, c}
		T _A = 70 °C	10.5 ^{b, c}	13.9 ^{b, c}
Pulsed Drain Current	I _{DM}	60	60	A
Source Drain Current Diode Current	I _S	T _C = 25 °C	14.7	
		T _A = 25 °C	1.96 ^{b, c}	2.3 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	2.36	2.8
		T _C = 70 °C	1.5	1.78
		T _A = 25 °C	1.4 ^{b, c}	1.47 ^{b, c}
		T _A = 70 °C	0.9 ^{b, c}	0.94 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	39	53	33	45	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	5.7	7.1	3.7	4.6		

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 90 °C/W for Channel-1 and 85 °C/W for Channel-2.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	20			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	20				
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		21		mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		21			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		- 5.8		mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		- 5.8			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	0.8		2.2	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	0.8		2.2		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	Ch-1			± 100	nA	
			Ch-2			± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	μA	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			1		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			10		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2			10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	30			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	30				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		0.007	0.0086	Ω	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0047	0.0058		
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1		0.0088	0.0108		
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	Ch-2		0.0054	0.0066		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		60		S	
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		100			
Dynamic^a								
Input Capacitance	C_{iss}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		1300		pF	
			Ch-2		3860			
Output Capacitance	C_{oss}		Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		290		
				Ch-2		760		
Reverse Transfer Capacitance	C_{rss}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		Ch-1		132		
				Ch-2		350		
Total Gate Charge	Q_g		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		20	35	nC
				Ch-2		55	85	
		Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	Ch-1		9.5	15		
			Ch-2		27	45		
Gate-Source Charge	Q_{gs}	Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		3.2			
Gate-Drain Charge	Q_{gd}		Ch-2		9.2			
			Ch-1		2.4			
			Ch-2		7.1			
Gate Resistance	R_g	$f = 1\text{ MHz}$	Ch-1	0.3	1.3	2.6	Ω	
			Ch-2	0.2	1.0	2.0		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 10\ \Omega$ $I_D \cong 1.0\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		9	15	ns
			Ch-2		13	20	
Rise Time	t_r		Ch-1		8	15	
			Ch-2		8	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 10\text{ V}, R_L = 10\ \Omega$ $I_D \cong 1.0\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		25	40	
			Ch-2		52	80	
Fall Time	t_f		Ch-1		8	15	
			Ch-2		15	25	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 10\ \Omega$ $I_D \cong 1.0\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		8	15	
			Ch-2		12	20	
Rise Time	t_r		Ch-1		9	15	
			Ch-2		8	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 10\text{ V}, R_L = 10\ \Omega$ $I_D \cong 1.0\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		25	40	
			Ch-2		47	75	
Fall Time	t_f		Ch-1		8	15	
			Ch-2		10	15	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			14.7	A
			Ch-2			16	
Pulse Diode Forward Current ^a	I_{SM}		Ch-1			60	A
			Ch-2			60	
Body Diode Voltage	V_{SD}	$I_S = 2.0\text{ A}, V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V
		$I_S = 2.3\text{ A}, V_{GS} = 0\text{ V}$	Ch-2		0.8	1.2	
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 $I_F = 2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		25	50	ns
			Ch-2		40	80	
Body Diode Reverse Recovery Charge	Q_{rr}		Ch-1		13	25	nC
			Ch-2		31	60	
Reverse Recovery Fall Time	t_a	Channel-2 $I_F = 2.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		12		ns
			Ch-2		21		
Reverse Recovery Rise Time	t_b		Ch-1		13		
			Ch-2		19		

Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

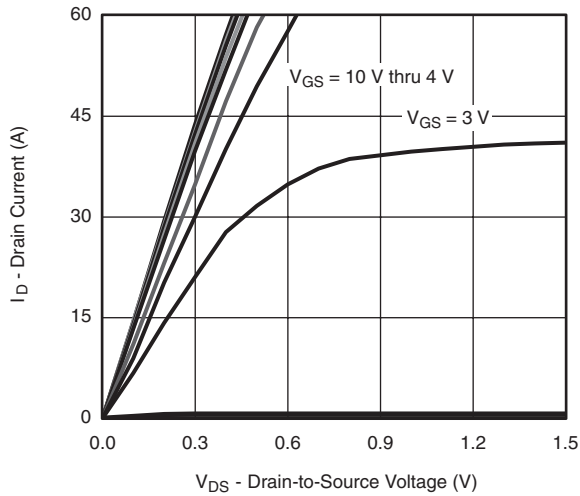
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SiZ700DT

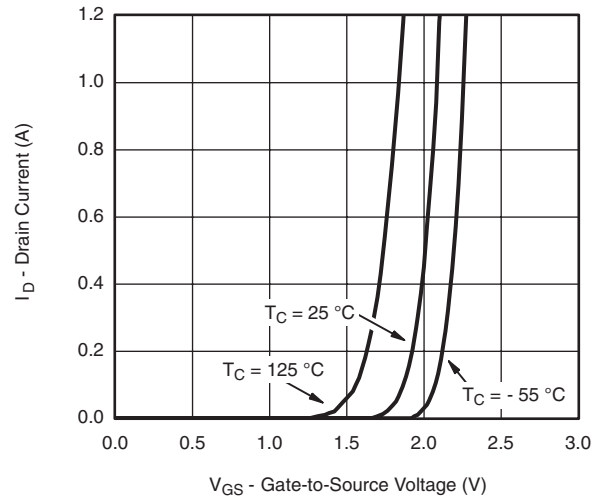
Vishay Siliconix



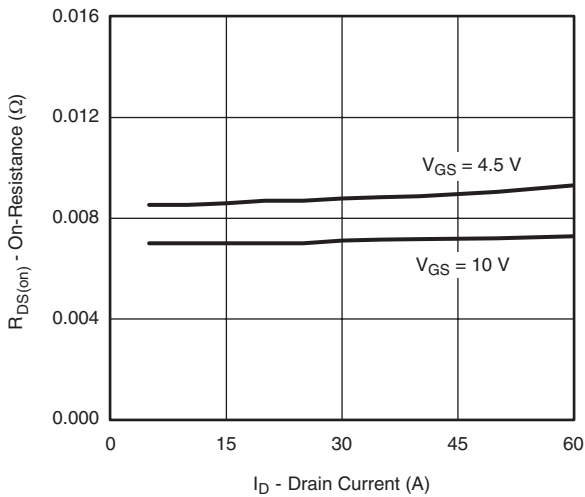
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



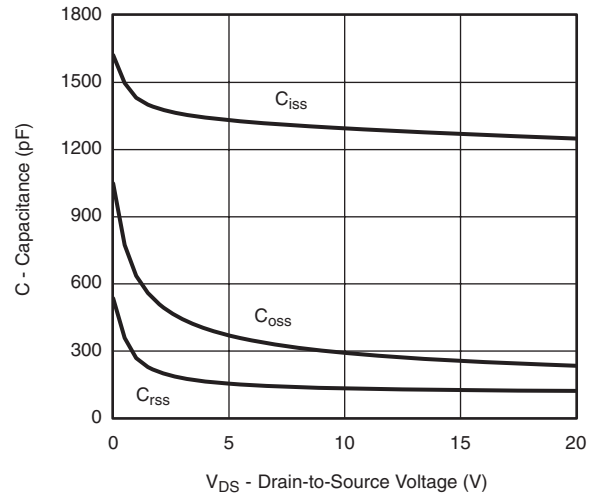
Output Characteristics



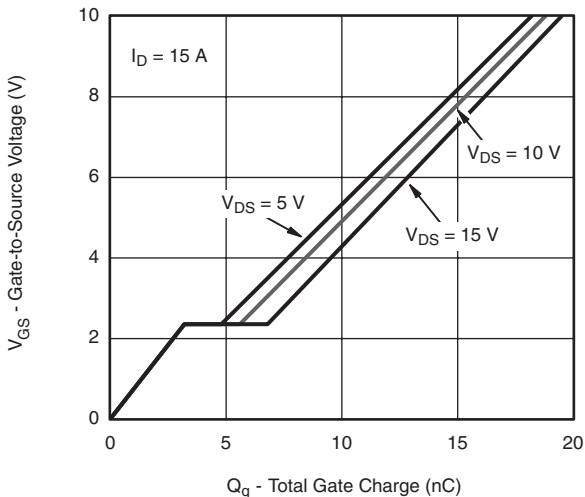
Transfer Characteristics



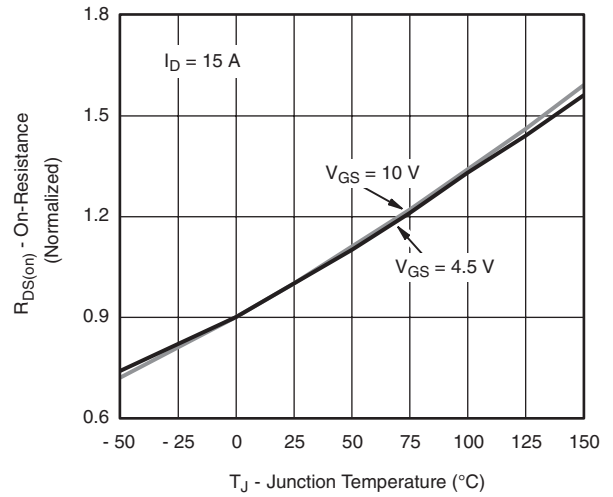
On-Resistance vs. Drain Current



Capacitance



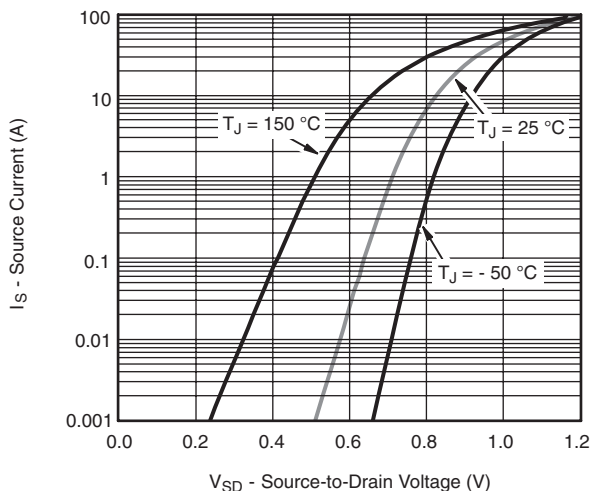
Gate Charge



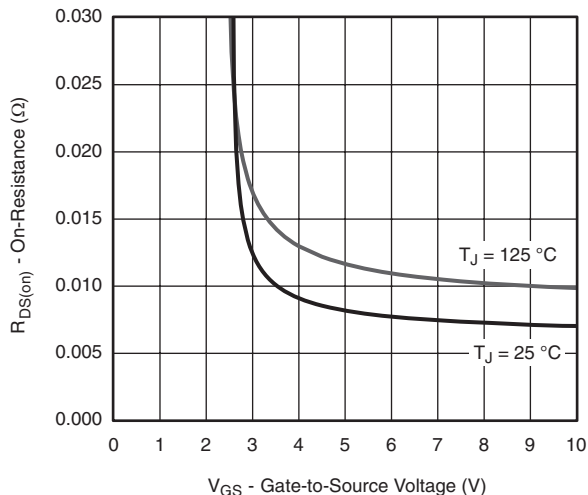
On-Resistance vs. Junction Temperature



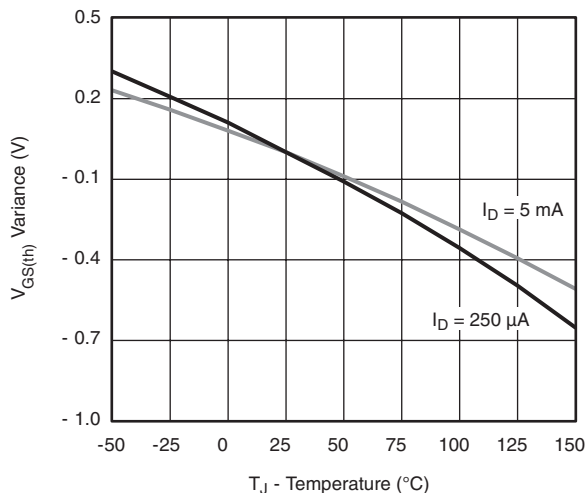
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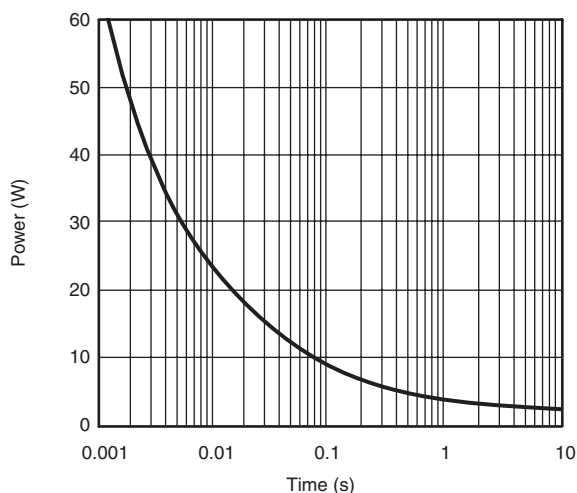
Source-Drain Diode Forward Voltage



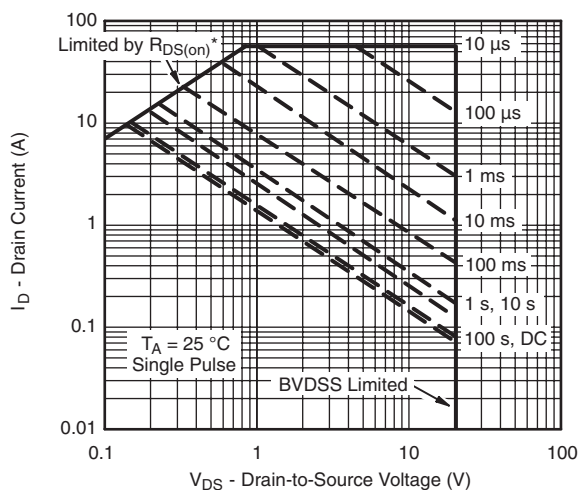
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

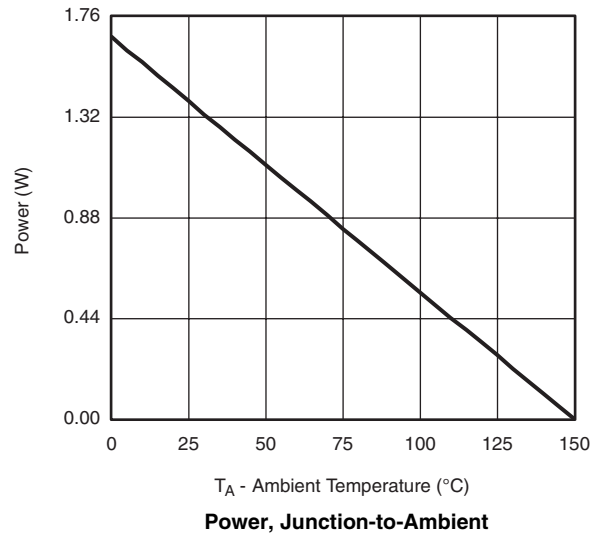
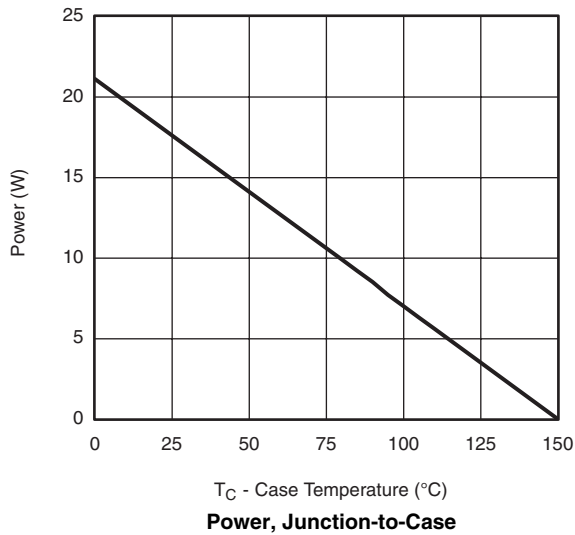
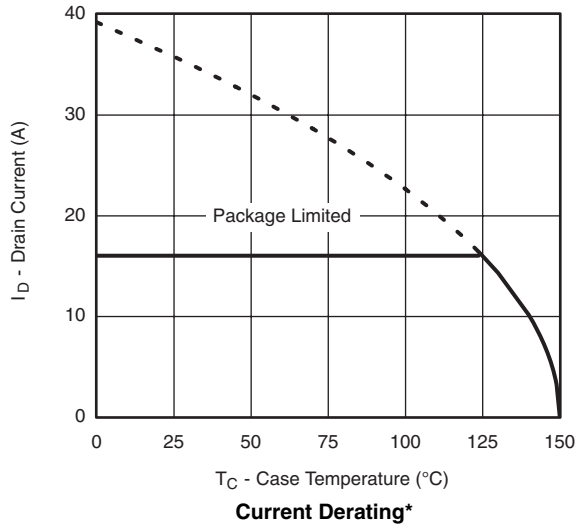
Safe Operating Area, Junction-to-Ambient

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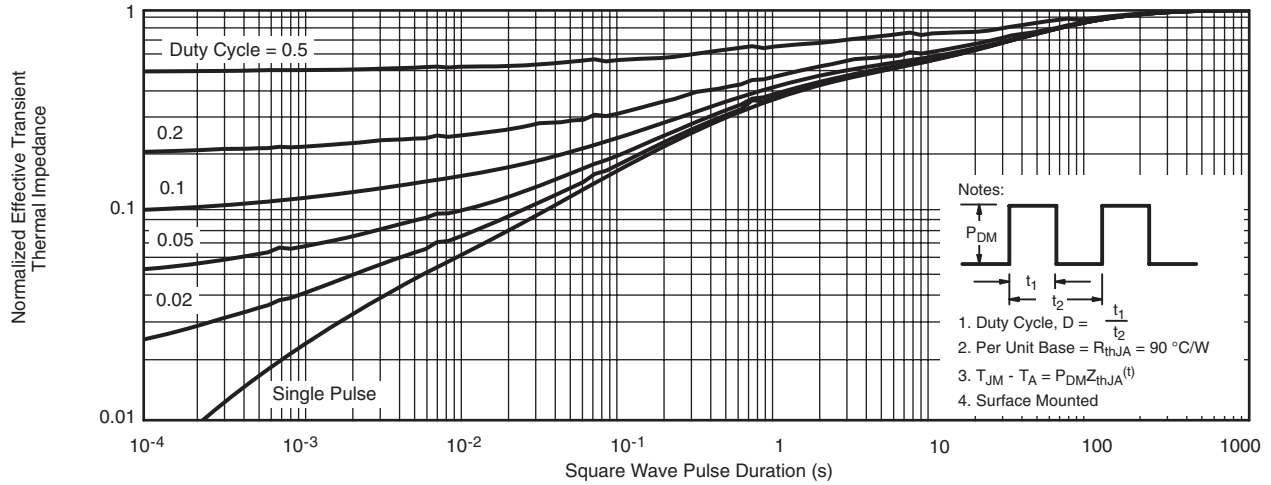
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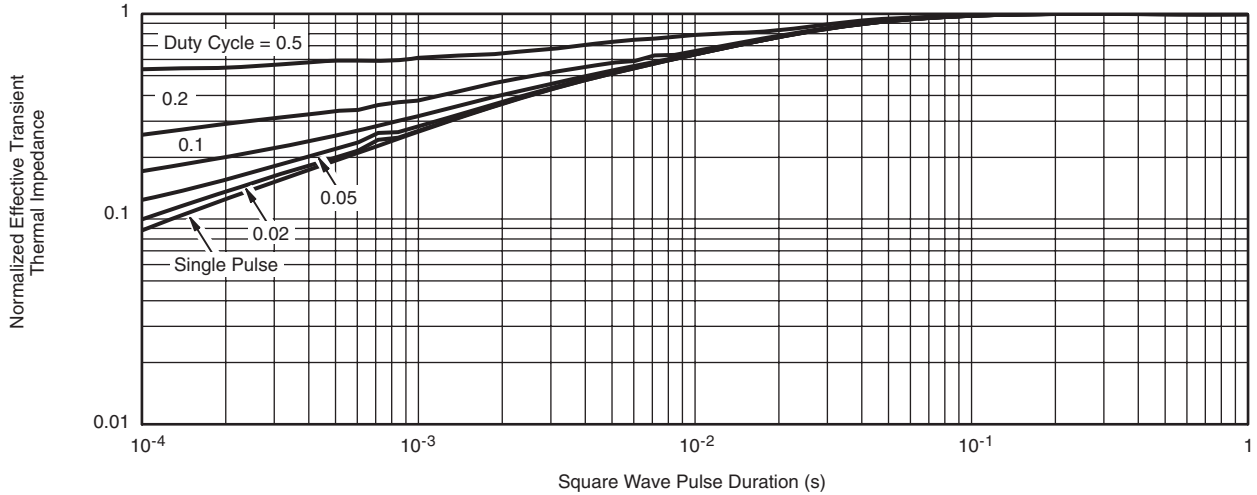
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



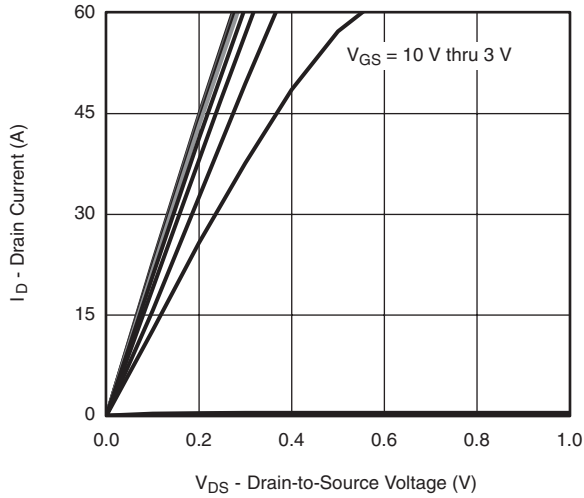
Normalized Thermal Transient Impedance, Junction-to-Case

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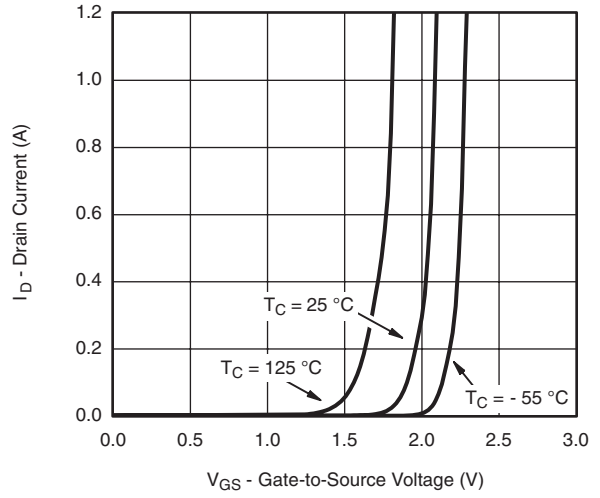
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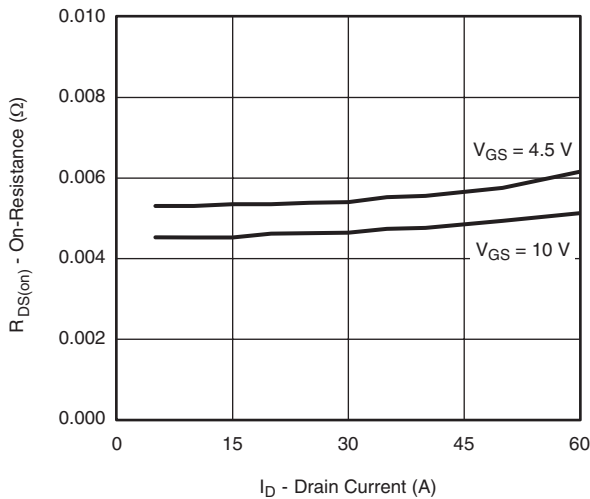
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



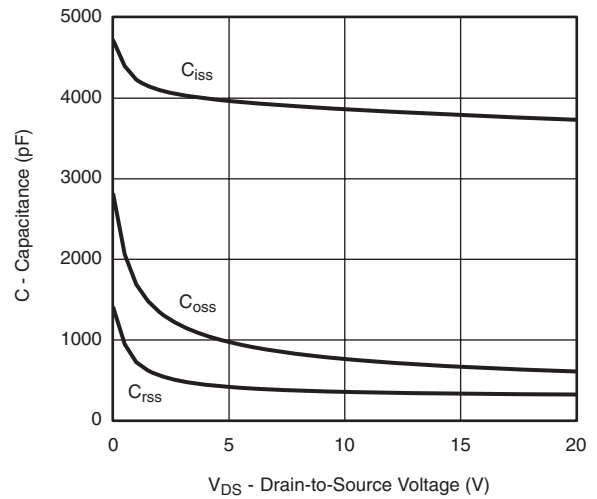
Output Characteristics



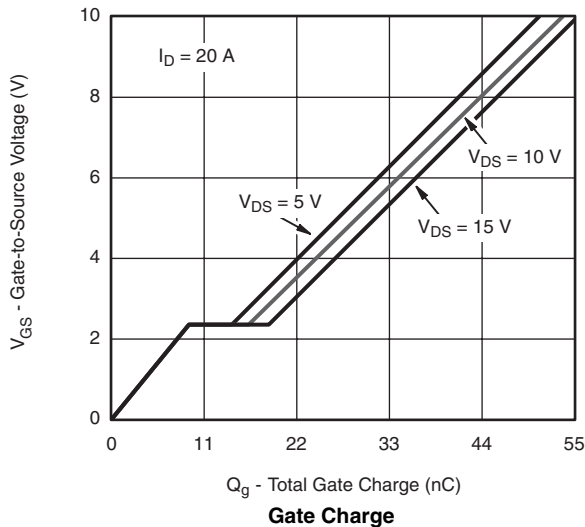
Transfer Characteristics



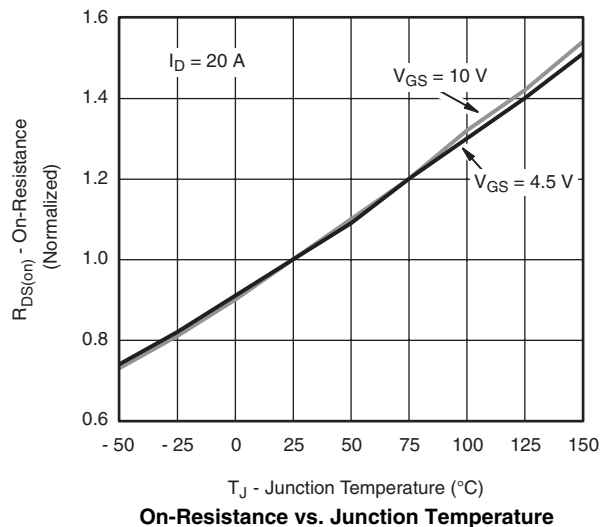
On-Resistance vs. Drain Current



Capacitance



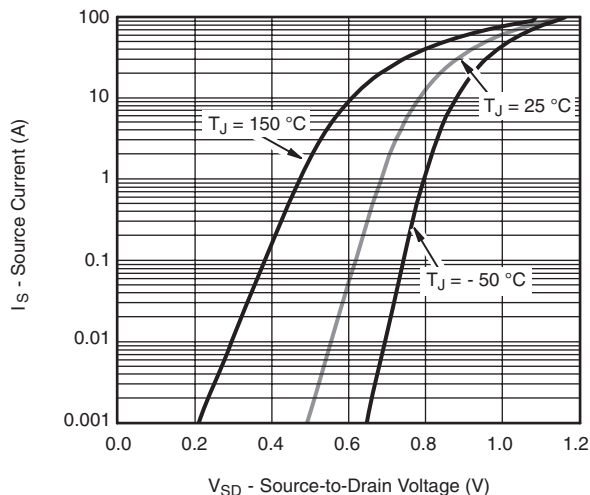
Gate Charge



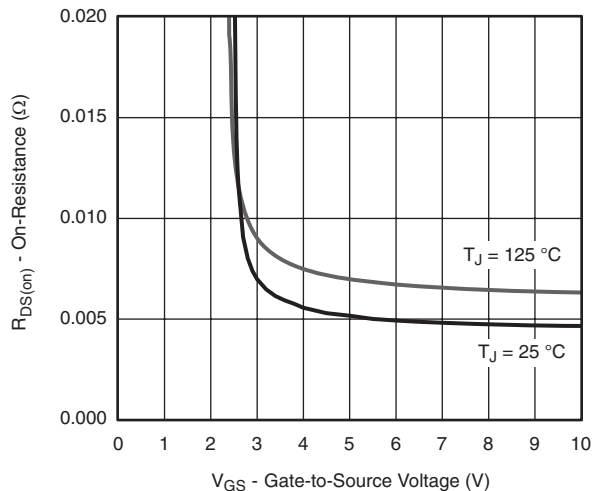
On-Resistance vs. Junction Temperature



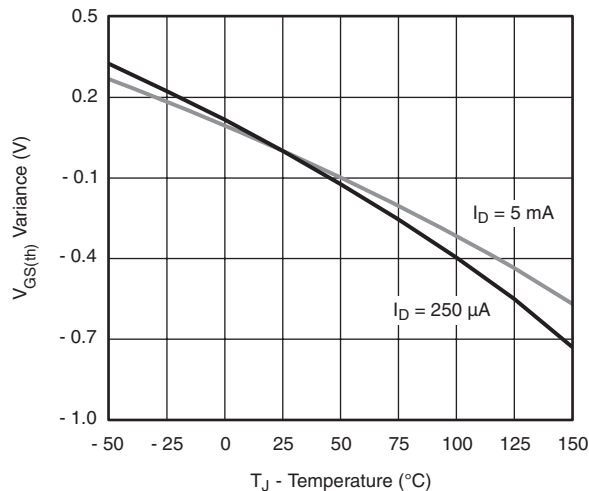
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



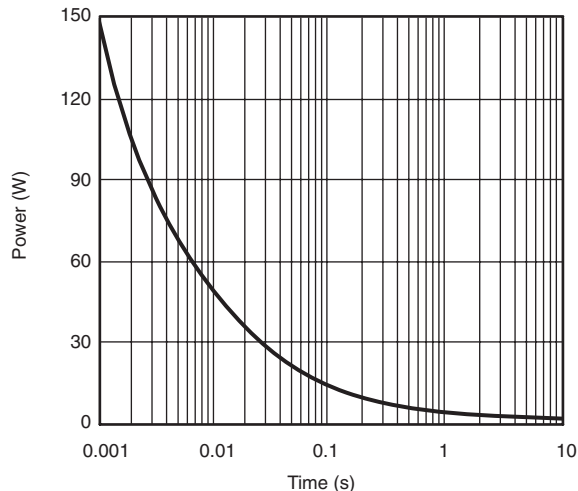
Source-Drain Diode Forward Voltage



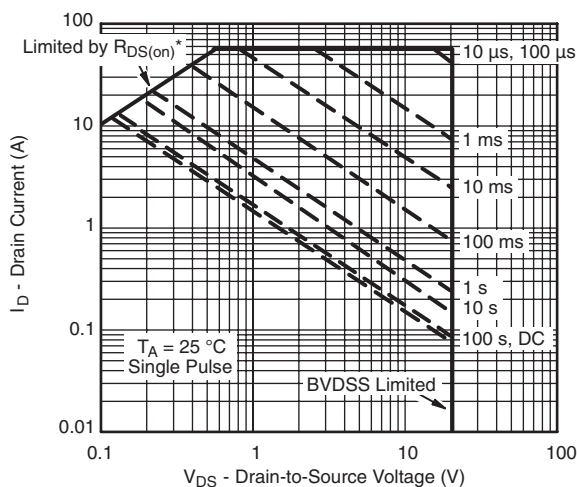
On-Resistance vs. Gate-to-Source



Threshold Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

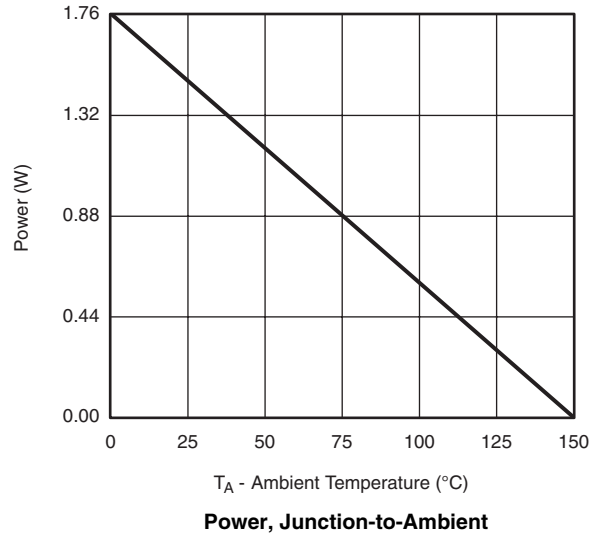
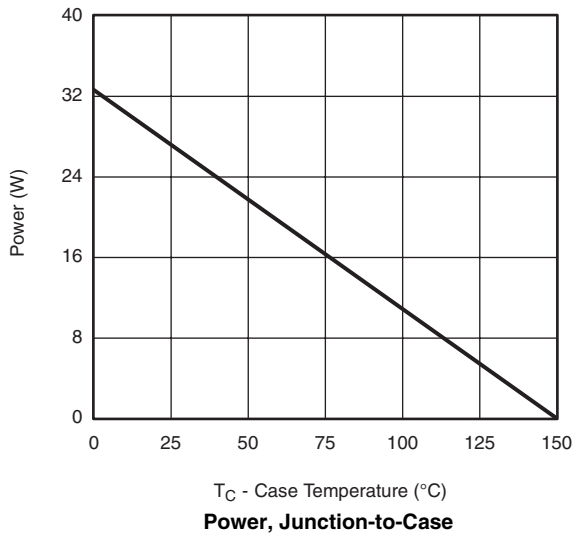
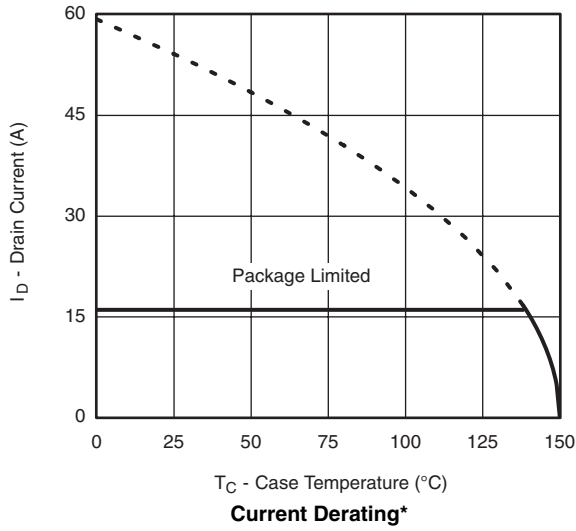
Safe Operating Area, Junction-to-Ambient

SiZ700DT

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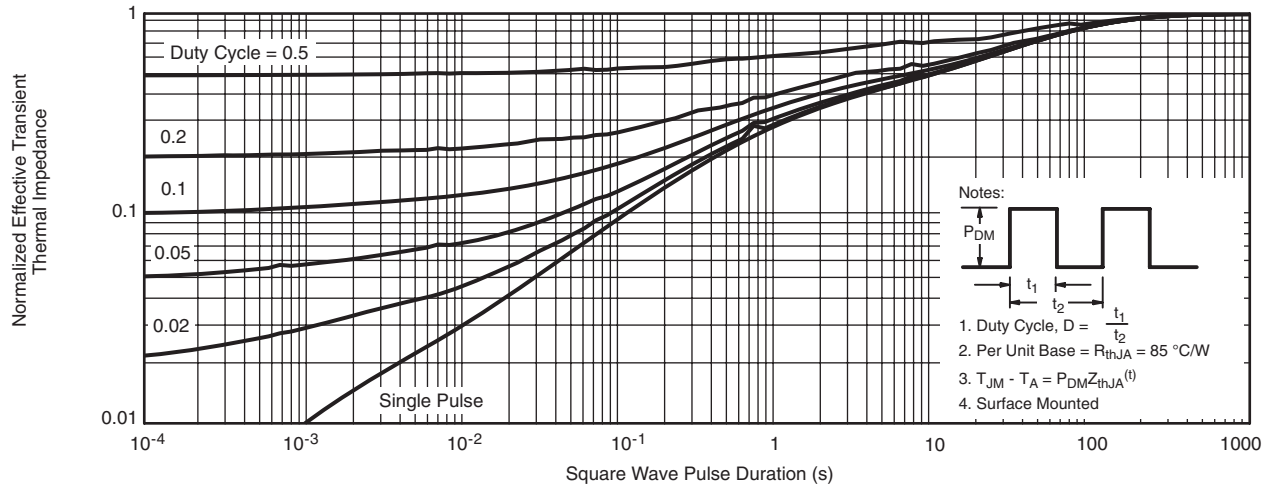
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



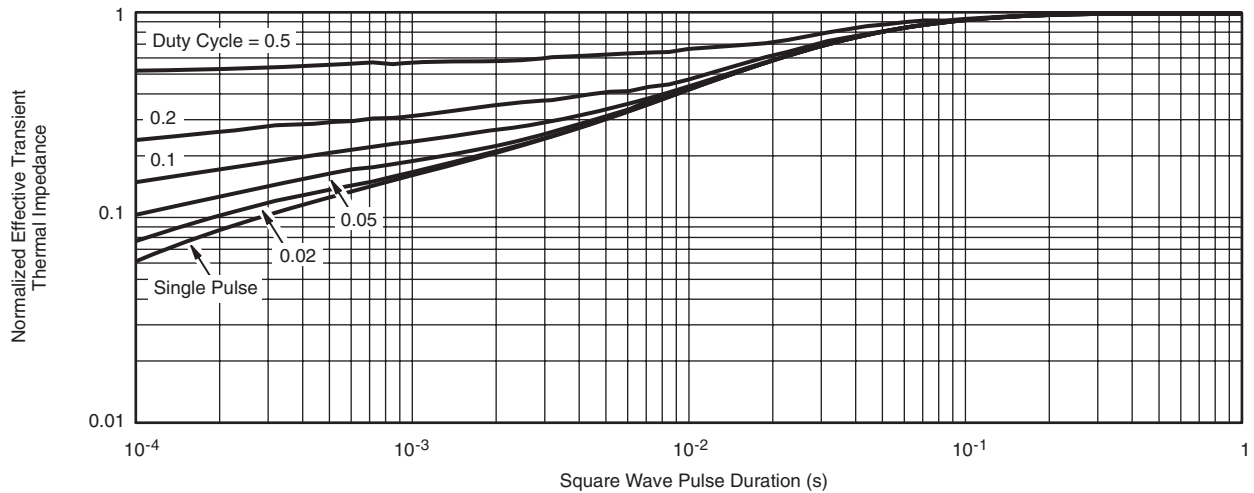
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CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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