

FEATURES

Ultralow power-down current: 0.3 μ A/amp max

Low quiescent current: 2.4 mA/amp

High speed

175 MHz -3 dB bandwidth

220 V/ μ s slew rate

85 ns settling time to 0.1%

Excellent video specifications

0.1 dB flatness: 14 MHz

Differential gain: 0.12%

Differential phase: 0.09°

Single-supply operation: 2.7 V to 6 V

Rail-to-rail output

Output swings to within 80 mV of either rail

Low voltage offset: 0.6 mV

APPLICATIONS

Portable multimedia players

Video cameras

Digital still cameras

Consumer video

GENERAL DESCRIPTION

The ADA4850-2¹ (dual) is a low price, high speed, voltage feedback rail-to-rail output op amp with ultralow power-down. Despite its low price, the ADA4850-2 provides excellent overall performance and versatility. The 175 MHz -3 dB bandwidth and 220 V/ μ s slew rate make this amplifier well-suited for many general-purpose, high speed applications.

The ADA4850-2 is designed to operate at supply voltages as low as 2.7 V and up to 6 V using only 2.4 mA of supply current per amplifier. To further reduce power consumption, the amplifier is equipped with a power-down mode, which lowers the supply current to less than 0.1 μ A, making it ideal in battery-powered applications.

The ADA4850 family provides users with a true single-supply capability, allowing input signals to extend 200 mV below the negative rail and to within 2.2 V of the positive rail. On the output, the amplifier can swing within 80 mV of either supply rail.

With its combination of low price, excellent differential gain (0.12%), differential phase (0.09°), and 0.1 dB flatness out to 14 MHz, this amplifier is ideal for video applications.

Rev. 0

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PIN CONFIGURATION

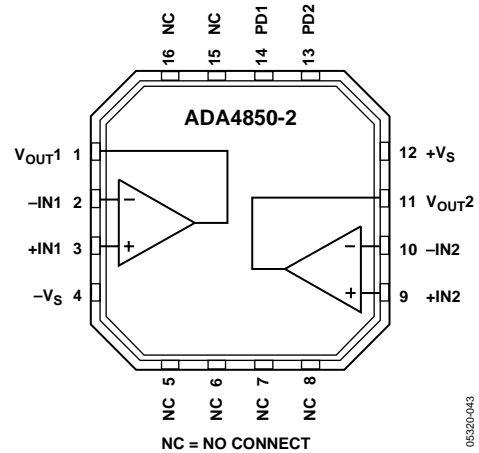


Figure 1. 16-Lead, 3 mm \times 3 mm LFCSP

The ADA4850-2 is available in a 16-lead, 3 mm \times 3 mm LFCSP and is designed to work in the extended temperature range (-40°C to $+125^{\circ}\text{C}$).

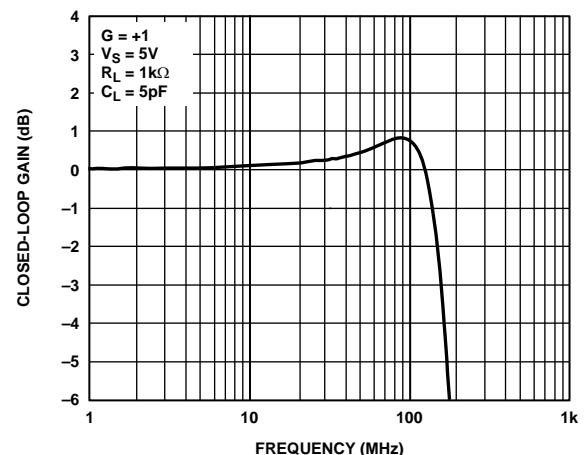


Figure 2. Small Signal Frequency Response

¹ Patent pending.

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REVISION HISTORY

2/05—Revision 0: Initial Version

SPECIFICATIONS WITH +3 V SUPPLY

$T_A = 25^\circ\text{C}$, $R_F = 0\ \Omega$ for $G = +1$, $R_F = 1\ \text{k}\Omega$ for $G > +1$, $R_L = 1\ \text{k}\Omega$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1$, $V_o = 0.1\ \text{V p-p}$		160		MHz
	$G = +2$, $V_o = 0.5\ \text{V p-p}$, $R_L = 150\ \Omega$		45		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_o = 0.5\ \text{V p-p}$, $R_L = 150\ \Omega$		14		MHz
Slew Rate	$G = +2$, $V_o = 1\ \text{V Step}$		110		V/ μs
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	$f = 100\ \text{kHz}$		10		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\ \text{kHz}$		2.5		pA/ $\sqrt{\text{Hz}}$
Differential Gain	$G = +3$, NTSC, $R_L = 150\ \Omega$, $V_o = 2\ \text{V p-p}$		0.2		%
Differential Phase	$G = +3$, NTSC, $R_L = 150\ \Omega$, $V_o = 2\ \text{V p-p}$		0.2		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.6	4.1	mV
Input Offset Voltage Drift			4		$\mu\text{V}/^\circ\text{C}$
Input Bias Current			2.4	4.4	μA
Input Bias Current Drift			4		nA/ $^\circ\text{C}$
Input Bias Offset Current			30		nA
Open-Loop Gain	$V_o = 0.25\ \text{V to } 0.75\ \text{V}$	78	102		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential/common-mode		0.5/5.0		M Ω
Input Capacitance			1.2		pF
Input Common-Mode Voltage Range			-0.2 to +0.8		V
Input Overdrive Recovery Time (Rise/Fall)	$V_{IN} = +3.5\ \text{V to } -0.5\ \text{V}$, $G = +1$		60/50		ns
Common-Mode Rejection Ratio	$V_{CM} = 0.5\ \text{V}$	-76	-108		dB
POWER-DOWN					
Power-Down Input Voltage	Power-down		<0.6		V
	Enabled		>1.7		V
Turn-Off Time			0.7		μs
Turn-On Time			60		ns
Power-Down Bias Current					
Enabled	Power-down = 3 V		37	47	μA
Power-Down	Power-down = 0 V		0.01	0.16	μA
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	$V_{IN} = +0.7\ \text{V to } -0.1\ \text{V}$, $G = +5$		70/100		ns
Output Voltage Swing		0.06 to 2.83	0.03 to 2.92		V
Short-Circuit Current	Sinking/sourcing		105/74		mA
POWER SUPPLY					
Operating Range ¹		2.7		6	V
Quiescent Current	Both amplifiers enabled		4.7	5.4	mA
Quiescent Current (Power-Down)	Power-down = low		<0.1	0.3	μA
Positive Power Supply Rejection	$+V_S = +3\ \text{V to } +4\ \text{V}$, $-V_S = 0\ \text{V}$	-83	-100		dB
Negative Power Supply Rejection	$+V_S = +3\ \text{V}$, $-V_S = 0\ \text{V to } -1\ \text{V}$	-83	-102		dB

¹ For operation on bipolar supplies, see the Operating the ADA4850-2 on Bipolar Supplies section.

ADA4850-2

SPECIFICATIONS WITH +5 V SUPPLY

$T_A = 25^\circ\text{C}$, $R_F = 0\ \Omega$ for $G = +1$, $R_F = 1\ \text{k}\Omega$ for $G > +1$, $R_L = 1\ \text{k}\Omega$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1$, $V_o = 0.1\ \text{V p-p}$		175		MHz
	$G = +1$, $V_o = 0.5\ \text{V p-p}$		110		MHz
Bandwidth for 0.1 dB Flatness	$G = +2$, $V_o = 1.4\ \text{V p-p}$, $R_L = 150\ \Omega$		9		MHz
Slew Rate	$G = +2$, $V_o = 4\ \text{V Step}$		220		V/ μs
	$G = +2$, $V_o = 2\ \text{V Step}$		160		V/ μs
Settling Time to 0.1%	$G = +2$, $V_o = 1\ \text{V Step}$, $R_L = 150\ \Omega$		85		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	$f = 100\ \text{kHz}$		10		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\ \text{kHz}$		2.5		pA/ $\sqrt{\text{Hz}}$
Differential Gain	$G = +3$, NTSC, $R_L = 150\ \Omega$		0.12		%
Differential Phase	$G = +3$, NTSC, $R_L = 150\ \Omega$		0.09		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.6	4.2	mV
Input Offset Voltage Drift			4		$\mu\text{V}/^\circ\text{C}$
Input Bias Current			2.3	4.2	μA
Input Bias Current Drift			4		nA/ $^\circ\text{C}$
Input Bias Offset Current			30		nA
Open-Loop Gain	$V_o = 2.25\ \text{V to } 2.75\ \text{V}$	83	108		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential/common-mode		0.5/5.0		M Ω
Input Capacitance			1.2		pF
Input Common-Mode Voltage Range			-0.2 to +2.8		V
Input Overdrive Recovery Time (Rise/Fall)	$V_{IN} = +5.5\ \text{V to } -0.5\ \text{V}$, $G = +1$		50/40		ns
Common-Mode Rejection Ratio	$V_{CM} = 2.0\ \text{V}$	-85	-110		dB
POWER-DOWN					
Power-Down Input Voltage	Power-down		<0.6		V
	Enabled		>1.7		V
Turn-Off Time			0.7		μs
Turn-On Time			50		ns
Power-Down Bias Current					
Enabled	Power-down = 5 V		52	71	μA
Power-Down	Power-down = 0 V		0.02	0.17	μA
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	$V_{IN} = +1.1\ \text{V to } -0.1\ \text{V}$, $G = +5$		60/70		ns
Output Voltage Swing		0.14 to 4.83	0.07 to 4.92		V
Short-Circuit Current	Sinking/sourcing		118/94		mA
POWER SUPPLY					
Operating Range ¹		2.7		6	V
Quiescent Current	Both amplifiers enabled		4.9	5.6	mA
Quiescent Current (Power-Down)	Power-down = low		<0.1	0.3	μA
Positive Power Supply Rejection	$+V_S = +5\ \text{V to } +6\ \text{V}$, $-V_S = 0\ \text{V}$	-84	-98		dB
Negative Power Supply Rejection	$+V_S = +5\ \text{V}$, $-V_S = -0\ \text{V to } -1\ \text{V}$	-84	-102		dB

¹ For operation on bipolar supplies, see the Operating the ADA4850-2 on Bipolar Supplies section.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Power Down Pin Voltage	(-V _S + 6) V
Common-Mode Input Voltage	(-V _S - 0.5) V to (+V _S + 0.5) V
Differential Input Voltage	+V _S to -V _S
Storage Temperature	-65°C to +125°C
Operating Temperature Range	-40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in the circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ _{JA}	Unit
LFCSP	91	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4850-2 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4850-2. Exceeding a junction temperature of 150°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4850-2 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L} \right) - \frac{V_{OUT}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to -V_S, as in single-supply operation, the total drive power is V_S × I_{OUT}. If the rms signal levels are indeterminate, consider the worst case, when V_{OUT} = V_S/4 for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to -V_S, the worst case is V_{OUT} = V_S/2.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduce θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the LFCSP (91°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

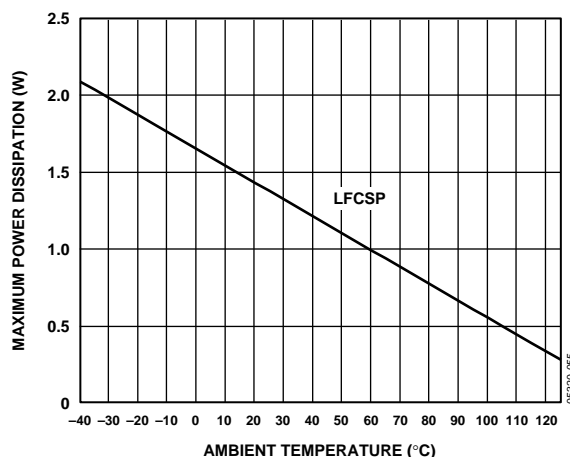


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board



TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, R_F = 0 Ω for G = +1, R_F = 1 kΩ for G > +1, R_L = 1 kΩ, unless otherwise noted.

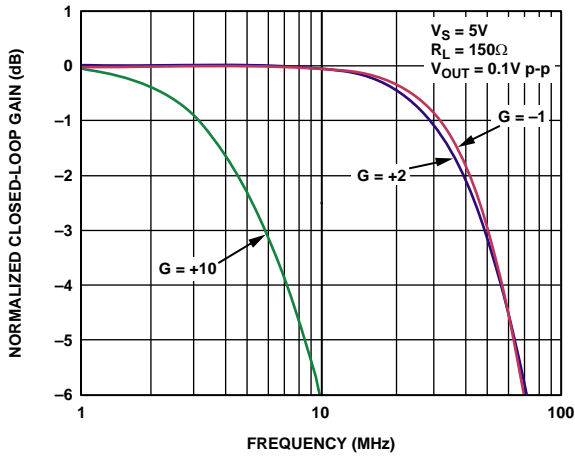


Figure 4. Small Signal Frequency Response for Various Gains

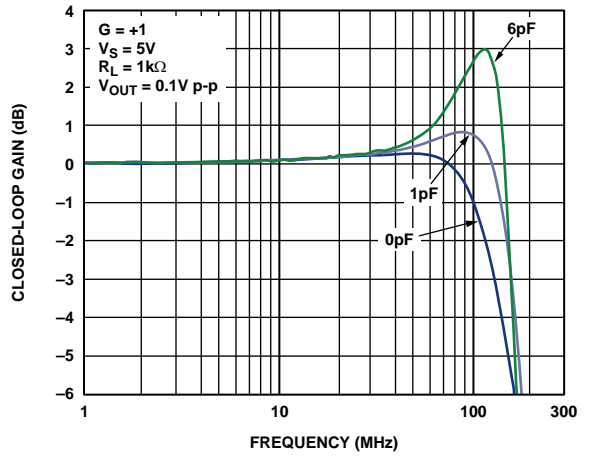


Figure 7. Small Signal Frequency Response for Various Capacitor Loads

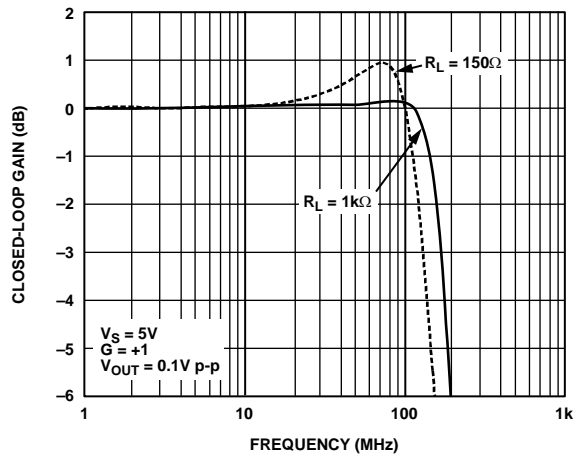


Figure 5. Small Signal Frequency Response for Various Loads

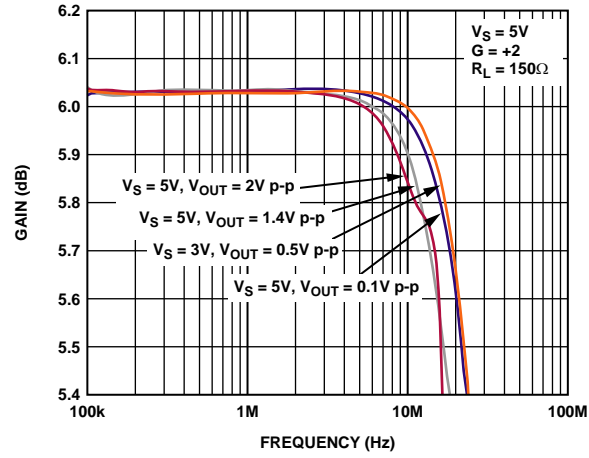


Figure 8. 0.1 dB Flatness Response

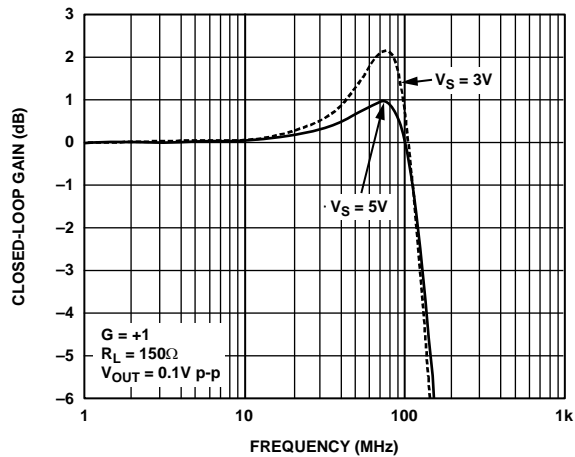


Figure 6. Small Signal Frequency Response for Various Supplies

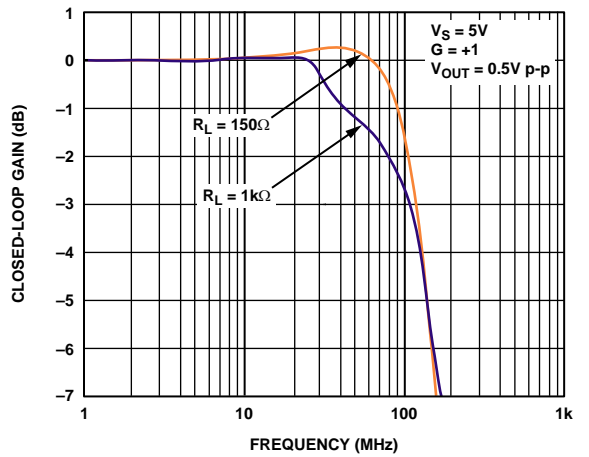


Figure 9. Large Frequency Response for Various Loads

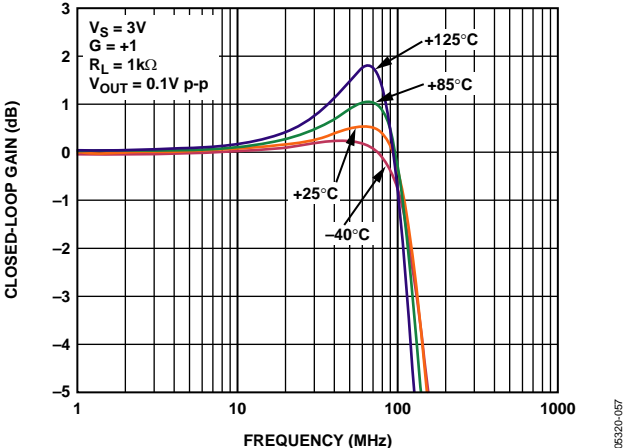


Figure 10. Small Signal Frequency Response for Various Temperatures

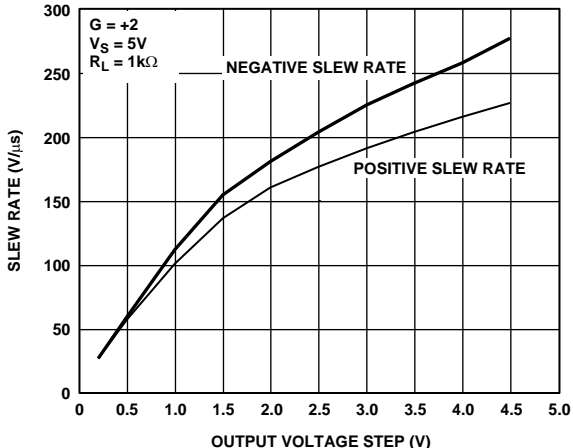


Figure 13. Slew Rate vs. Output Voltage

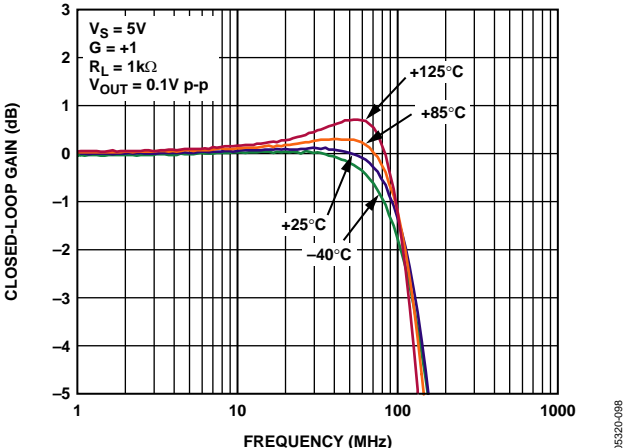


Figure 11. Small Signal Frequency Response for Various Temperatures

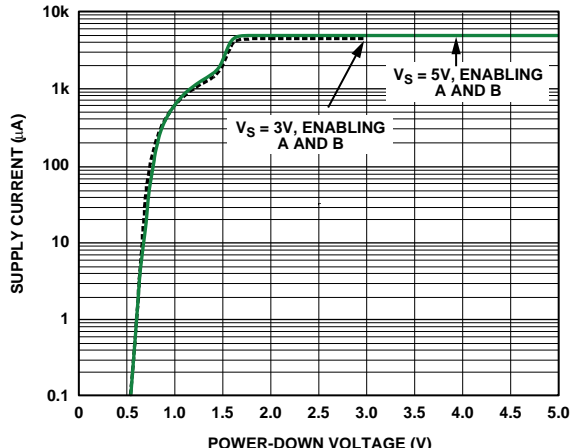


Figure 14. Supply Current vs. Power-Down Voltage

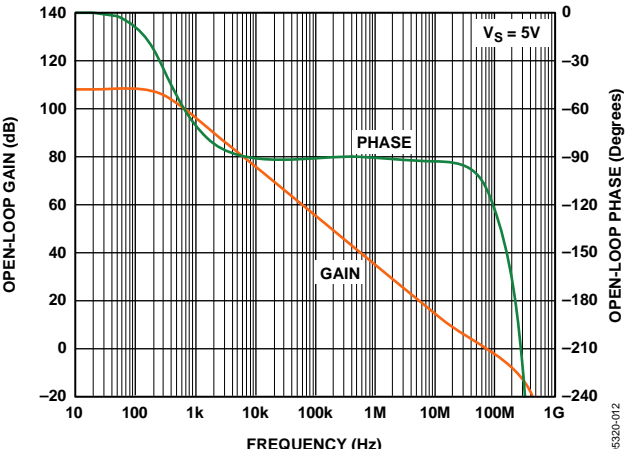


Figure 12. Open-Loop Gain and Phase vs. Frequency

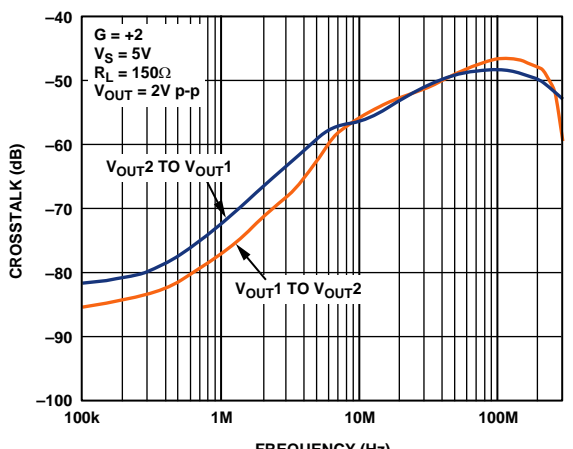


Figure 15. Crosstalk vs. Frequency

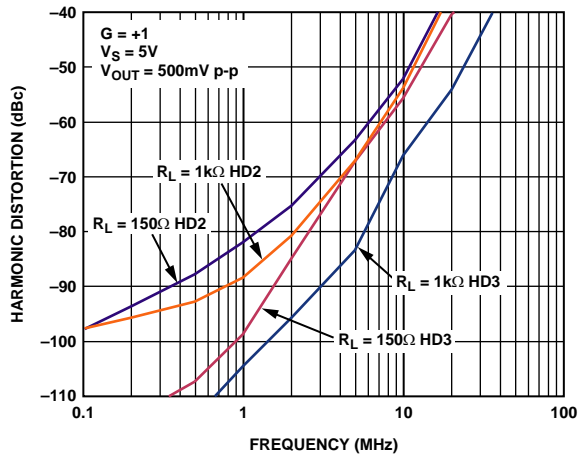


Figure 16. Harmonic Distortion vs. Frequency for Various Loads

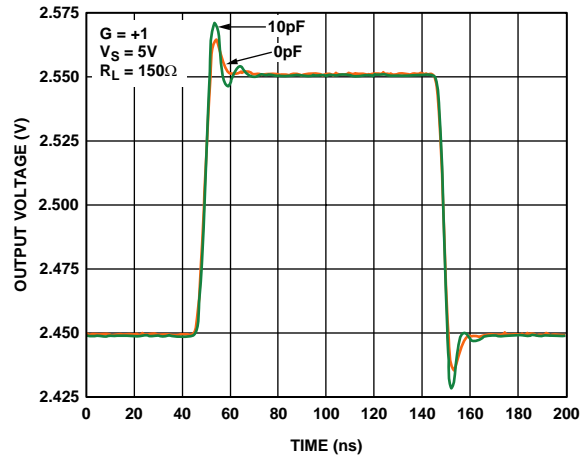


Figure 19. Small Signal Transient Response for Capacitive Load

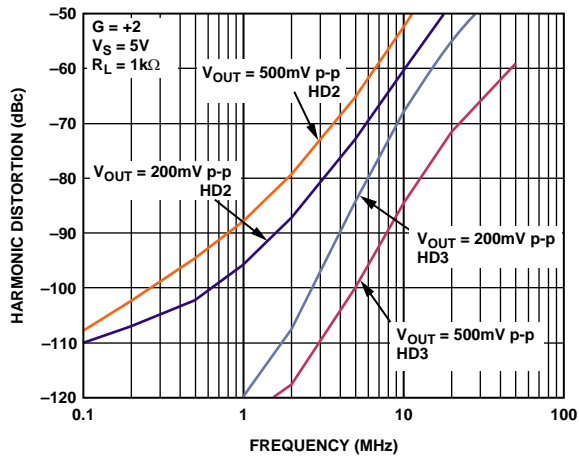


Figure 17. Harmonic Distortion vs. Frequency for Various V_{OUT}

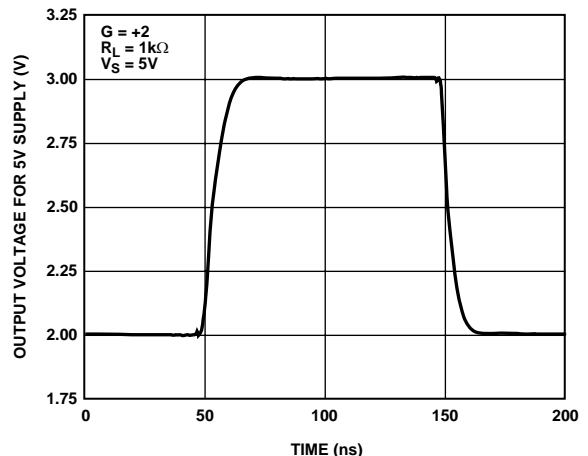


Figure 20. Large Signal Transient Response

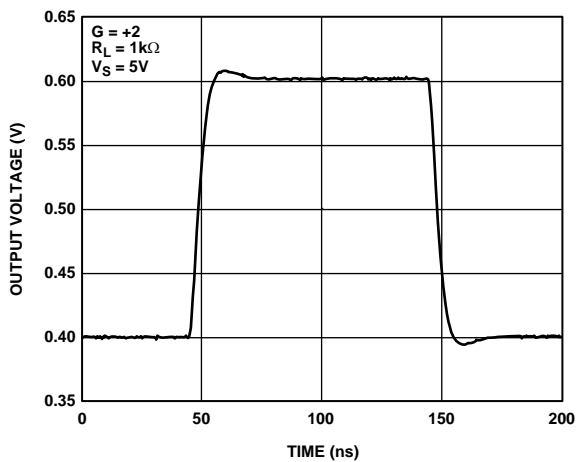


Figure 18. Small Signal Transient Response for Various Supplies

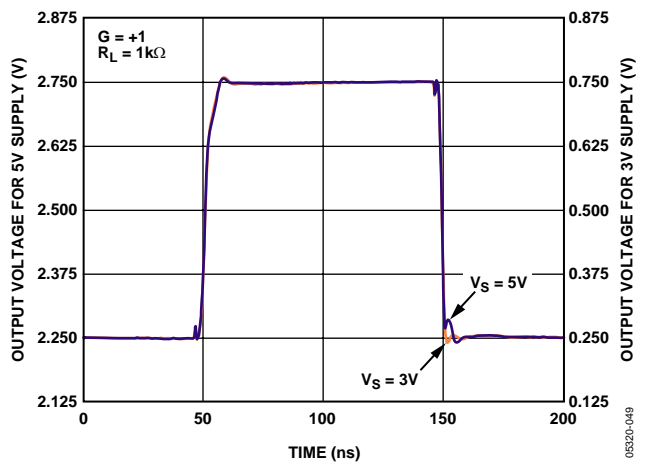


Figure 21. Large Signal Transient Response for Various Supplies

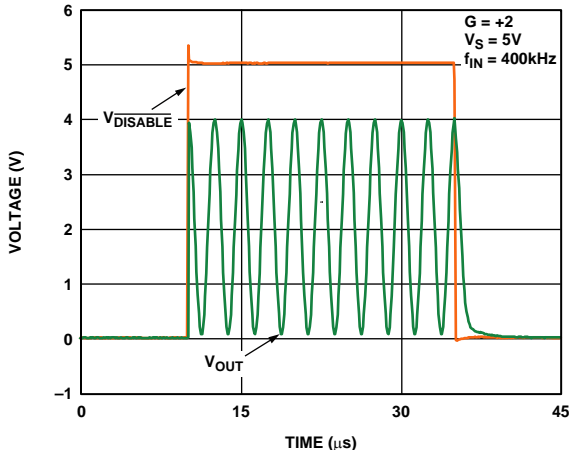


Figure 22. Enable/Disable Time

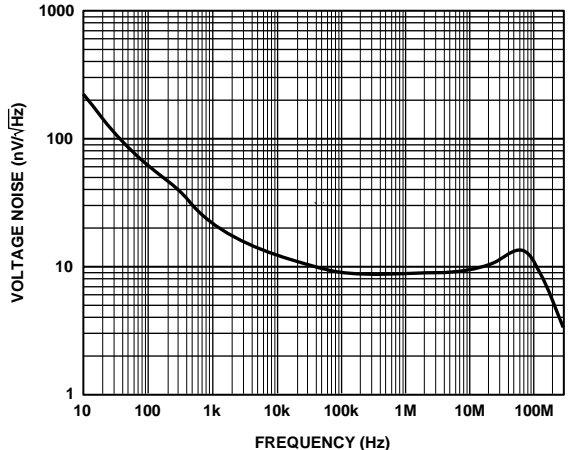


Figure 25. Voltage Noise vs. Frequency

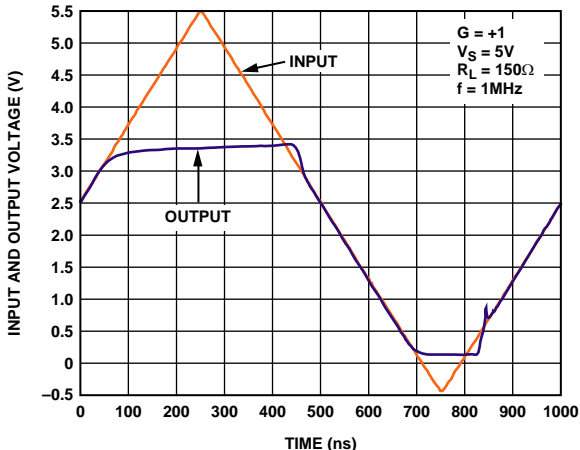


Figure 23. Input Overdrive Recovery

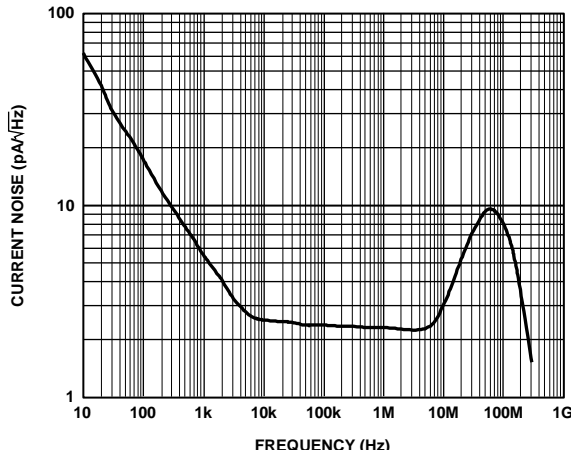


Figure 26. Current Noise vs. Frequency

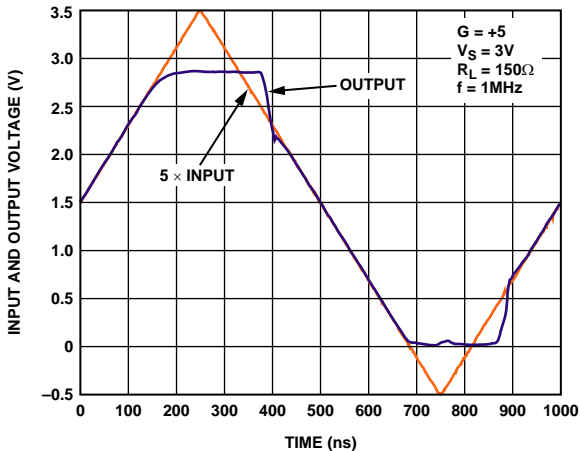


Figure 24. Output Overdrive Recovery

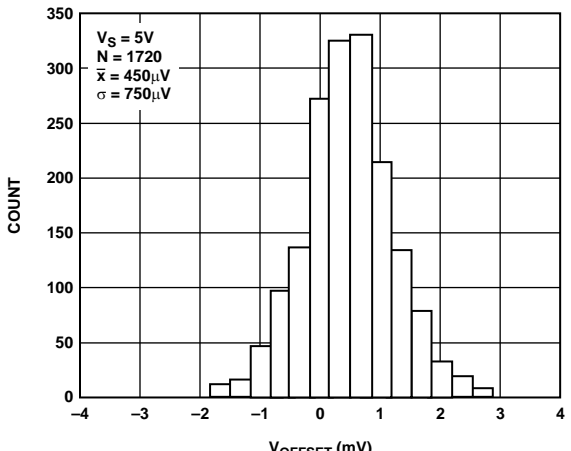


Figure 27. Input Offset Voltage Distribution

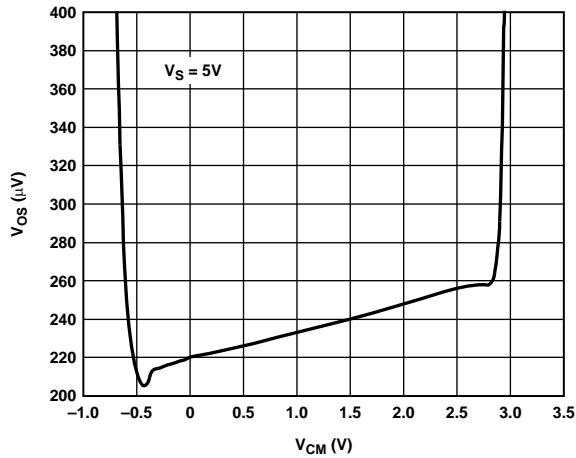


Figure 28. Input Offset Voltage vs. Common-Mode Voltage

05320-063

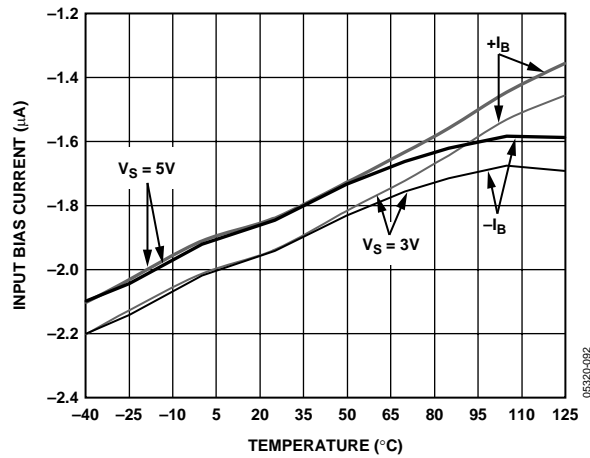


Figure 31. Input Bias Current vs. Temperature for Various Supplies

05320-082

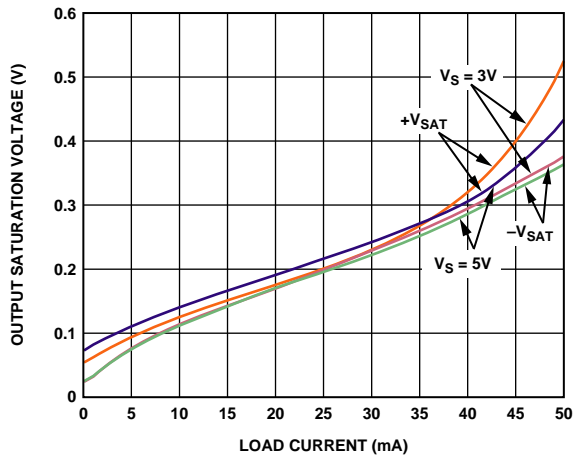


Figure 29. Output Saturation Voltage vs. Load Current (Voltage Differential from Rails)

05320-064

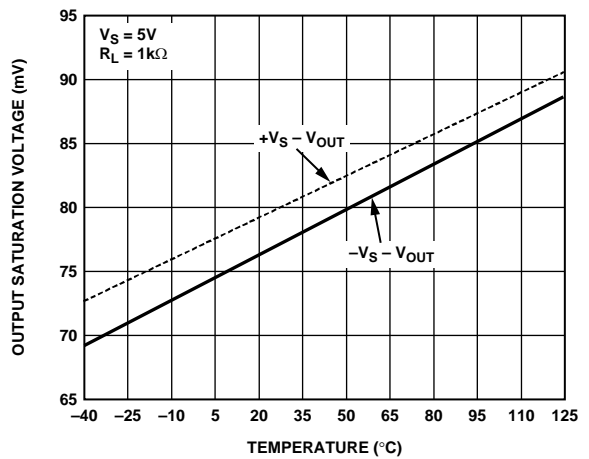


Figure 32. Output Saturation Voltage vs. Temperature (Voltage Differential from Rails)

05320-062

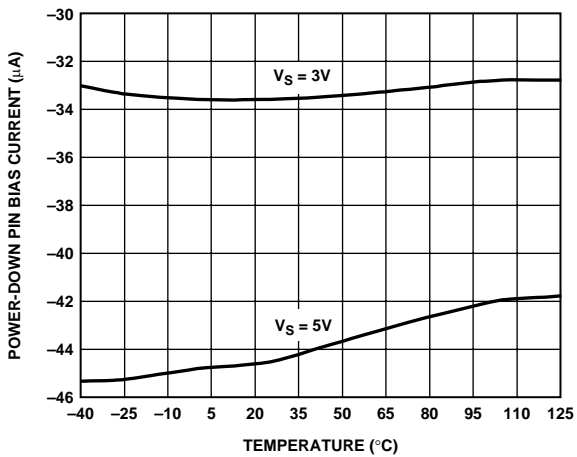


Figure 30. Power-Down Bias Current vs. Temperature for Various Supplies

05320-081

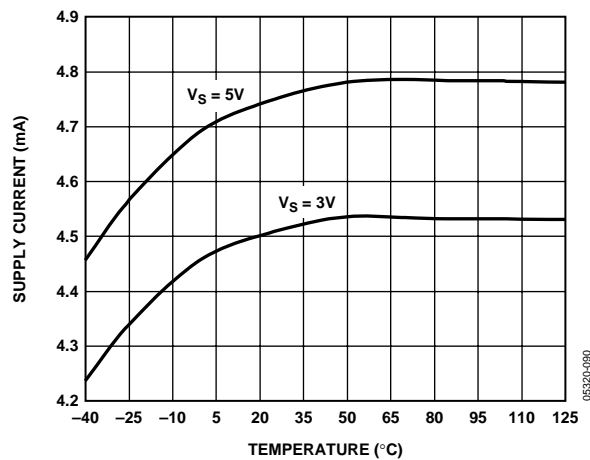


Figure 33. Current vs. Temperature for Various Supplies

05320-080

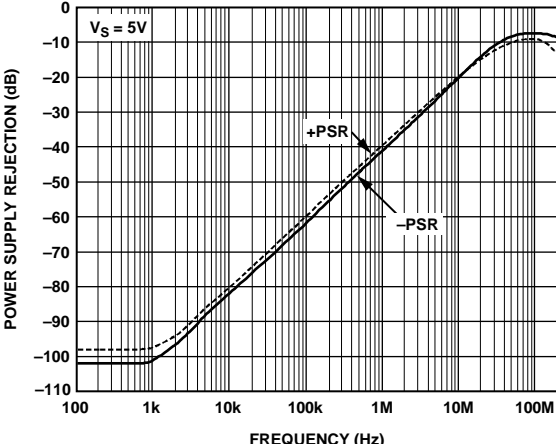


Figure 34. Power Supply Rejection (PSR) vs. Frequency

05320-094

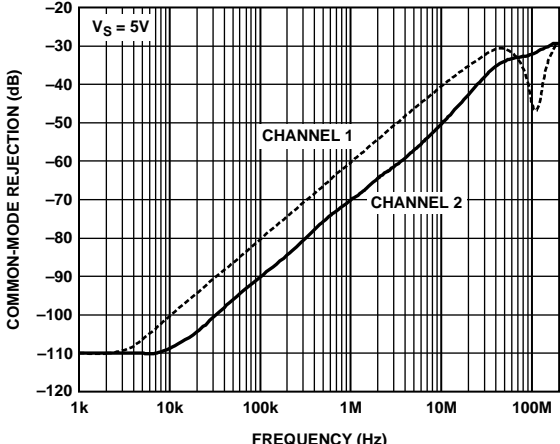


Figure 36. Common-Mode Rejection Ratio (CMRR) vs. Frequency

05320-034

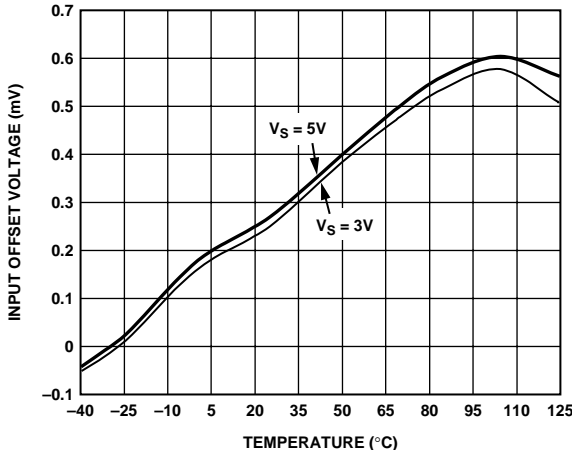


Figure 35. Input Offset Voltage vs. Temperature for Various Supplies

05320-093

CIRCUIT DESCRIPTION

The ADA4850-2 features a high slew rate input stage that is a true single-supply topology, capable of sensing signals at or below the negative supply rail. The rail-to-rail output stage can swing to within 80 mV of either supply rail when driving light loads and within 0.17 V when driving 150 Ω. High speed performance is maintained at supply voltages as low as 2.7 V.

HEADROOM AND OVERDRIVE RECOVERY CONSIDERATIONS

Input

The ADA4850-2 is designed for use in low voltage systems. To obtain optimum performance, it is useful to understand the behavior of the amplifier as input and output signals approach the amplifier's headroom limits. The input common-mode voltage range extends 200 mV below the negative supply voltage or ground for single-supply operation to within 2.2 V of the positive supply voltage. Therefore, in a gain of +3, the ADA4850-2 can provide full rail-to-rail output swing for supply voltage as low as 3.3 V, assuming the input signal swing is from $-V_s$ (or ground) to 1.1 V.

Exceeding the headroom limit is not a concern for any inverting gain on any supply voltage, as long as the reference voltage at the amplifier's positive input lies within the amplifier's input common-mode range.

The input stage sets the headroom limit for signals when the amplifier is used in a gain of +1 for signals approaching the positive rail. For high speed signals, however, there are other considerations. Figure 37 shows -3 dB bandwidth vs. dc input voltage for a unity-gain follower. As the common-mode voltage approaches the positive supply, the bandwidth begins to drop when within 2 V of $+V_s$. This can manifest itself in increased distortion or settling time.

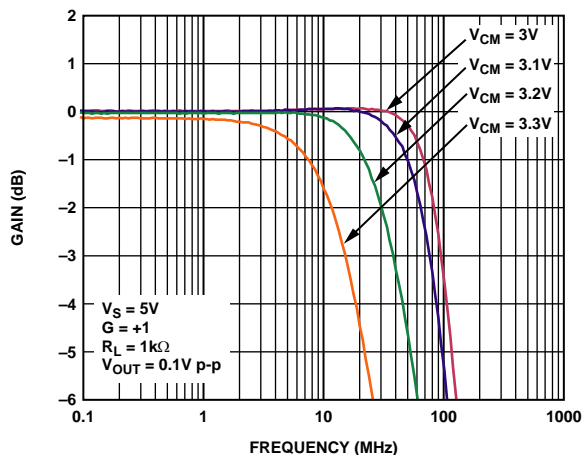


Figure 37. Unity-Gain Follower Bandwidth vs. Frequency for Various Input Common-Mode

Higher frequency signals require more headroom than the lower frequencies to maintain distortion performance. Figure 38 illustrates how the rising edge settling time for the amplifier configured as a unity-gain follower stretches out as the top of a 1 V step input approaches and exceeds the specified input common-mode voltage limit.

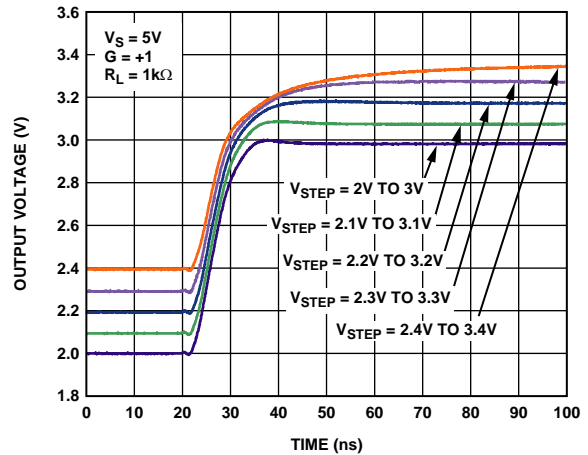


Figure 38. Pulse Response, Input Headroom Limits

The recovery time from input voltages 2.2 V or closer to the positive supply is approximately 50 ns, which is limited by the settling artifacts caused by transistors in the input stage coming out of saturation.

The ADA4850-2 does not exhibit phase reversal, even for input voltages beyond the voltage supply rails. Going more than 0.6 V beyond the power supplies turns on protection diodes at the input stage, which greatly increase the current draw of the devices.

Output

For signals approaching the negative supply and inverting gain, and high positive gain configurations, the headroom limit is the output stage. The ADA4850-2 amplifiers use a common-emitter output stage. This output stage maximizes the available output range, limited by the saturation voltage of the output transistors. The saturation voltage increases with drive current, due to the output transistor collector resistance.

As the saturation point of the output stage is approached, the output signal shows increasing amounts of compression and clipping. As in the input headroom case, higher frequency signals require a bit more headroom than the lower frequency signals.

Output overload recovery is typically within 40 ns after the amplifier's input is brought to a nonoverloading value.

Figure 39 shows the output recovery transients for the amplifier recovering from a saturated output from the top and bottom supplies to a point at midsupply.

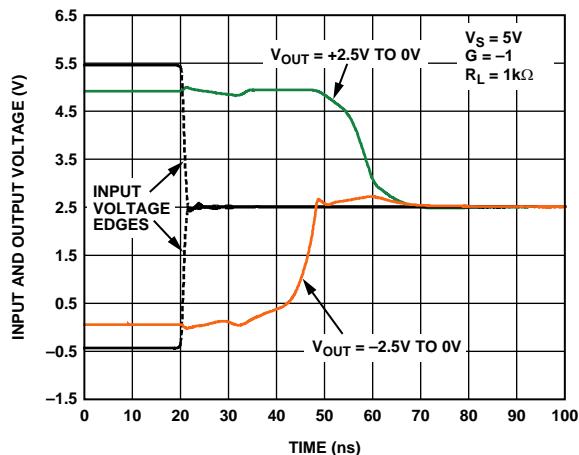


Figure 39. Overload Recovery

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OPERATING THE ADA4850-2 ON BIPOLAR SUPPLIES

The ADA4850-2 can operate on bipolar supplies up to ± 5 V. The only restriction is that the voltage between $-V_S$ and the power-down pin must not exceed 6 V. Voltage differences greater than 6 V can cause permanent damage to the amplifier. For example, when operating on ± 5 V supplies, the power-down pin must not exceed +1 V.

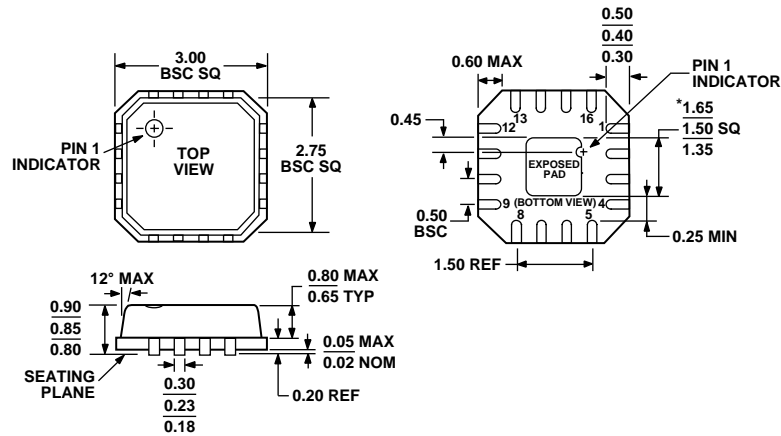
POWER-DOWN PIN

The ADA4850-2 features an ultralow power-down mode that lowers the supply current to less than $0.1 \mu\text{A}$. When a power-down pin (Pin 13 or Pin 14) is brought to within 1 V of the negative supply, the amplifier is powered down. Table 5 outlines the power-down pin functionality. The power-down pins (PD) should not be left floating.

Table 5. Power-Down Pin Functionality

Supply Voltage	3 V	5 V
Powered Down	0 V to 0.6 V	0 V to 0.6 V
Enabled	1.7 V to 3 V	1.7 V to 5 V

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2 EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 40. 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding
ADA4850-2YCPZ-R2 ¹	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP)	CP-16-3	HTB
ADA4850-2YCPZ-RL ¹	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP)	CP-16-3	HTB
ADA4850-2YCPZ-RL7 ¹	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP)	CP-16-3	HTB

¹ Z = Pb-free part.

NOTES

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