

# ADS7841

## 12-Bit, 4-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

### FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL SINGLE-ENDED OR 2-CHANNEL DIFFERENTIAL INPUT
- UP TO 200kHz CONVERSION RATE
- $\pm 1$  LSB MAX INL AND DNL
- GUARANTEED NO MISSING CODES
- 72dB SINAD
- SERIAL INTERFACE
- 16-PIN PDIP OR 16-LEAD SSOP PACKAGE
- ALTERNATE SOURCE FOR MAX1247

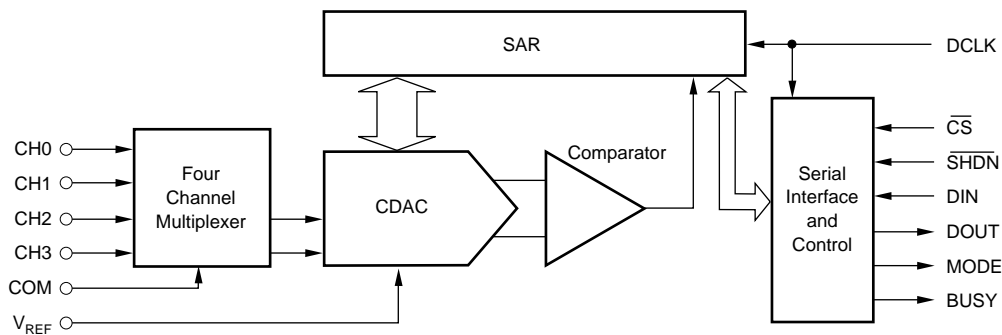
### APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

### DESCRIPTION

The ADS7841 is a 4-channel, 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 or 12 bits. Typical power dissipation is 2mW at a 200kHz throughput rate and a +5V supply. The reference voltage ( $V_{REF}$ ) can be varied between 100mV and  $V_{CC}$ , providing a corresponding input voltage range of 0V to  $V_{REF}$ . The device includes a shutdown mode which reduces power dissipation to under 15 $\mu$ W. The ADS7841 is guaranteed down to 2.7V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a 16-pin PDIP or a 16-lead SSOP package and is guaranteed over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.



# SPECIFICATION: +5V

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $V_{REF} = +5\text{V}$ ,  $f_{SAMPLE} = 200\text{kHz}$ , and  $f_{CLK} = 16 \cdot f_{SAMPLE} = 3.2\text{MHz}$ , unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ANALOG INPUT</b>								
Full-Scale Input Span	Positive Input - Negative Input	0		$V_{REF}$	*		*	V
Absolute Input Range	Positive Input	-0.2		$+V_{CC} + 0.2$	*		*	V
	Negative Input	-0.2		+1.25	*		*	V
Capacitance			25			*		pF
Leakage Current			$\pm 1$			*		$\mu\text{A}$
<b>SYSTEM PERFORMANCE</b>								
Resolution		12	12		12	*		Bits
No Missing Codes		12			12	*		Bits
Integral Linearity Error				$\pm 2$			$\pm 1$	LSB <sup>(1)</sup>
Differential Linearity Error			$\pm 0.8$	$\pm 3$		$\pm 0.5$	$\pm 1$	LSB
Offset Error				$\pm 3$			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				$\pm 4$			$\pm 3$	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		$\mu\text{V}_{\text{rms}}$
Power Supply Rejection			70			*		dB
<b>SAMPLING DYNAMICS</b>								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				200			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
<b>DYNAMIC CHARACTERISTICS</b>								
Total Harmonic Distortion <sup>(2)</sup>	$V_{IN} = 5\text{Vp-p}$ at 10kHz		-78	-72		-80	-76	dB
Signal-to-(Noise + Distortion)	$V_{IN} = 5\text{Vp-p}$ at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	$V_{IN} = 5\text{Vp-p}$ at 10kHz	72	79		76	81		dB
Channel-to-Channel Isolation	$V_{IN} = 5\text{Vp-p}$ at 50kHz		120			*		dB
<b>REFERENCE INPUT</b>								
Range	DCLK Static	0.1		$+V_{CC}$	*		*	V
Resistance			5			*		$\text{G}\Omega$
Input Current	$f_{SAMPLE} = 12.5\text{kHz}$		40	100		*	*	$\mu\text{A}$
	DCLK Static		2.5	3		*	*	$\mu\text{A}$
			0.001			*	*	$\mu\text{A}$
<b>DIGITAL INPUT/OUTPUT</b>								
Logic Family			CMOS			*		
Logic Levels								
$V_{IH}$	$ I_{IH}  \leq +5\mu\text{A}$	3.0		5.5	*		*	V
$V_{IL}$	$ I_{IL}  \leq +5\mu\text{A}$	-0.3		+0.8	*		*	V
$V_{OH}$	$I_{OH} = -250\mu\text{A}$	3.5			*		*	V
$V_{OL}$	$I_{OL} = 250\mu\text{A}$			0.4			*	V
Data Format				Straight Binary		*		
<b>POWER SUPPLY REQUIREMENTS</b>								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			550	900			*	$\mu\text{A}$
	$f_{SAMPLE} = 12.5\text{kHz}$		300			*		$\mu\text{A}$
	Power-Down Mode <sup>(3)</sup> , $\overline{CS} = +V_{CC}$			3			*	$\mu\text{A}$
Power Dissipation				4.5			*	mW
<b>TEMPERATURE RANGE</b>								
Specified Performance		-40		+85	*		*	$^{\circ}\text{C}$

\* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With  $V_{REF}$  equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode ( $PD1 = PD0 = 0$ ) active or  $\overline{SHDN} = \text{GND}$ .

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# SPECIFICATION: +2.7V

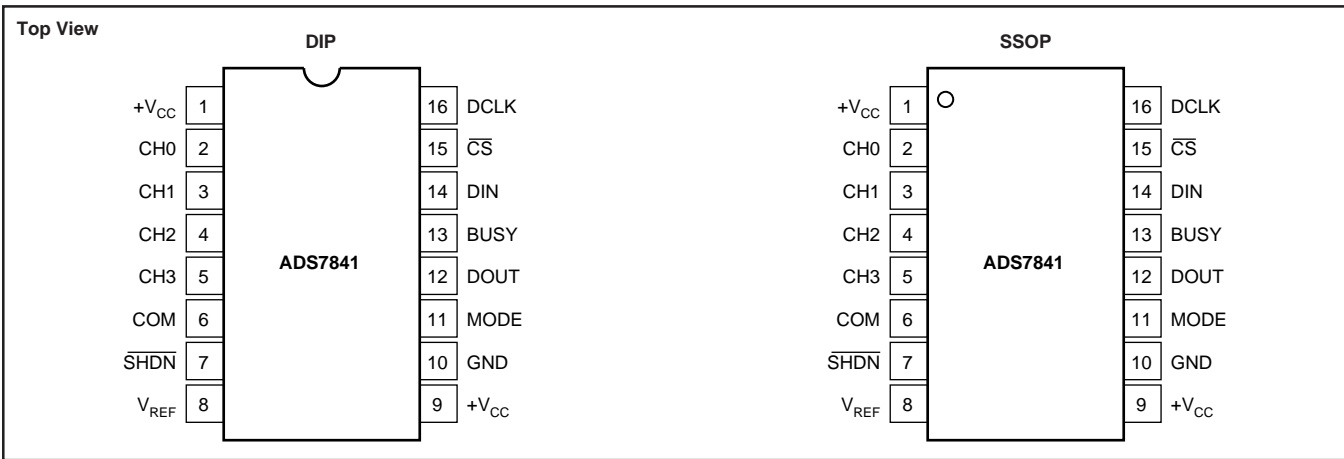
At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+V_{CC} = +2.7\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 125\text{kHz}$ , and  $f_{CLK} = 16 \cdot f_{SAMPLE} = 2\text{MHz}$ , unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ANALOG INPUT</b>								
Full-Scale Input Span	Positive Input - Negative Input	0		$V_{REF}$	*		*	V
Absolute Input Range	Positive Input	-0.2		$+V_{CC} + 0.2$	*		*	V
	Negative Input	-0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			$\pm 1$			*		$\mu\text{A}$
<b>SYSTEM PERFORMANCE</b>								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				$\pm 2$			$\pm 1$	LSB <sup>(1)</sup>
Differential Linearity Error			$\pm 0.8$			$\pm 0.5$	$\pm 1$	LSB
Offset Error				$\pm 3$			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				$\pm 4$			$\pm 3$	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		$\mu\text{V}_{rms}$
Power Supply Rejection			70			*		dB
<b>SAMPLING DYNAMICS</b>								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
<b>DYNAMIC CHARACTERISTICS</b>								
Total Harmonic Distortion <sup>(2)</sup>	$V_{IN} = 2.5\text{Vp-p}$ at 10kHz		-77	-72		-79	-76	dB
Signal-to-(Noise + Distortion)	$V_{IN} = 2.5\text{Vp-p}$ at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	$V_{IN} = 2.5\text{Vp-p}$ at 10kHz	72	78		76	80		dB
Channel-to-Channel Isolation	$V_{IN} = 2.5\text{Vp-p}$ at 50kHz		100			*		dB
<b>REFERENCE INPUT</b>								
Range	DCLK Static	0.1		$+V_{CC}$	*		*	V
Resistance			5			*		$\text{G}\Omega$
Input Current	$f_{SAMPLE} = 12.5\text{kHz}$ DCLK Static		13	40		*	*	$\mu\text{A}$
			2.5			*	*	$\mu\text{A}$
			0.001	3		*	*	$\mu\text{A}$
<b>DIGITAL INPUT/OUTPUT</b>								
Logic Family			CMOS			*		
Logic Levels								
$V_{IH}$	$ I_{IH}  \leq +5\mu\text{A}$	$+V_{CC} \cdot 0.7$		5.5	*		*	V
$V_{IL}$	$ I_{IL}  \leq +5\mu\text{A}$	-0.3		+0.8	*		*	V
$V_{OH}$	$I_{OH} = -250\mu\text{A}$	$+V_{CC} \cdot 0.8$			*		*	V
$V_{OL}$	$I_{OL} = 250\mu\text{A}$			0.4			*	V
Data Format				Straight Binary		*		
<b>POWER SUPPLY REQUIREMENTS</b>								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	$\mu\text{A}$
	$f_{SAMPLE} = 12.5\text{kHz}$		220			*	*	$\mu\text{A}$
	Power-Down Mode <sup>(3)</sup> , $\overline{CS} = +V_{CC}$			3			*	$\mu\text{A}$
Power Dissipation				1.8			*	mW
<b>TEMPERATURE RANGE</b>								
Specified Performance		-40		+85	*		*	$^{\circ}\text{C}$

\* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With  $V_{REF}$  equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or  $\overline{SHDN} = \text{GND}$ .

## PIN CONFIGURATIONS



## PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	+V <sub>CC</sub>	Power Supply, 2.7V to 5V.
2	CH0	Analog Input Channel 0.
3	CH1	Analog Input Channel 1.
4	CH2	Analog Input Channel 2.
5	CH3	Analog Input Channel 3.
6	COM	Ground Reference for Analog Inputs. Sets zero code voltage in single-ended mode. Connect this pin to ground or ground reference point.
7	$\overline{\text{SHDN}}$	Shutdown. When LOW, the device enters a very low power shutdown mode.
8	V <sub>REF</sub>	Voltage Reference Input
9	+V <sub>CC</sub>	Power Supply, 2.7V to 5V.
10	GND	Ground
11	MODE	Conversion Mode. When LOW, the device always performs a 12-bit conversion. When HIGH, the resolution is set by the MODE bit in the CONTROL byte.
12	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{\text{CS}}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{\text{CS}}$ is HIGH.
14	DIN	Serial Data Input. If $\overline{\text{CS}}$ is LOW, data is latched on rising edge of DCLK.
15	$\overline{\text{CS}}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
16	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

+V <sub>CC</sub> to GND	−0.3V to +6V
Analog Inputs to GND	−0.3V to +V <sub>CC</sub> + 0.3V
Digital Inputs to GND	−0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	ORDERING NUMBER <sup>(2)</sup>	TRANSPORT MEDIA
ADS7841E	±2	68	−40°C to +85°C	16-Lead SSOP	322	ADS7841E	Rails
"	"	"	"	"	"	ADS7841E/2K5	Tape and Reel
ADS7841P	±2	68	−40°C to +85°C	16-Pin PDIP	180	ADS7841P	Rails
ADS7841EB	±1	70	−40°C to +85°C	16-Lead SSOP	322	ADS7841EB	Rails
"	"	"	"	"	"	ADS7841EB/2K5	Tape and Reel
ADS7841PB	±1	70	−40°C to +85°C	16-Pin PDIP	180	ADS7841PB	Rails

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of “ADS7841/2K5” will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.



ADS7841



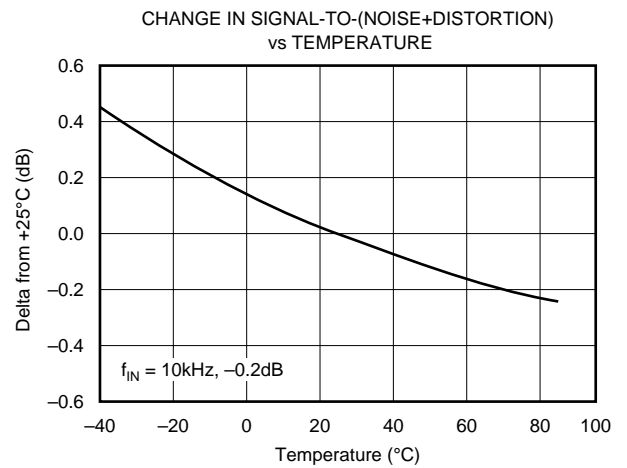
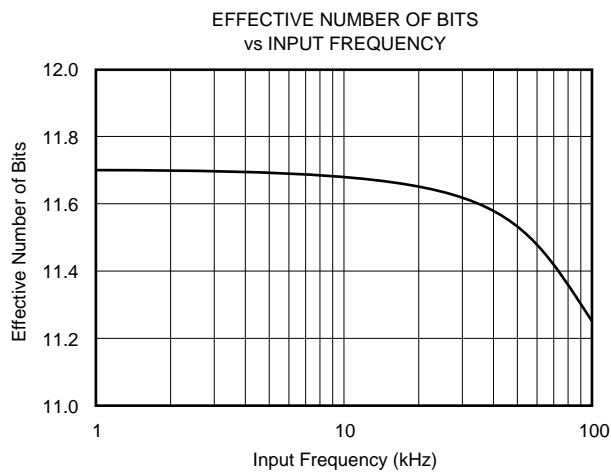
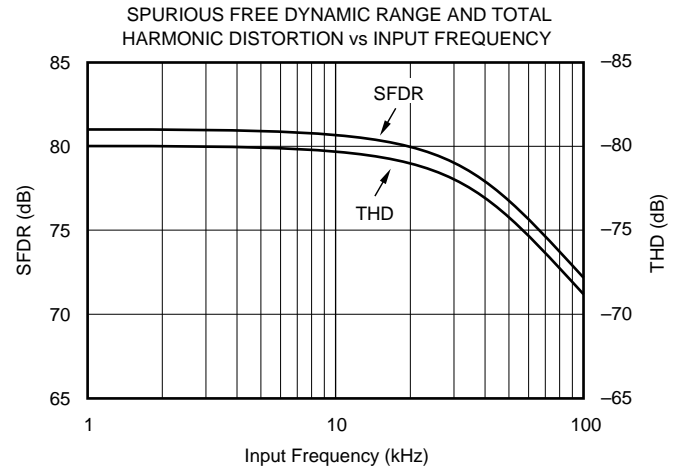
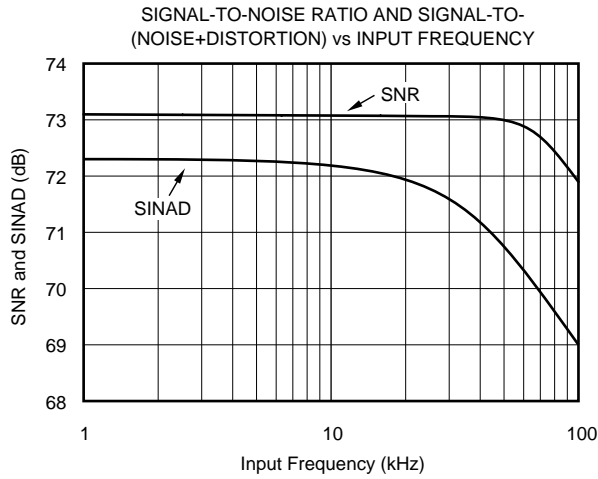
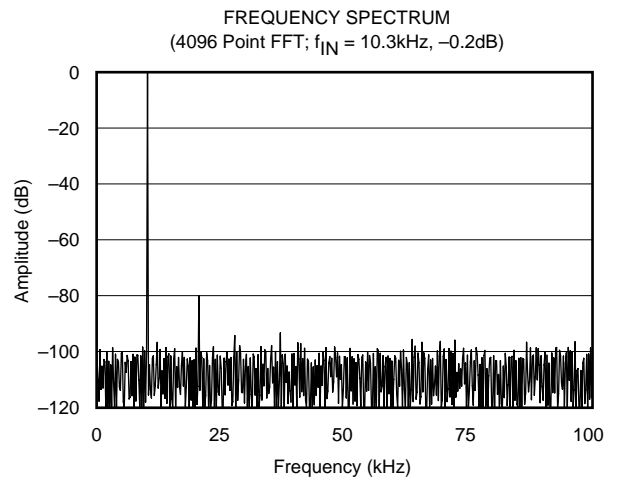
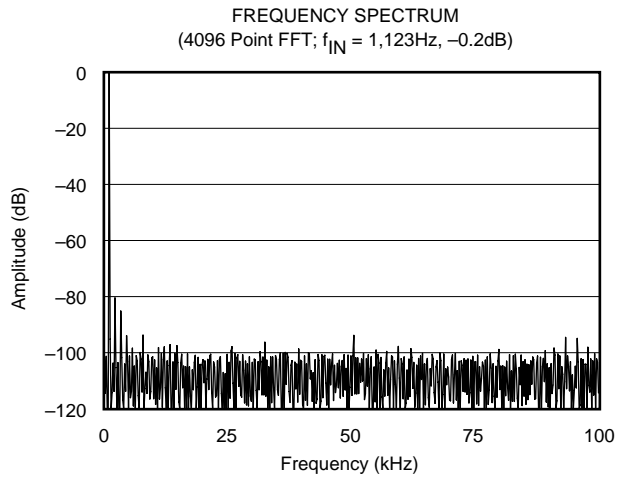
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

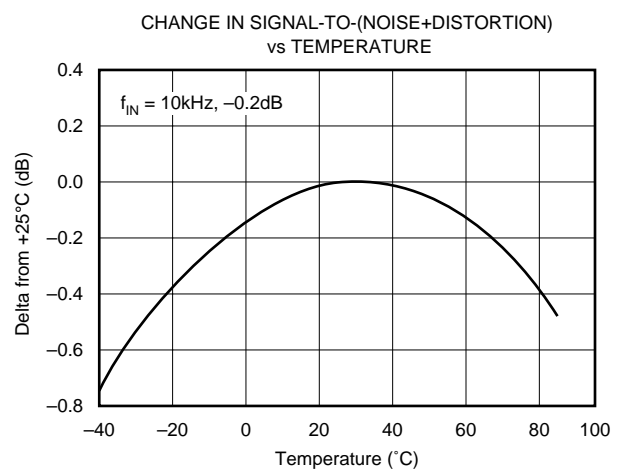
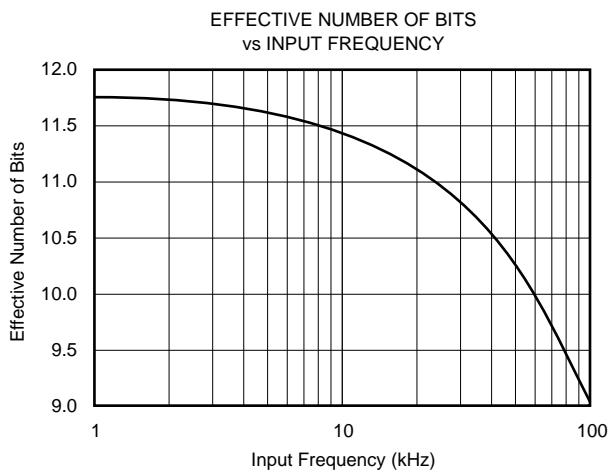
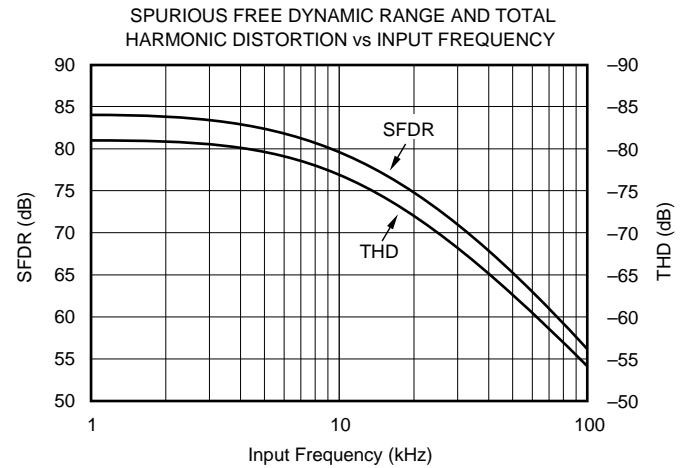
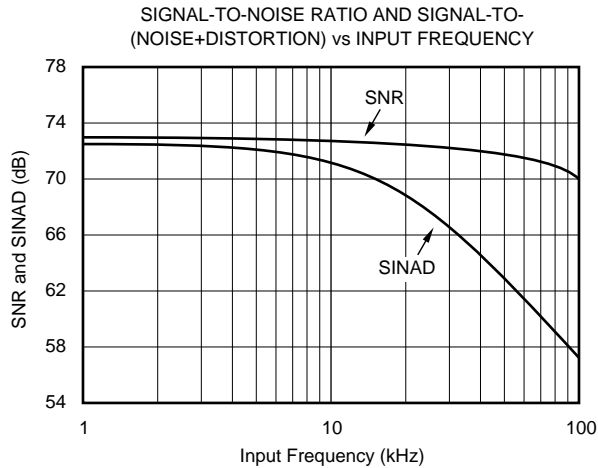
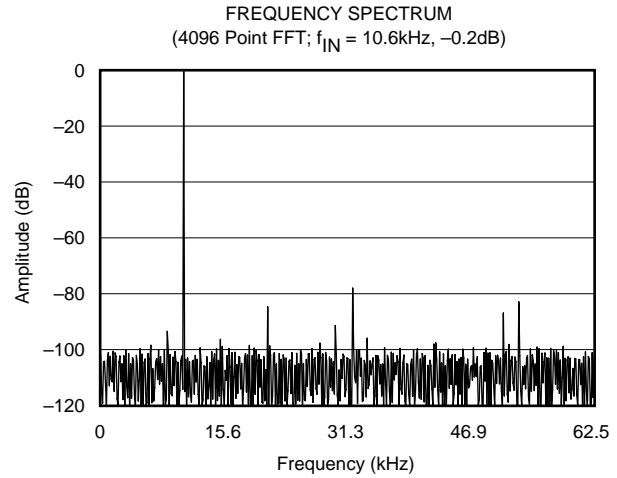
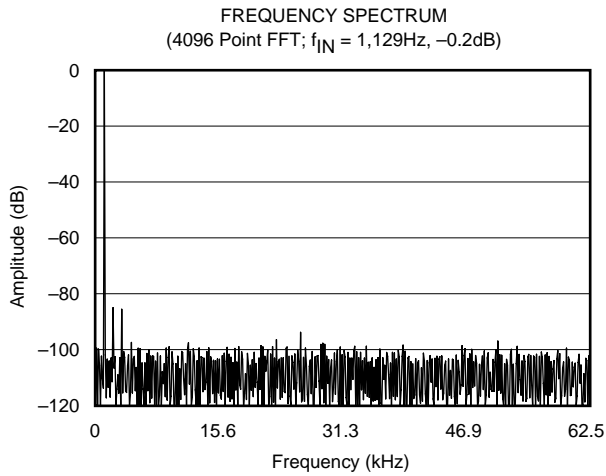
# TYPICAL PERFORMANCE CURVES: +5V

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $V_{REF} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 200\text{kHz}$ , and  $f_{\text{CLK}} = 16 \cdot f_{\text{SAMPLE}} = 3.2\text{MHz}$ , unless otherwise noted.



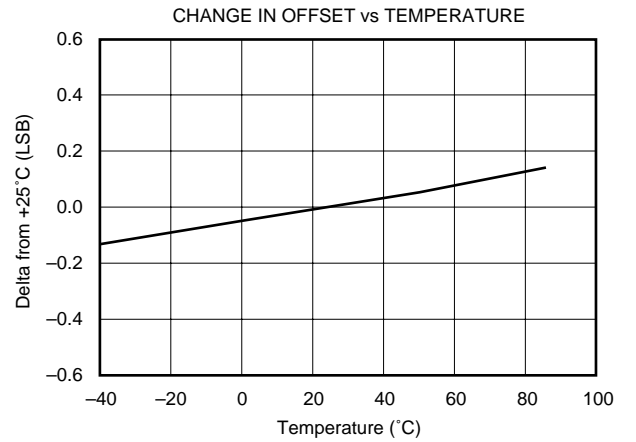
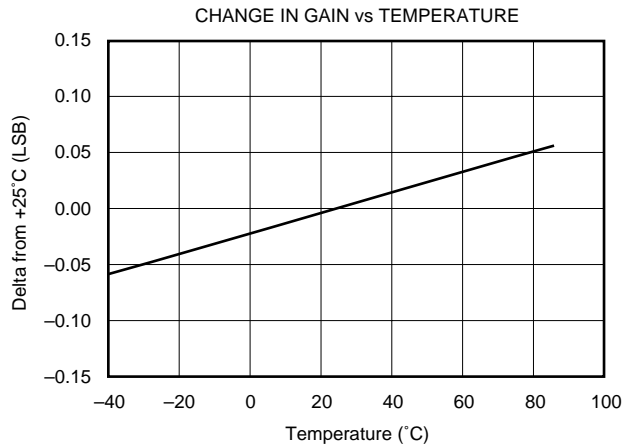
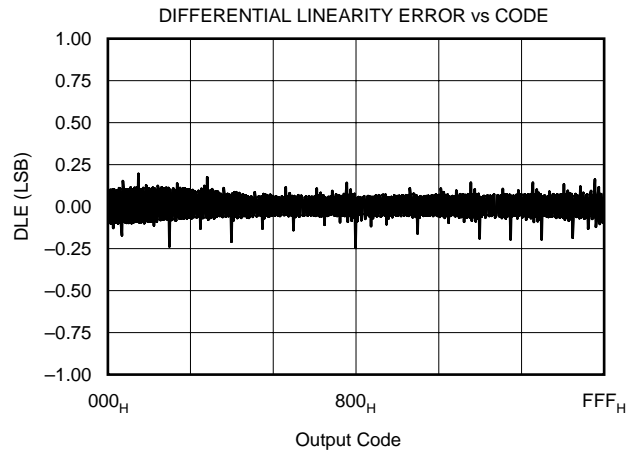
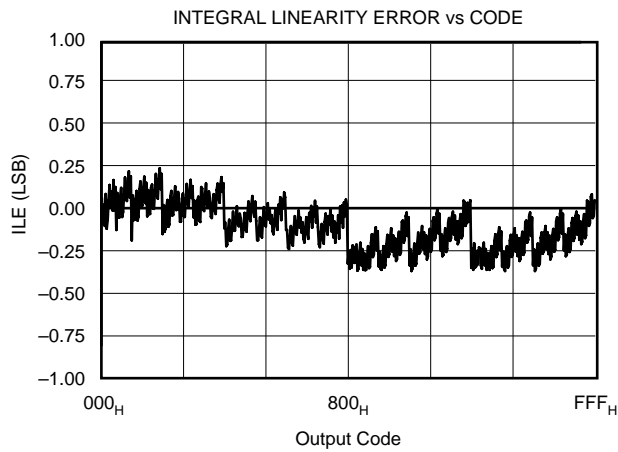
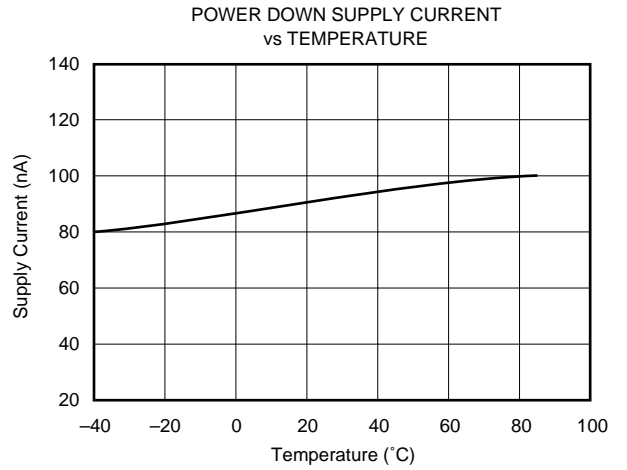
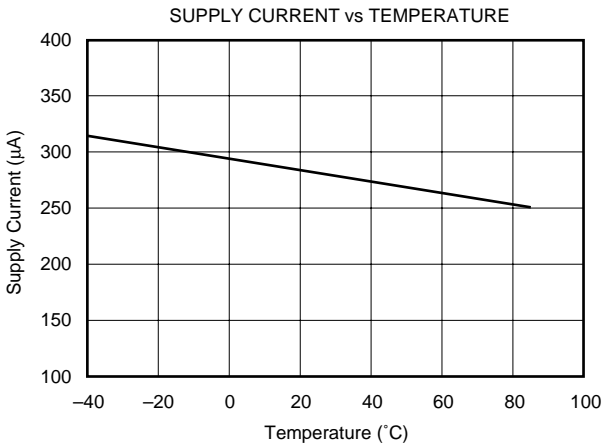
# TYPICAL PERFORMANCE CURVES: +2.7V

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +2.7\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{\text{SAMPLE}} = 125\text{kHz}$ , and  $f_{\text{CLK}} = 16 \cdot f_{\text{SAMPLE}} = 2\text{MHz}$ , unless otherwise noted.



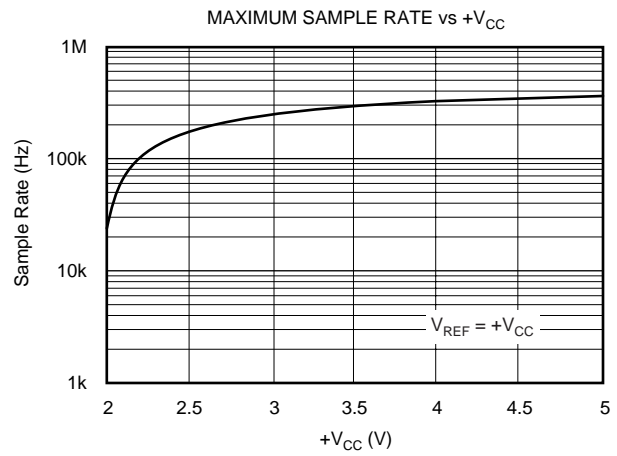
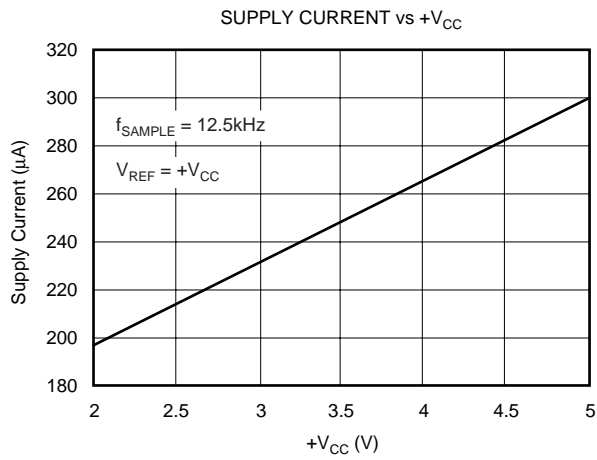
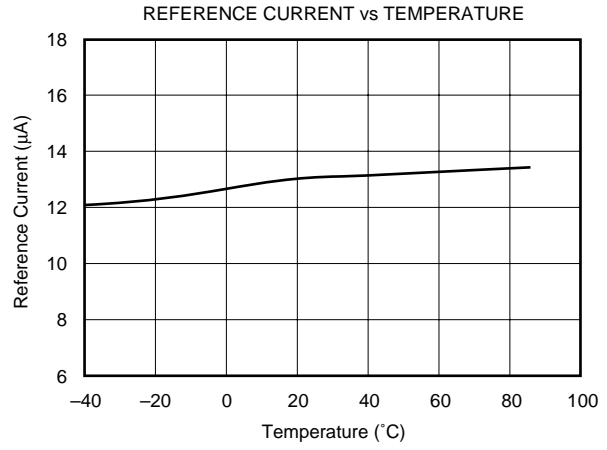
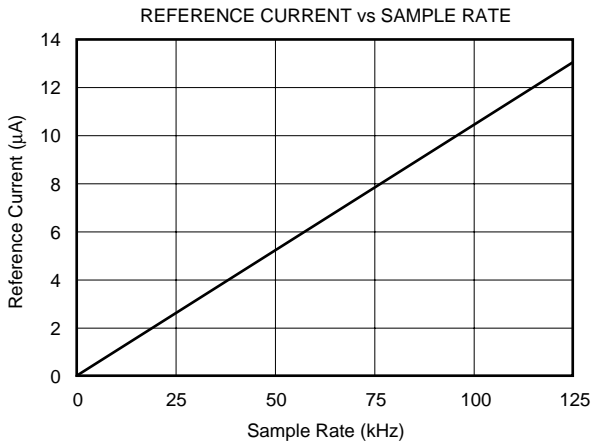
# TYPICAL PERFORMANCE CURVES: +2.7V (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +2.7\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 125\text{kHz}$ , and  $f_{CLK} = 16 \cdot f_{SAMPLE} = 2\text{MHz}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +2.7\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 125\text{kHz}$ , and  $f_{CLK} = 16 \cdot f_{SAMPLE} = 2\text{MHz}$ , unless otherwise noted.





# THEORY OF OPERATION

The ADS7841 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6μs CMOS process.

The basic operation of the ADS7841 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and +V<sub>CC</sub>. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7841.

The analog input to the converter is differential and is provided via a four-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using two of the four input channels (CH0 - CH3). The particular configuration is selectable via the digital interface.

## ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the ADS7841. The differential input of the converter is derived from one of the four inputs in reference to the COM pin or two of the four inputs. Table I and Table II show the relationship between the A2, A1, A0, and SGL/DIF control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and -IN inputs (see Figure 2) is captured on the internal capacitor array. The voltage on the -IN input is limited between -0.2V and 1.25V, allowing the input to reject small signals which are common to both the +IN and -IN input. The +IN input has a range of -0.2V to +V<sub>CC</sub> + 0.2V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN				-IN
1	0	1		+IN			-IN
0	1	0			+IN		-IN
1	1	0				+IN	-IN

TABLE I. Single-Ended Channel Selection (SGL/DIF HIGH).

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN	-IN			
1	0	1	-IN	+IN			
0	1	0			+IN	-IN	
1	1	0			-IN	+IN	

TABLE II. Differential Channel Control (SGL/DIF LOW).

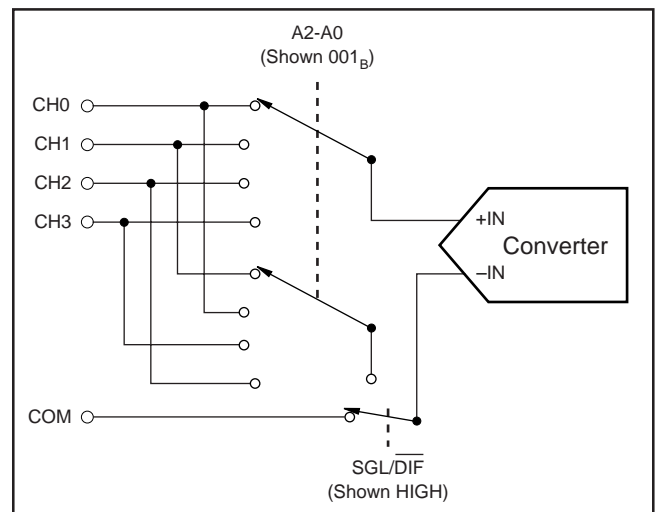


FIGURE 2. Simplified Diagram of the Analog Input.

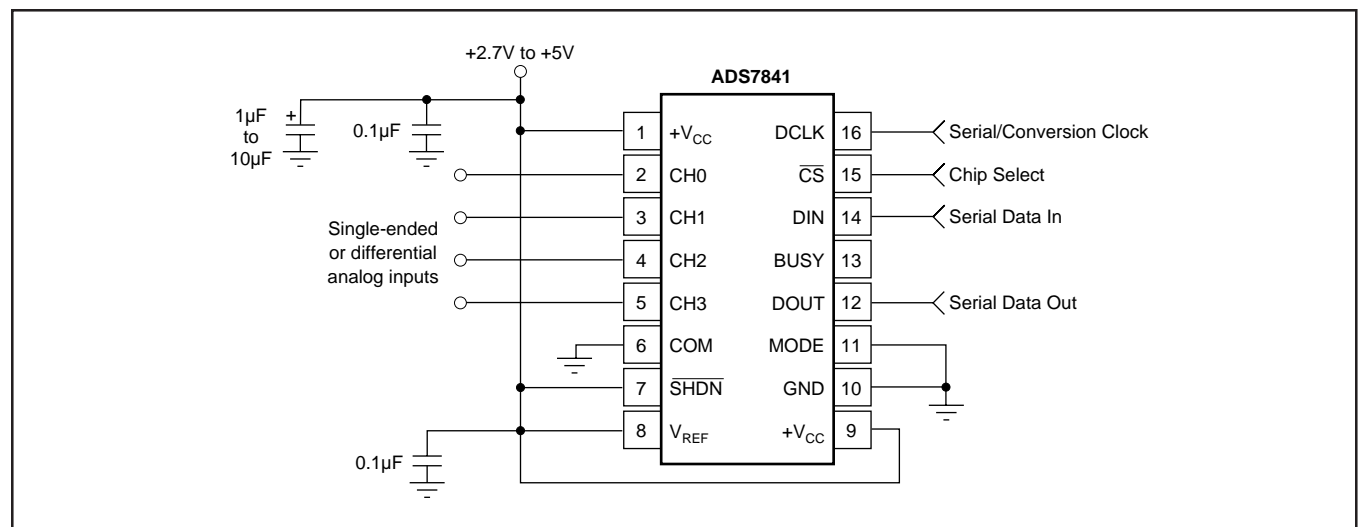


FIGURE 1. Basic Operation of the ADS7841.

## REFERENCE INPUT

The external reference sets the analog input range. The ADS7841 will operate with a reference in the range of 100mV to +V<sub>CC</sub>. Keep in mind that the analog input is the difference between the +IN input and the -IN input as shown in Figure 2. For example, in the single-ended mode, a 1.25V reference, and with the COM pin grounded, the selected input channel (CH0 - CH3) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5V reference, then it will typically be 10 LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 1.22mV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 100mV, the LSB size is 24μV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V<sub>REF</sub> input is not buffered and directly drives the capacitor digital-to-analog converter (CDAC) portion of the ADS7841. Typically, the input current is 13μA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

## DIGITAL INTERFACE

Figure 3 shows the typical operation of the ADS7841's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5V, regardless of +V<sub>CC</sub>). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample/hold goes into the hold mode. The next twelve clock cycles accomplish the actual analog-to-digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

## Control Byte

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7841 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2 - A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

The MODE bit and the MODE pin work together to determine the number of bits for a given conversion. If the MODE pin is LOW, the converter always performs a 12-bit conversion regardless of the state of the MODE bit. If the MODE pin is HIGH, then the MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SGL/DIF	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6 - 4	A2 - A0	Channel Select Bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input as detailed in Tables I and II.
3	MODE	12-Bit/8-Bit Conversion Select Bit. If the MODE pin is HIGH, this bit controls the number of bits for the next conversion: 12-bits (LOW) or 8-bits (HIGH). If the MODE pin is LOW, this bit has no function and the conversion is always 12 bits.
2	SGL/DIF	Single-Ended/Differential Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input as detailed in Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

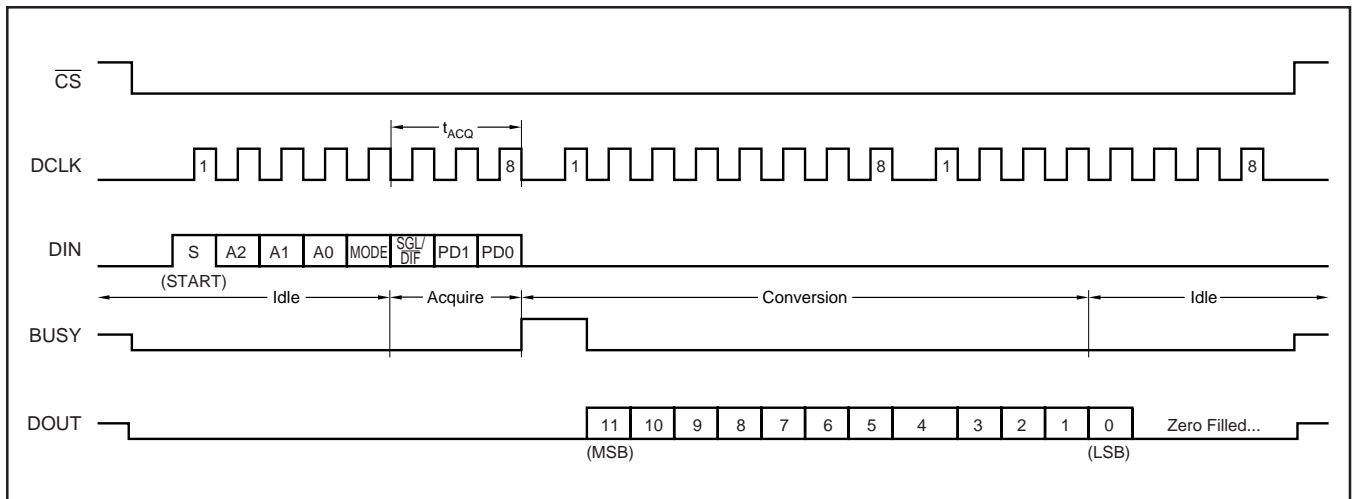


FIGURE 3. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

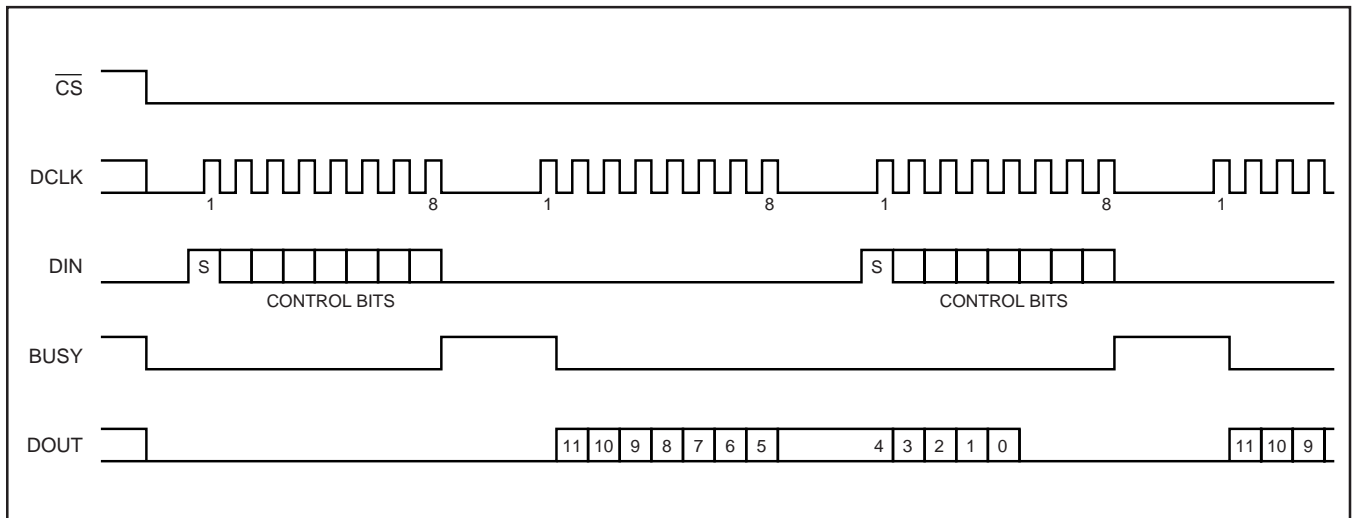


FIGURE 4. Conversion Timing, 16-Clocks per Conversion, 8-bit Bus Interface. No DCLK delay required with dedicated serial port.

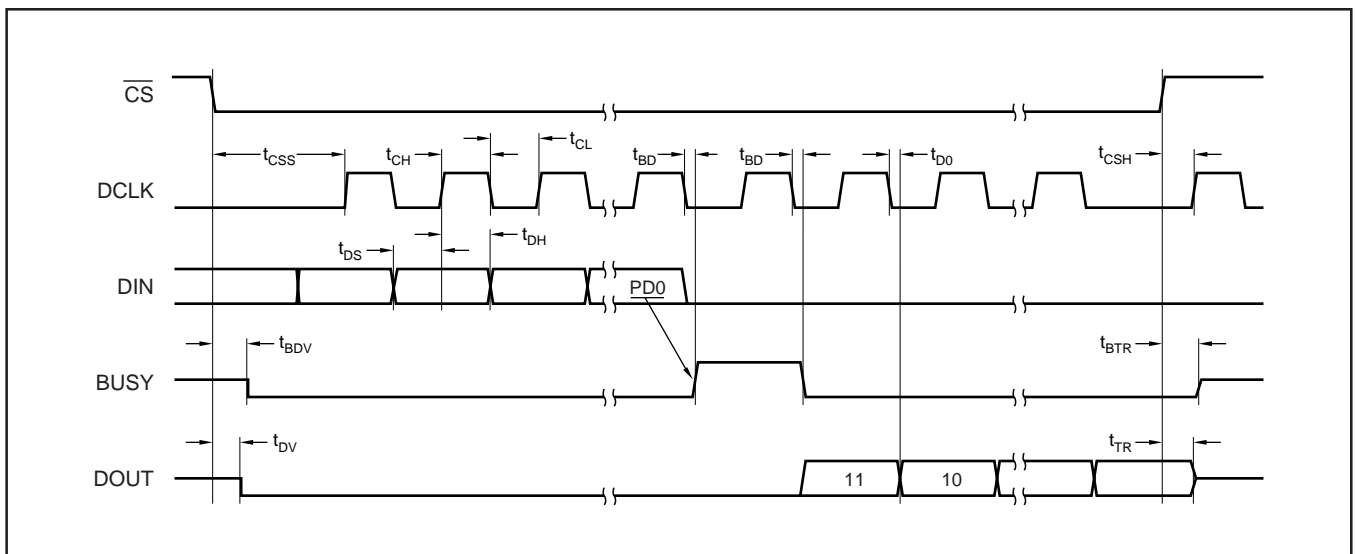


FIGURE 5. Detailed Timing Diagram.

The SGL/DIF bit controls the multiplexer input mode: either single-ended (HIGH) or differential (LOW). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Tables I and II and Figure 2 for more information. The last two bits (PD1 - PD0) select the power-down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

### 16-Clocks per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample/hold may droop enough to affect the conversion result. In addition, the ADS7841 is fully powered while other serial communications are taking place.

### Digital Timing

Figure 5 and Tables VI and VII provide detailed timing for the digital interface of the ADS7841.

### 15-Clocks per Conversion

Figure 6 provides the fastest way to clock the ADS7841. This method will not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

PD1	PD0	Description
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
0	1	Reserved for future use.
1	0	Reserved for future use.
1	1	No power-down between conversions, device always powered.

TABLE V. Power-Down Selection.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t <sub>ACQ</sub>	Acquisition Time	1.5			μs
t <sub>DS</sub>	DIN Valid Prior to DCLK Rising	100			ns
t <sub>DH</sub>	DIN Hold After DCLK HIGH	10			ns
t <sub>DO</sub>	DCLK Falling to DOUT Valid			200	ns
t <sub>DV</sub>	CS Falling to DOUT Enabled			200	ns
t <sub>TR</sub>	CS Rising to DOUT Disabled			200	ns
t <sub>CSS</sub>	CS Falling to First DCLK Rising	100			ns
t <sub>CSH</sub>	CS Rising to DCLK Ignored	0			ns
t <sub>CH</sub>	DCLK HIGH	200			ns
t <sub>CL</sub>	DCLK LOW	200			ns
t <sub>BD</sub>	DCLK Falling to BUSY Rising			200	ns
t <sub>BDV</sub>	CS Falling to BUSY Enabled			200	ns
t <sub>BTR</sub>	CS Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications (+V<sub>CC</sub> = +2.7V to 3.6V, T<sub>A</sub> = -40°C to +85°C, C<sub>LOAD</sub> = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t <sub>ACQ</sub>	Acquisition Time	900			ns
t <sub>DS</sub>	DIN Valid Prior to DCLK Rising	50			ns
t <sub>DH</sub>	DIN Hold After DCLK HIGH	10			ns
t <sub>DO</sub>	DCLK Falling to DOUT Valid			100	ns
t <sub>DV</sub>	CS Falling to DOUT Enabled			70	ns
t <sub>TR</sub>	CS Rising to DOUT Disabled			70	ns
t <sub>CSS</sub>	CS Falling to First DCLK Rising	50			ns
t <sub>CSH</sub>	CS Rising to DCLK Ignored	0			ns
t <sub>CH</sub>	DCLK HIGH	150			ns
t <sub>CL</sub>	DCLK LOW	150			ns
t <sub>BD</sub>	DCLK Falling to BUSY Rising			100	ns
t <sub>BDV</sub>	CS Falling to BUSY Enabled			70	ns
t <sub>BTR</sub>	CS Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications (+V<sub>CC</sub> = +4.75V to +5.25V, T<sub>A</sub> = -40°C to +85°C, C<sub>LOAD</sub> = 50pF).

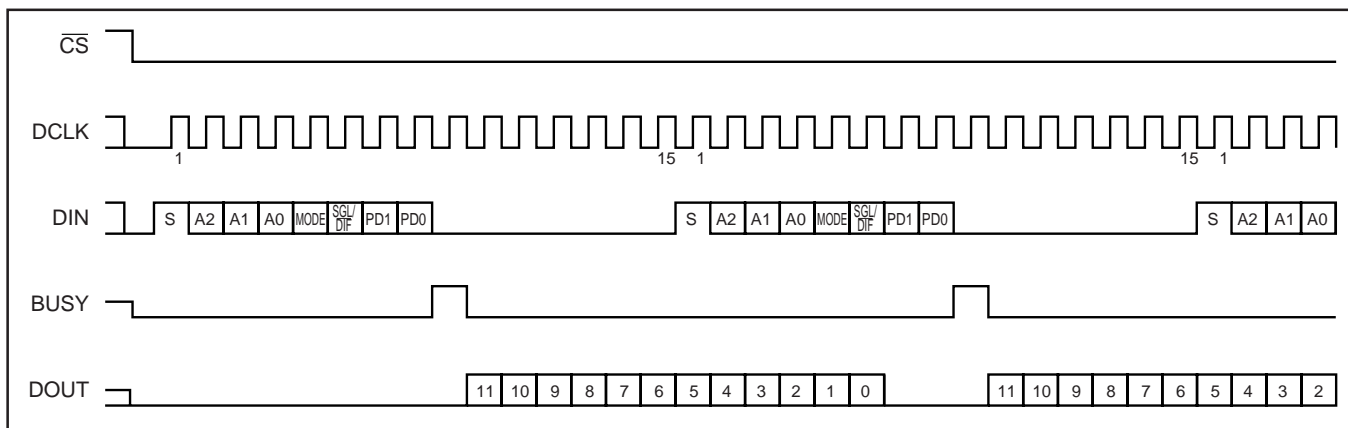


FIGURE 6. Maximum Conversion Rate, 15-Clocks per Conversion.

## Data Format

The ADS7841 output data is in straight binary format as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

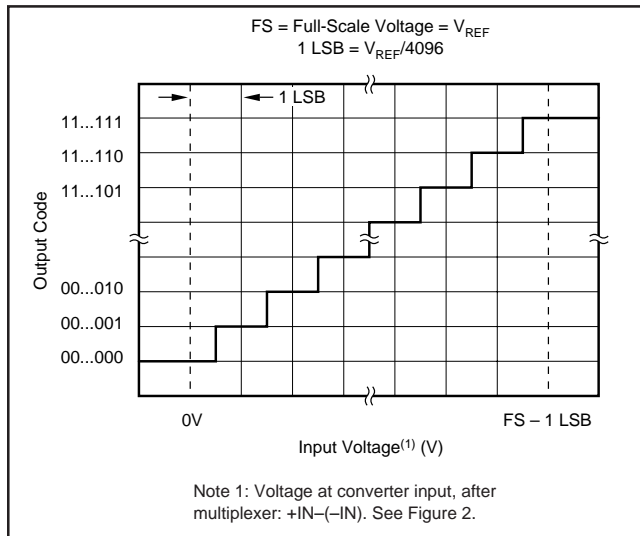


FIGURE 7. Ideal Input Voltages and Output Codes.

## 8-Bit Conversion

The ADS7841 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide a 12-bit transfer or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7841 is not as critical, settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

## POWER DISSIPATION

There are three power modes for the ADS7841: full power (PD1 - PD0 = 11B), auto power-down (PD1 - PD0 = 00B), and shutdown (SHDN LOW). The affects of these modes varies depending on how the ADS7841 is being operated. For example, at full conversion rate and 16 clocks per conversion, there is very little difference between full power mode and auto power-down. Likewise, if the device has entered auto power-down, a shutdown (SHDN LOW) will not lower power dissipation.

When operating at full-speed and 16-clocks per conversion (as shown in Figure 4), the ADS7841 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes

remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversion are simply done less often, then the difference between the two modes is dramatic. Figure 8 shows the difference between reducing the DCLK frequency (“scaling” DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversion per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and  $\overline{CS}$  is LOW while the ADS7841 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping  $\overline{CS}$  HIGH. The differences in supply current for these two cases are shown in Figure 9.

Operating the ADS7841 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time “penalty” on power-up. The very first conversion will be valid. SHDN can be used to force an immediate power-down.

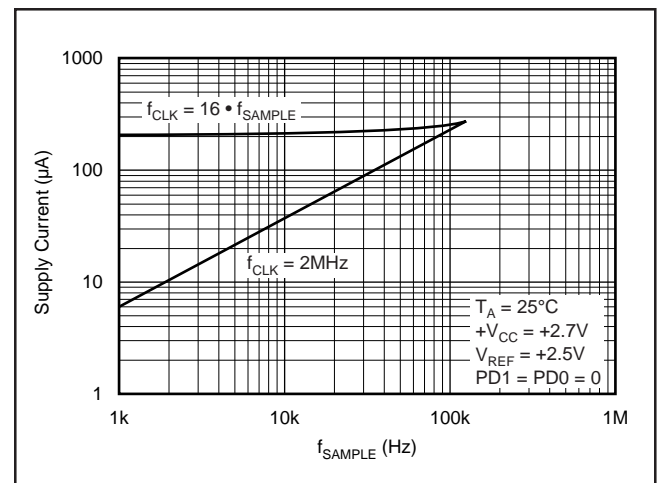


FIGURE 8. Supply Current vs Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

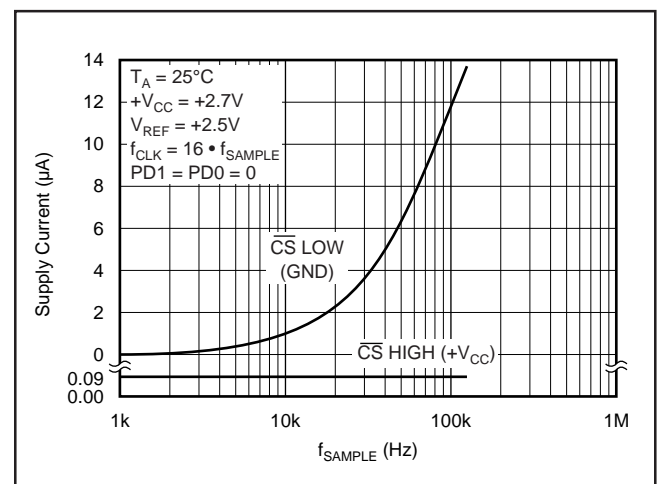


FIGURE 9. Supply Current vs State of  $\overline{CS}$ .

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7841 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7841 should be clean and well bypassed. A 0.1 $\mu$ F ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor and a 5 $\Omega$  or 10 $\Omega$  series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1 $\mu$ F capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7841 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7841 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.