GM3842A,GM3843A,GM3844A,GM3845A

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLERS

- **Low Start-Up and Operating Current**
- **Automatic Feed Forward Compensation**
- **Current Mode Operating Frequency up to 500kHz**
- **Trimmed Oscillator Discharge Current for Precise Duty Cycle Control**
- **Latching PWM for Cycle-By-Cycle Current Limiting**
- **Undervoltage Lockout with Hysteresis**
- **High Current Totem Pole Output**

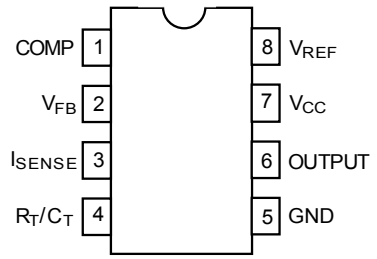
The GM384xA series of high performance fixed-frequency current mode PWM controllers are designed for off–Line and DC–to–DC converter applications. They require minimal external components to precisely tailor performance in a wide variety of applications.

These GM384xA's incluide a trimmed oscillator for precise duty cycle control, a temperature-compensated reference, high gain error amplifier, a current-sensing comparator, and a high-current totem pole output for driving a power MOSFET.

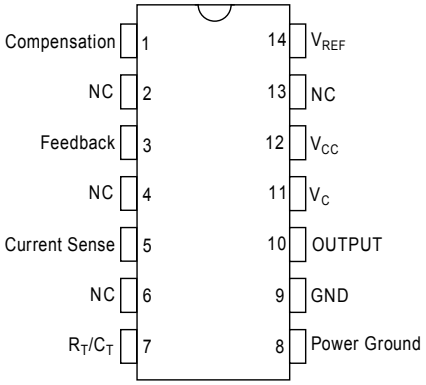
On-chip protection features include undervoltage lockouts with hysteresis for both input and reference, cycle–by–cycle current limiting, programmable output deadtime, and a latch for single pulse metering. All this in a simple DIP-8 or SOP-8 package!

GM3842A and GM3844A have UVLO thresholds of 16V (on)/10V(off); GM3843A and GM3845A have UVLO thresholds of 8.4V (on)/7.6V (off). GM3842A and GM3843A operate within 100% duty cycle; GM3844A and GM3845A operate within 50% duty cycle.

PIN CONNECTIONS

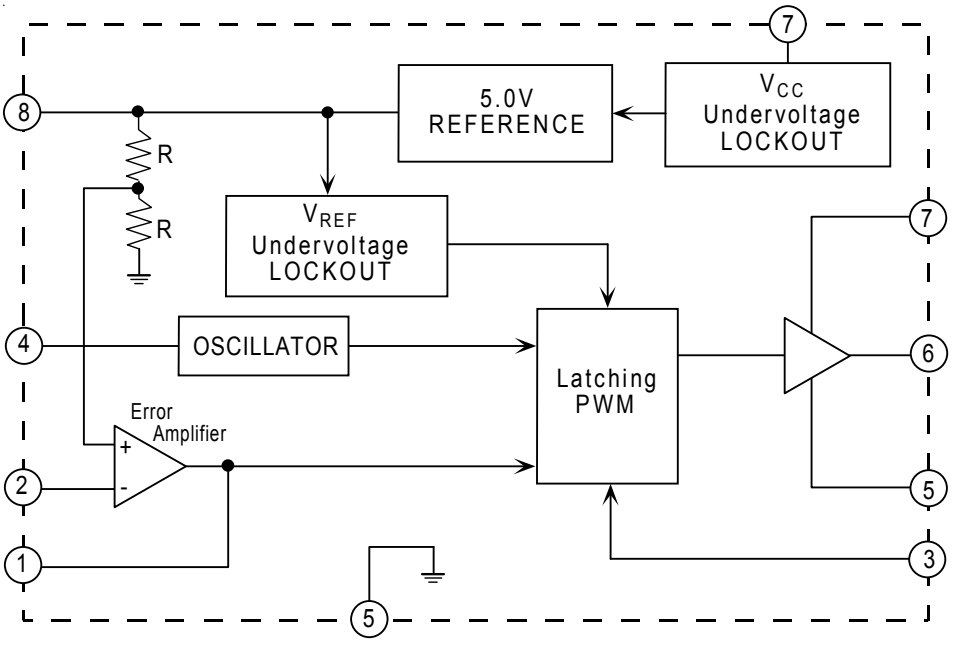


DIP-8, SOP-8 (TOP VIEW)



SOP-14 (TOP VIEW)

SIMPLIFIED BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage (low impedance source)	V_{CC}	30	V
Output Current, Source or Sink *	I_O	±1.0	mA
Input Voltage (analog inputs pins 2,3)	V_I	-0.3 to +5.5	V
Maximum Power Dissipation (T_A=25°C)	P_D	1.0	W
Error Amp Output Sink Current	$I_{SINK(E.A)}$	10	mA
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (soldering 5 sec.)	T_L	260	°C

* Note: Maximum Package Power Dissipation Limits must be observed.

■ PIN FUNCTIONS DESCRIPTION

PIN	FUNCTION	DESCRIPTION
1	COMP	This pin is Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	GND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control integrated circuit (IC).
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

■ ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70° C, *V_{CC}=15V, C_T=3.3nF, R_T=10kΩ, unless otherwise specified)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Reference Output Voltage	V_{REF}	T_J=25°C, I_{REF}=1mA	4.9	5.0	5.1	V
Line Regulation	ΔV_{REF}	12V ≤ V_{CC} ≤ 25V		6.0	20	mV
Load Regulation	ΔV_{REF}	1mA ≤ I_{REF} ≤ 20mA		6.0	25	mV
Short Circuit Output Current	I_{SC}	T_A=25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T_J=25°C	47	52	57	kHz
Frequency Change with Voltage	$\Delta f / \Delta V_{CC}$	12V ≤ V_{CC} ≤ 25V		0.05	1.0	%
Oscillator Amplitude	$V_{(OSC)}$	(peak to peak)		1.6		V
Error Amplifier Section						
Input Bias Current	I_{BIAS}	V_{FB} = 3V		-0.1	-2.0	μA
Input Voltage	$V_{I(E.A)}$	V_{PIN1} = 2.5V		2.5	2.58	V
Open Loop Voltage Gain	A_{VOL}	2V ≤ V_O ≤ 4V	65	90		dB
Power Supply Rejection Ratio	PSRP	12V ≤ V_{CC} ≤ 25V	60	70		dB
Output Sink Current	I_{SINK}	V_{PIN2} = 2.7V, V_{PIN1} = 1.1V	2	7		mA
Output Source Current	I_{SOURCE}	V_{PIN2} = 2.3V, V_{PIN1} = 5V	-0.5	-1.0		mA
High Output Voltage	V_{OH}	V_{PIN2} = 2.3V, RL=15k Ω to GND	5.0	6.0		V
Low Output Voltage	V_{OL}	V_{PIN2} = 2.7V, RL=15k Ω to Pin8		0.8	1.1	V
Current Sense Section						
Gain	G_V	(Note 1 and 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_{PIN1} = 5V (Note 1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V_{CC} ≤ 25V (Note1)		70		dB
Input Bias Current	I_{BIAS}	V_{PIN3} = 3V		-3.0	-10	μA
Output Section						
Low Output Voltage	V_{OL}	I_{SINK} = 20 mA		0.08	0.4	V
		I_{SINK} = 200 mA		1.4	2.2	V
High Output Voltage	V_{OH}	I_{SINK} = 20 mA	13	13.5		V
		I_{SINK} = 200 mA	12	13		V
Rise Time	t_R	T_J=25°C, C_L = 1nF (Note 3)		45	150	nS
Fall Time	t_F	T_J=25°C, C_L = 1nF (Note 3)		35	150	nS
Undervoltage Lockout Section						
Start Threshold	$V_{TH(ST)}$	GM3842A, GM3844A	14.5	16.0	17.5	V
		GM3843A, GM3845A	7.8	8.4	9.0	V
Minimum Operating Voltage (after turn ON)	$V_{OPR(MIN)}$	GM3842A, GM3844A	8.5	10	11.5	V
		GM3843A, GM3845A	7.0	7.6	8.2	V
PWM Section						
Maximum Duty Cycle	$D_{(MAX)}$	GM3842A, GM3843A	95	97	100	%
		GM3844A, GM3845A	47	48	50	%
Minimum Duty Cycle	$D_{(MIN)}$				0	%
Total Standby Current						
Start-Up Current	I_{ST}			0.17	0.3	mA
Operating Supply Current	$I_{CC(OPR)}$	V_{PIN3} = V_{PIN2} = 0V		13	17	mA
Zener Voltage	V_Z	I_{CC} = 25 mA	30	38		V

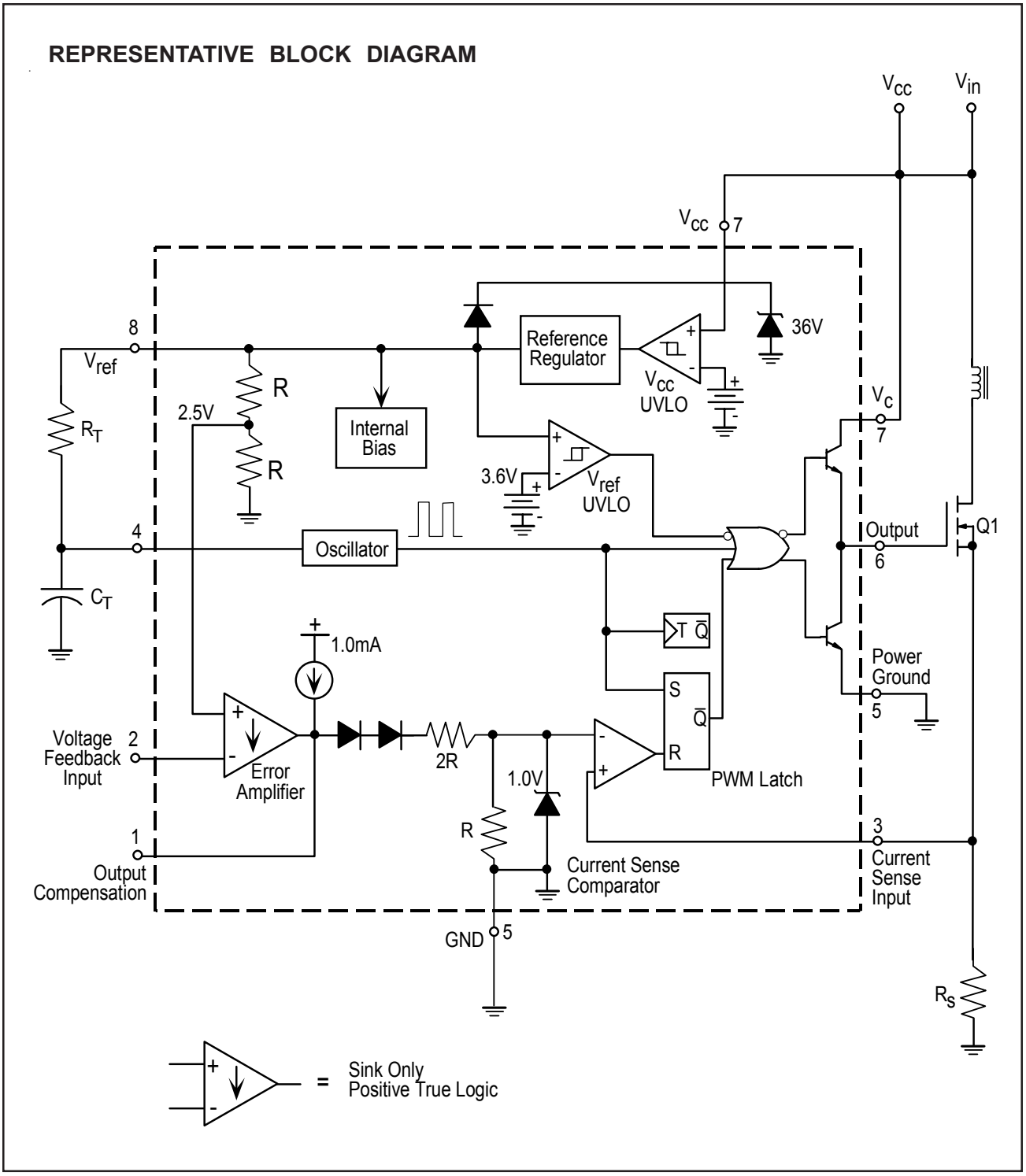
* Adjust Vcc above the Startup threshold before setting to 15 V.

Note1: Parameter measured at trip point of latch with V_{PIN2} = 0.

Note2: Gain defined as A=ΔV_{PIN1} / ΔV_{PIN3} ; 0 ≤ V_{PIN3} ≤ 0.8V

Note3: These parameters, although guaranteed, are not 100% tested in production

REPRESENTATIVE BLOCK DIAGRAM



■ OPERATING DESCRIPTION

The GM3842A, GM3843A, GM3844A and GM3845A are high performance, fixed frequency, current mode controllers. They are designed for off–line and DC–to–DC converter applications offering great versatility with minimal external components. A representative block diagram is shown on page 4.

Oscillator

The oscillator frequency is determined by the values of the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. As C_T discharges, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the output to be in a low state, and produces a controlled amount of output deadtime.

Many different values of R_T and C_T will give the same oscillator frequency, but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature-compensated; discharge current is trimmed and guaranteed to within ±10% at T_J = 25°C. Thiw minimizes variations of oscillator frequency and maximum output duty cycle. In many noise sensitive applications it may be desirable to frequency–lock the converter by applying a clock signal to the circuit shown in Figure 1. For best locking results, set the free–running oscillator frequency to about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 2. You can get very accurate output duty cycle clamping by tweaking the clock waveform..

Error Amplifier

The GM384xA's have a fully compensated error amplifier with access to both the inverting input and output, providing DC voltage gain of 90 dB (typical). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 mA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amplfier Output (Pin 1) allows external loop compensation. The output voltage is offset by the two diode drops (≈1.4 V) and divided by three before connecting to the inverting input of the Current Sense Comparator. This assures that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This happens when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 4, 5). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{F(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The GM384xA's operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). The error signal controls the peak inductor current cycle–by–cycle. The Current Sense Comparator PWM Latch configuration assures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

When the power supply output is overloaded or if output voltage sensing is lost, the chip operation is not normal. In these situations, the Current Sense Comparator threshold will be internally clamped to 1.0 V and the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0V}{R_S}$$

In designing a high power switching regulator you really want to reduce the internal clamp voltage, to keep a reasonable level of power dissipation of R_S. Adjusting the internal clamp voltage is very simple, as shown in Figure 3. The two external diodes compensate the internal diodes so you get a constant clamp voltage over temperature. Avoid too much reduction of the $I_{pk(max)}$ clamp voltage, or you will get noise pickup and erratic results.

A narrow spike on the leading edge of the current waveform often occurs and can cause the power supply instability when the output load is light. This spike is caused by power transformer interwinding capacitance and output rectifier recovery time. You can eliminate this problem by adding an RC filter on the Current Sense Input, with a time constant similar to the spike's duration; see Figure 7.

Undervoltage Lockout

Two UVLO comparators in the GM384xA's assure that the chips are fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) each have separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their thresholds are reached. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the GM3842A and GM3844A, and 8.4V/7.6V for the GM3843A and GM3845A.

The Vref comparator upper and lower thresholds are 3.6V/3.4 V. The large hysteresis and low startup current of the GM3842A and GM3844A makes them ideal for off–line converter applications where efficient bootstrap startup is required.

The GM3843A and GM3845A are intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator form V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the GM3842A and GM3844A is 11V; for the GM3843A and GM3845A it is 8.2V.

Output

The GM384xA's have a single totem pole output stage that was designed for direct drive of power MOSFETs. It provides up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry keeps the output in a sinking mode whenever a UVLO is active. This eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce switching transient noise levels imposed on the control circuitry. This is very useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input gives you added flexibility to tweak the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20V. Figure 6 shows proper power and control ground connections in a current-sensing power MOSFET application.

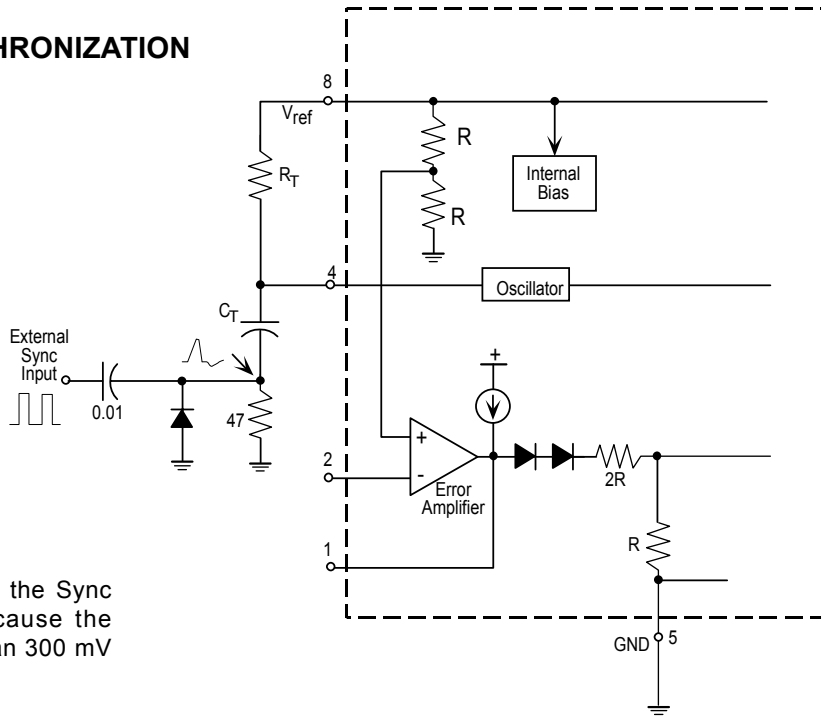
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C on the GM384xA's. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is can provide more than 20mA for powering additional control system circuitry.

Design Considerations

Do not make your converter using wire–wrap or plug–in prototype boards. High-frequency circuit layout techniques must be observed to prevent pulsewidth jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. You can improve noice immunity by lowering circuit impedances at these points. The PCB layout should have a ground plane with low–current signal and high–current switch and output grounds returning on separate paths to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required, depending upon circuit layout, to provide a low impedance path for filtering high frequency noise. All high-current loops should be as short as possible and use heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be placed as close as possible to the GM384xA, and as far as possible from the power switch and other noise-generating components.

Figure 1.
EXTERNAL CLOCK SYNCHRONIZATION



* The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300 mV below ground.

Figure 2.
EXTERNAL DUTY CYCLE CLAMP AND MULTI-UNIT SYNCHRONIZATION

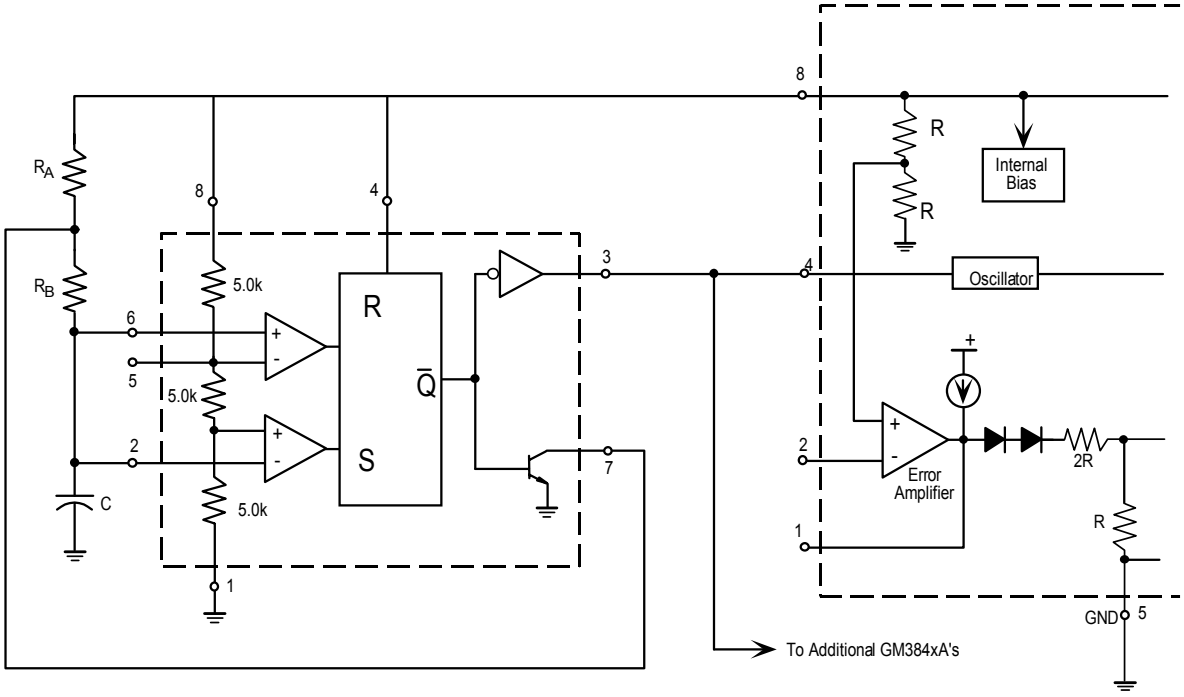


Figure 3.
ADJUSTABLE REDUCTION OF CLAMP LEVEL

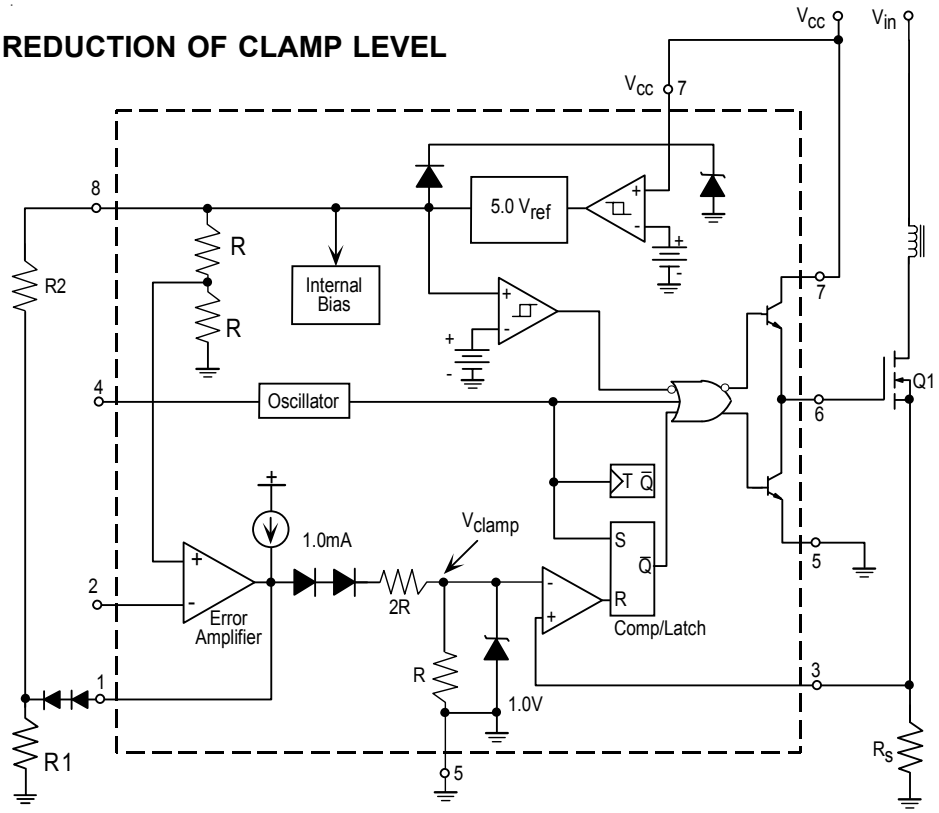
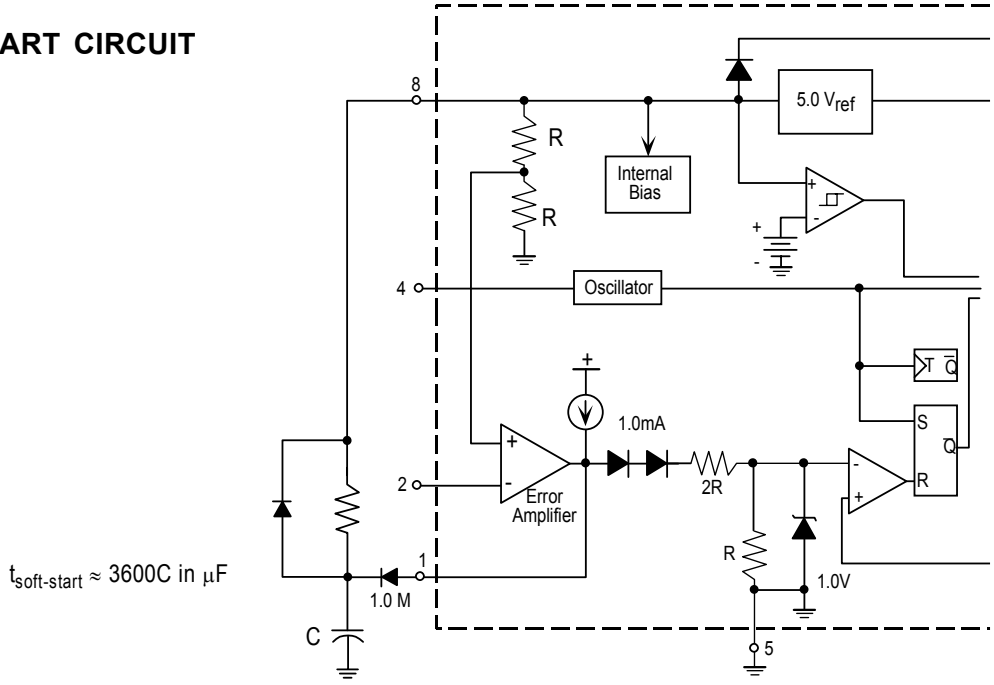


Figure 4.
SOFT-START CIRCUIT



$t_{soft\text{-}start} \approx 3600C$ in μF

Figure 5.
ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

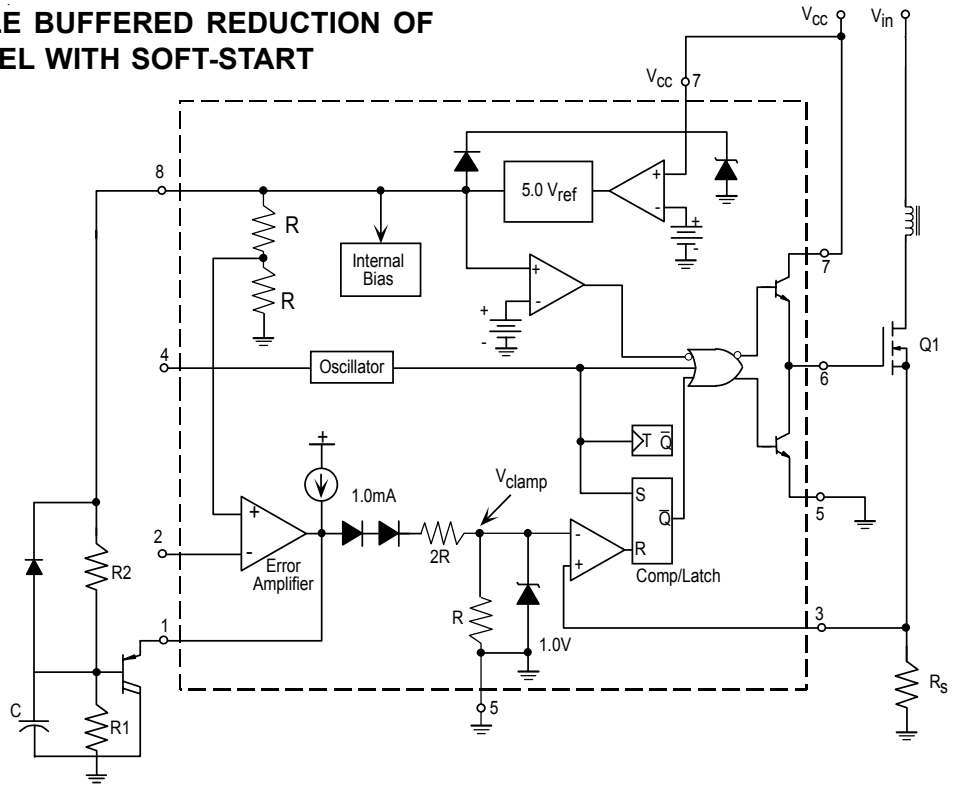


Figure 6.
CURRENT SENSING POWER MOSFET

For proper operation during over current conditions, a reduction of the Ipk(max) clamp level must be implemented. Refer to Figures 3 and 4.

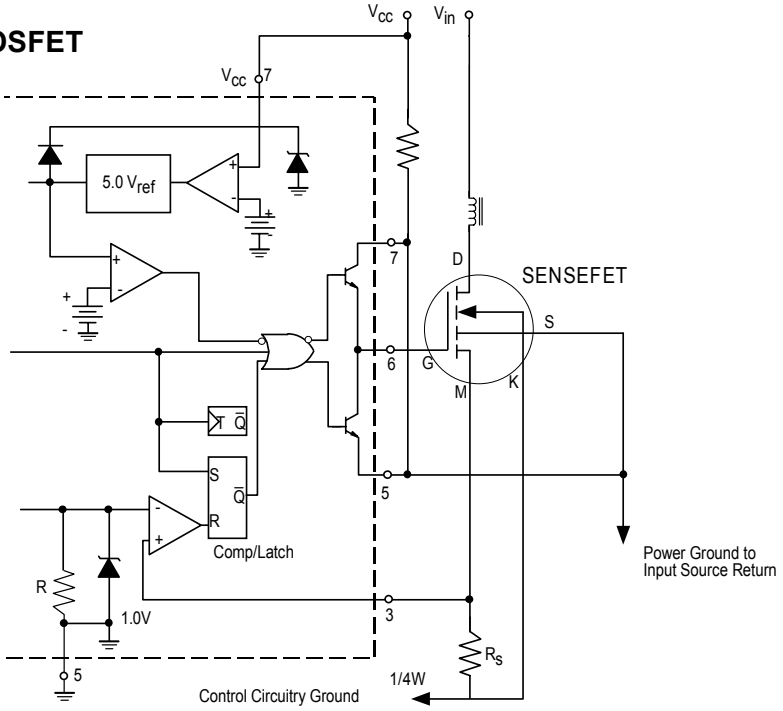
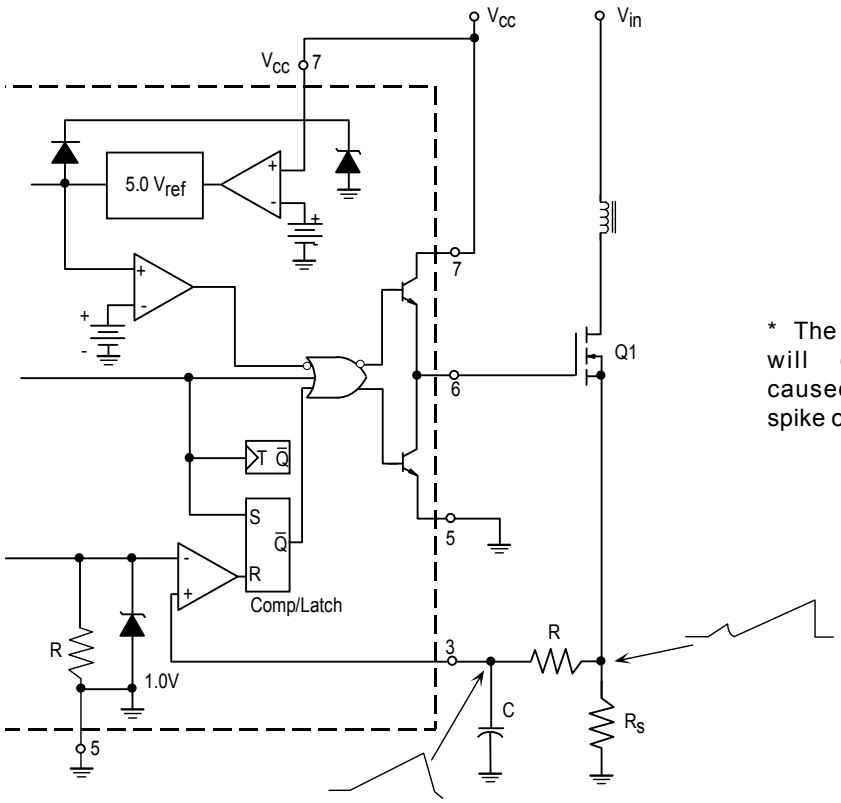


Figure 7.
CURRENT WAVEFROM SPIKE SUPPRESSION

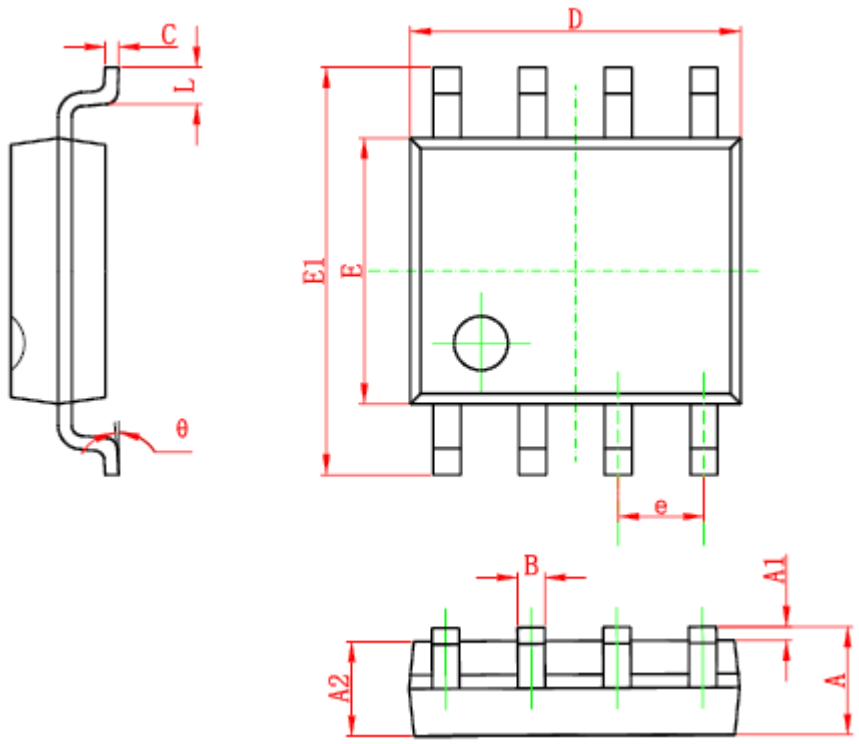


* The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

■ ORDERING INFORMATION

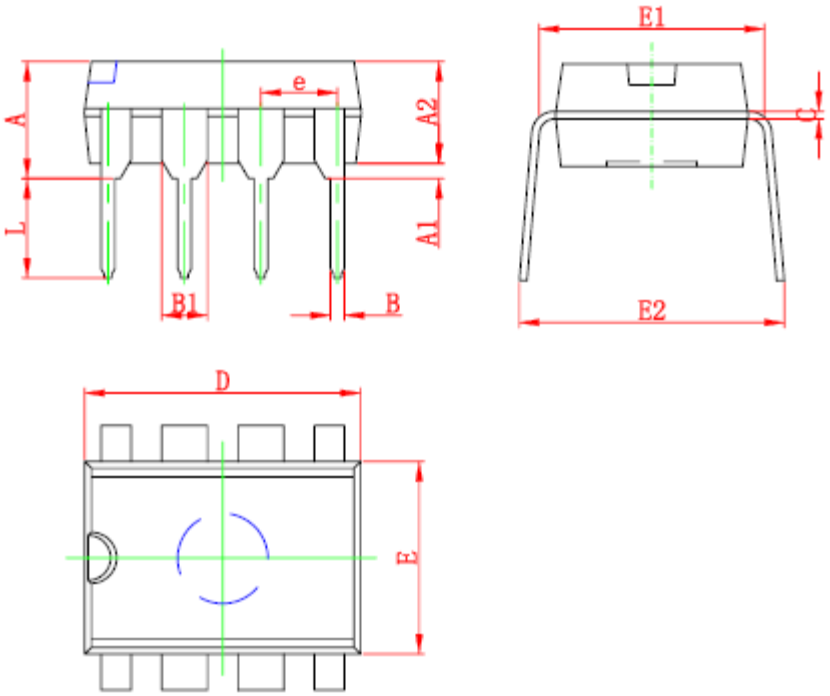
PART No.	PACKAGE		
	SOP-8	SOP-14	DIP-8
GM3842A	GM3842A-S8	GM3842A-S14	GM3842A-D8
GM3843A	GM3843A-S8	GM3843A-S14	GM3843A-D8
GM3844A	GM3844A-S8	GM3844A-S14	GM3844A-D8
GM3845A	GM3845A-S8	GM3845A-S14	GM3845A-D8

■ SOP-8 PACKAGE OUTLINE DIMENSIONS



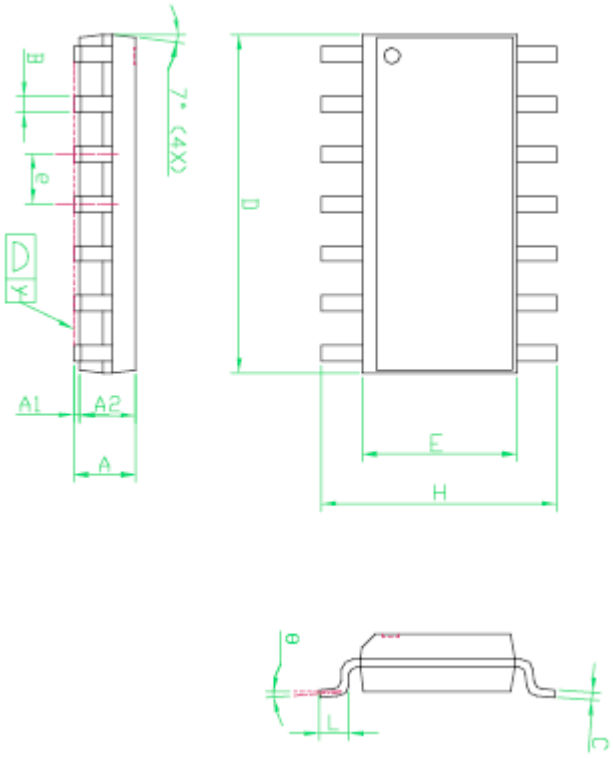
SYMBOL	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.45	1.75	0.057	0.069
A1	0.1	0.25	0.004	0.01
A2	1.35	1.55	0.053	0.061
B	0.306	0.506	0.012	0.02
C	0.153	0.253	0.006	0.01
D	4.81	5.01	0.189	1.197
E	3.84	4.04	0.151	0.159
E1	5.84	6.24	0.23	0.246
e	1.27		0.05	
L	0.45	1	0.018	0.039
θ	0°	8°	0°	8°

■ DIP-8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	3.71	4.31	0.146	0.17
A1	0.51		0.02	
A2	3.2	3.6	0.126	0.142
B	0.36	0.56	0.014	0.022
B1	1.374	1.674	0.054	0.066
C	0.204	0.404	0.008	0.016
D	9	9.4	0.354	0.37
E	6.2	6.6	0.244	0.26
E1	7.42	7.82	0.292	0.308
e	2.34	2.74	0.092	0.108
L	3.1	3.5	0.122	0.138
E2	8.3	9.1	0.327	0.358

■ SOP-14 PACKAGE OUTLINE DIMENSIONS



SYMBOL	Dimensions In Millimeters			Dimensions In Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10		0.25	0.004		0.010
A2		1.45			0.057	
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
L	0.40		1.27	0.016		0.050
y			0.10			0.004
θ	0°		8°	0°		8°

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS
2. DIMENSION L IS MEASURED IN GAGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. FOLLOWED FROM JEDEC MS-012