

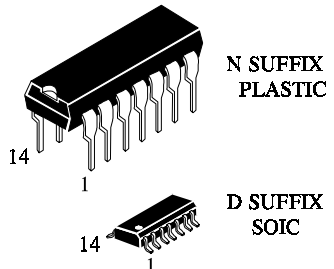
IN74ACT132

**Quad 2-Input NAND Gate
with Schmitt-Trigger Inputs
High-Performance Silicon-Gate CMOS**

The IN74ACT132 is identical in pinout to the LS/ALS132, HC/HCT132. The IN74ACT132 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

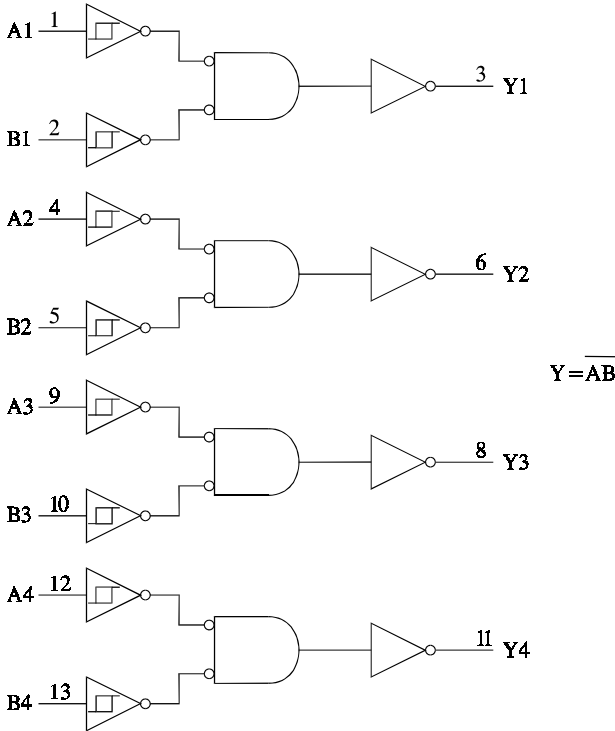
The IN74ACT132 can be used to enhance noise immunity or to square up slowly changing waveforms.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- Outputs Source/Sink 24 mA



ORDERING INFORMATION
 IN74ACT132N Plastic
 IN74ACT132D SOIC
 $T_A = -40^\circ$ to 85° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT

| | | | |
|-----|-----|----|----------|
| A1 | 1 ● | 14 | V_{CC} |
| B1 | 2 | 13 | B4 |
| Y1 | 3 | 12 | A4 |
| A2 | 4 | 11 | Y4 |
| B2 | 5 | 10 | B3 |
| Y2 | 6 | 9 | A3 |
| GND | 7 | 8 | Y3 |

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Sink/Source Current, per Pin | ± 50 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | $^{\circ}C$ |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$
SOIC Package: : - 7 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|--------------------------------------|----------------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_J | Junction Temperature (PDIP) | | 140 | $^{\circ}C$ |
| T_A | Operating Temperature, All Package Types | -40 | +85 | $^{\circ}C$ |
| I_{OH} | Output Current - High | | -24 | mA |
| I_{OL} | Output Current - Low | | 24 | mA |
| t_r, t_f | Input Rise and Fall Time * (except Schmitt Inputs) | $V_{CC} = 4.5 V$ $V_{CC} = 5.5 V$ | 0 10 8.0 | ns/V |

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limits | | Unit |
|----------------------|--|---|----------------------|-------------------|---------------|------|
| | | | | 25 °C | -40°C to 85°C | |
| V _{OH} | Minimum High-Level Output Voltage | I _{OUT} ≤ -50 μA | 4.5 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | |
| | | *V _{IN} ≤ V _T - min or V _T +max I _{OH} =-12 mA I _{OH} =-24 mA I _{OH} =-24 mA | 4.5 | 3.86 | 3.76 | |
| | | | 5.5 | 4.86 | 4.76 | |
| V _{OL} | Maximum Low-Level Output Voltage | I _{OUT} ≤ 50 μA | 4.5 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | |
| | | *V _{IN} ≥ V _T +max I _{OL} =12 mA I _{OL} =24 mA I _{OL} =24 mA | 4.5 | 0.36 | 0.44 | |
| | | | 5.5 | 0.36 | 0.44 | |
| V _T +max | Maximum Positive-Going Input Threshold Voltage | V _{OUT} =0.1 V T _A = Worst Case | 4.5 5.5 | 2.0 2.0 | | V |
| V _T - min | Minimum Negative-Going Input Threshold Voltage | V _{OUT} = V _{CC} - 0.1 V T _A = Worst Case | 4.5 5.5 | 0.8 0.8 | | V |
| V _H max | Maximum Hysteresis Voltage | V _{OUT} =0.1 V or V _{CC} - 0.1 V T _A = Worst Case | 4.5 5.5 | 1.2 1.2 | | V |
| V _H min | Minimum Hysteresis Voltage | V _{OUT} =0.1 V or V _{CC} - 0.1 V T _A = Worst Case | 4.5 5.5 | 0.4 0.4 | | V |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | μA |
| ΔI _{CC} | Addition Quiescent Supply Current | V _{IN} =V _{CC} -2.1 V | 5.5 | | 1.5 | mA |
| I _{OLD} | +Minimum Dynamic Output Current | V _{OLD} =1.65 V Max | 5.5 | | 75 | mA |
| I _{OHD} | +Minimum Dynamic Output Current | V _{OHD} =3.85 V Min | 5.5 | | -75 | mA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND | 5.5 | 4.0 | 40 | μA |

* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

Note: V_H=(V_{T+})-(V_{T-})

AC ELECTRICAL CHARACTERISTICS($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | | | Unit |
|-----------|--|--------------------------------------|------|---------------|------|------|
| | | 25 °C | | -40°C to 85°C | | |
| | | Min | Max | Min | Max | |
| t_{PLH} | Propagation Delay, Input A or B to Output Y (Figure 1) | 3.0 | 11.5 | 2.5 | 13.0 | ns |
| t_{PHL} | Propagation Delay, Input A or B to Output Y (Figure 1) | 3.0 | 11.0 | 2.5 | 12.5 | ns |
| C_{IN} | Maximum Input Capacitance | 4.5 | | 4.5 | | pF |
| C_{PD} | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | | | pF |
| | | 30 | | | | |

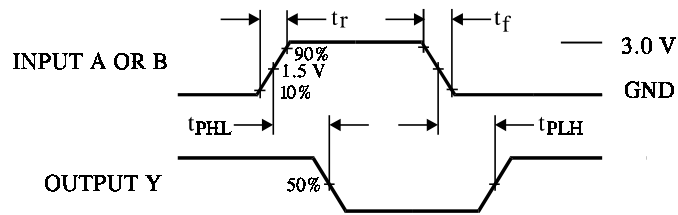


Figure 1. Switching Waveforms