National Semiconductor

June 2004

LMH6503
Wideband, Low Power, Linear Variable Gain Amplifier

General Description

The LMH™6503 is a wideband DC coupled differential input voltage controlled gain stage followed by a high-speed current feedback Op Amp which can directly drive a low impedance load. Gain adjustment range is more than 70dB for up to 10MHz.

Maximum gain is set by external components and the gain can be reduced all the way to cut-off. Power consumption is 370mW with a speed of 135MHz . Output referred DC offset voltage is less than 350mV over the entire gain control voltage range. Device-to-device Gain matching is within 0.7dB at maximum gain. Furthermore, gain at any V_G is tested and the tolerance is guaranteed. The output current feedback Op Amp allows high frequency large signals (Slew Rate = 1800V/µs) and can also drive heavy load current (75mA). Differential inputs allow common mode rejection in low level amplification or in applications where signals are carried over relatively long wires. For single ended operation, the unused input can easily be tied to ground (or to a virtual half-supply in single supply application). Inverting or non-inverting gains could be obtained by choosing one input polarity or the other.

To further increase versatility when used in a single supply application, gain control range is set to be from –1V to +1V relative to pin 11 potential (ground pin). In single supply operation, this ground pin is tied to a "virtual" half supply. Gain control pin has high input impedance to simplify its drive requirement. Gain control is linear in V/V throughout the gain adjustment range. Maximum gain can be set to be anywhere between 1V/V to 100V/V or higher. For linear in dB gain control applications, see LMH6502 datasheet.

The LMH6503 is available in the SOIC-14 and TSSOP-14 package.

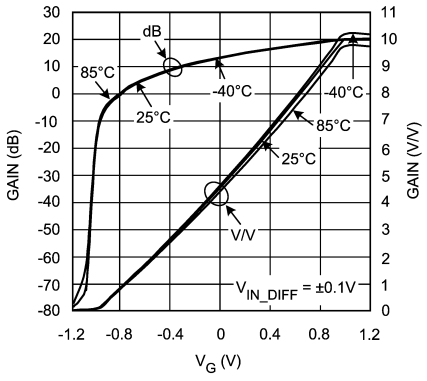
Features

V_S = ±5V, T_A = 25˚C, R_F = 1kΩ, R_G = 174Ω, R_L = 100Ω, A_V = $A_{V(MAX)}$ = 10, Typical values unless specified.

- -3dB BW 135MHz
- Gain control BW 100MHz
- Adjustment range (typical over temp) 70dB
- Gain matching (limit) ±0.7dB
- Slew rate 1800V/µs
- Supply current (no load) 37mA
- Linear output current ±75mA
- Output voltage (R_L = 100Ω) ±3.2V
- Input voltage noise 6.6nV/$\sqrt{Hz}$
- Input current noise 2.4pA/$\sqrt{Hz}$
- THD (20MHz, R_L = 100Ω, V_O = $2V_{PP}$) –57dBc
- Replacement for CLC522

Applications

- Variable attenuator
- AGC
- Voltage controller filter
- Multiplier



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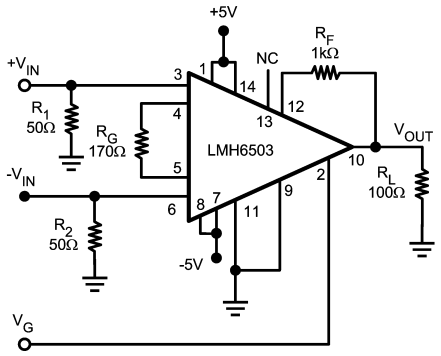
Gain vs. V_G for Various Temperature

Typical Application



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A_{VMAX} = 10V/V

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance: (Note 4)	
Human Body	2KV
Machine Model	200V
Input Current	±10mA
V_{IN} Differential	$\pm(V^+ - V^-)$
Output Current	120mA (Note 3)
Supply Voltages (V^+ - V^-)	12.6V
Voltage at Input/ Output pins	V^+ +0.8V,V^- - 0.8V
Soldering Information:	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C
Storage Temperature Range	–65˚C to +150˚C
Junction Temperature	+150˚C

Operating Ratings (Note 1)

Supply Voltages (V^+ - V^-)		5V to 12V
Temperature Range		–40˚C to +85˚C
Thermal Resistance:	θ_{JA}	θ_{JC}
14-Pin SOIC	138˚C/W	45˚C/W
14-Pin TSSOP	160˚C/W	51˚C/W

Electrical Characteristics(Note 2)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN-_DIFF} = ±0.1V, R_L = 100Ω, V_G = +1V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
Frequency Domain Response						
BW	-3dB Bandwidth	V_{OUT} < 0.5_{PP}		135		MHz
		V_{OUT} < 0.5_{PP}, $A_{V(MAX)}$ = 100		50		
GF	Gain Flatness	V_{OUT} < $0.5V_{PP}$, –1V < V_G < 1V, ±0.2dB		40		MHz
Att Range	Flat Band (Relative to Max Gain)	±0.2dB Flatness, f < 30MHZ		20		MHz
	Attenuation Range (Note 13)	±0.1dB, f < 30MHZ		6.6		
BW Control	Gain Control Bandwidth	V_G = 0V (Note 11)		100		MHz
PL	Linear Phase Deviation	DC to 60MHz		1.6		deg
G Delay	Group Delay	DC to 130MHz		2.6		ns
CT (dB)	Feed-through	V_G = –1.2V, 30MHz (Output Referred)		–48		dB
GR	Gain Adjustment Range	f < 10MHz		79		dB
		f < 30MHz		68		
Time Domain Response						
t_r , t_f	Rise and Fall Time	0.5V Step		2.2		ns
OS%	Overshoot	0.5V Step		10		%
SR	Slew Rate	4V Step (Note 5)		1800		V/µs
ΔG Rate	Gain Change Rate	V_{IN} = 0.3V, 10%–90% of final output		4.6		dB/ns
Distortion & Noise performance						
HD2	2^{nd} Harmonic Distortion	$2V_{PP}$, 20MHz		–60		dBc
HD3	3^{rd}Harmonic Distortion	$2V_{PP}$, 20MHz		–61		dBc
THD	Total Harmonic Distortion	$2V_{PP}$, 20MHz		–57		dBc
En tot	Total Equivalent Input Noise	1MHz to 150MHz		6.6		nV/$\sqrt{Hz}$
I_n	Input Noise Current	1MHz to 150MHz		2.4		pA/$\sqrt{Hz}$
DG	Differential Gain	f = 4.43MHz, R_L = 150Ω, Neg. Sync		0.15		%
DP	Differential Phase	f = 4.43MHz, R_L = 150Ω, Neg. Sync		0.22		deg

Electrical Characteristics(Note 2) (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_S = ±5V, $A_{V(MAX)}$ = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN_DIFF} = ±0.1V, R_L = 100Ω, V_G = +1V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
DC & Miscellaneous Performance						
GACCU	Gain Accuracy (see Application Notes)	V_G =1.0V		+0.25	+0.9/–0.4	dB
		0V < V_G < 1V		±0.3	+1.3/–1.5	
		–0.7V < V_G < 1V		±0.4	+4.4/–4.3	
G Match	Gain Matching (see Application Notes)	V_G = 1.0		–	±0.7	dB
		0 < V_G < 1V		–	+1.7/–1.1	
		–0.7V < V_G < 1V		–	+4.0/–4.7	
K	Gain Multiplier (see Application Notes)		1.58 **1.58**	1.72	1.87 **1.91**	V/V
V_{CM}	Input Voltage Range	Pin 3 & 6 Common Mode, |CMRR| > 50dB (Note 9)	±2.0 **±1.80**	±2.2		V
V_{IN_DIFF}	Differential Input Voltage	Across pins 3 & 6	±0.34 **±0.28**	±0.37		V
$I_{RG\ MAX}$	R_G Current	Pins 4 & 5	±1.70 **±1.60**	±2.30		mA
I_{BIAS}	Bias Current	Pins 3 & 6 (Note 7)		11	18 **20**	µA
		Pins 3 & 6 (Note 7), V_S= ±2.5V		3	10 **13**	
TC_{BIAS}	Bias Current Drift	Pin 3 & 6 (Note 8)		100		nA/˚C
I_{OFF}	Offset Current	Pin 3 & 6		0.01	2.0 **2.5**	µA
TC I_{OFF}	Offset Current Drift	(Note 8)		5		nA/˚C
R_{IN}	Input Resistance	Pin 3 & 6		750		kΩ
C_{IN}	Input Capacitance	Pin 3 & 6		5		pF
IV_G	V_G Bias Current	Pin 2, V_G = 1.4V(Note 7)		45		µA
TC IV_G	V_G Bias Drift	Pin 2 (Note 8)		20		nA/˚C
R V_G	V_G Input Resistance	Pin 2		70		KΩ
C V_G	V_G Input Capacitance	Pin 2		1.3		pF
V_{OUT}	Output Voltage Range	R_L = 100Ω	±3.00 **±2.97**	±3.20		V
		R_L Open	±3.95 **±3.90**	±4.05		
R_{OUT}	Output Impedance	DC		0.1		Ω
I_{OUT}	Output Current	V_{OUT} ±4V from Rails	±75 **±70**	±90		mA
$V_{O\ OFFSET}$	Output Offset Voltage	–1V < V_G < 1V		±80	±350 **±380**	mV
+PSRR	+Power Supply Rejection Ratio (see (Note 10))	Input Referred, 1V change, V_G = 1.4V		–80	–58 **–56**	dB
–PSRR	–Power Supply Rejection Ratio (see (Note 10))	Input Referred, 1V change, V_G = 1.4V		–67	–57 **–51**	dB
CMRR	Common Mode Rejection Ratio (see (Note 9))	Input Referred, V_G = 1V –1.8V < V_{CM} < 1.8V		–67		dB
I_S	Supply Current	R_L = Open		37	50 **53**	mA
		R_L = Open, V_S = ±2.5V		12	20 **23**	

Electrical Characteristics(Note 2) (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations or value specified, whichever is lower.

Note 4: Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

Note 5: Slew Rate is the average of the rising and falling rates.

Note 6: Typical values represent the most likely parametric norm. Bold numbers refer to over temperature limits.

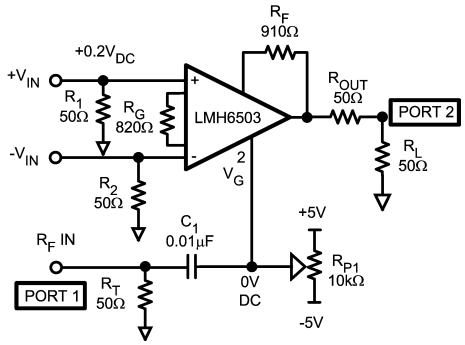
Note 7: Positive current correspondes to current flowing in the device.

Note 8: Drift determined by dividing the change in parameter distribution at temperature extremes by the total temperature change.

Note 9: CMRR definition: $[|\Delta V_{OUT}/\Delta V_{CM}|/A_V]$ with 0.1V differential input voltage. ΔV_{OUT} is the change in output voltage with offset shift subtracted out.

Note 10: +PSRR definition: $[|\Delta V_{OUT}/\Delta V^+|/A_V]$, -PSRR definition: $[|\Delta V_{OUT}/\Delta V^-|/A_V]$ with 0.1V differential input voltage. ΔV_{OUT} is the change in output voltage with offset shift subtracted out.

Note 11: Gain Control Frequency Response Schematic:



Note 12: Gain/Phase normalized to low frequency value at each A_V.

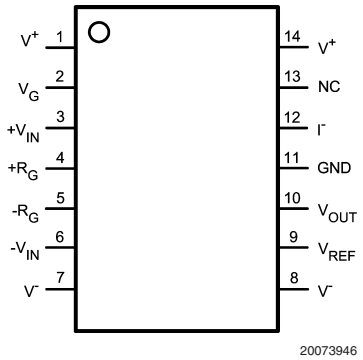
Note 13: Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB), relative to A_{VMAX} gain. For example, for f<30MHz, here are the Flat Band Attenuation ranges:

±0.2dB: 10V/V down to 1V/V=20dB range

±0.1dB: 10V/V down to 4.7V/V=6.5dB range

Connection Diagram

14-Pin SOIC/TSSOP



Top View

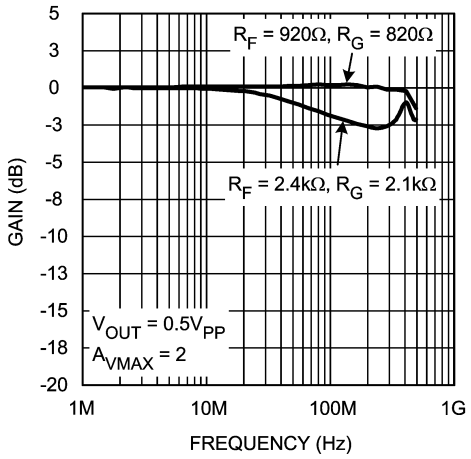
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
14-pin SOIC	LMH6503MA	LMH6503MA	55 Units/Rail	M14A
	LMH6503MAX		2.5k Units Tape and Reel	
14-Pin TSSOP	LMH6503MT	LMH6503MT	94 Units/Rail	MTC14
	LMH6503MTX		2.5k Units Tape and Reel	

Typical Performance Charateristics

Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output:

Small Signal Frequency Response (A_V = 2)



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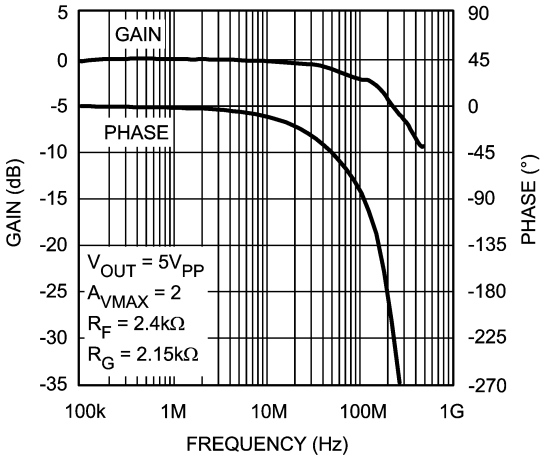
Large Signal Frequency Response (A_V = 2)



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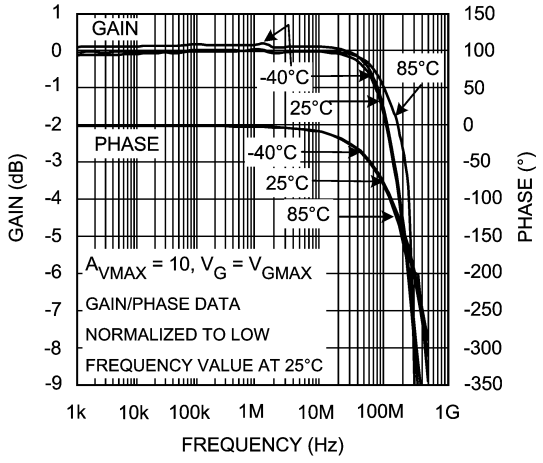
Frequency Response over Temperature (A_V = 10)



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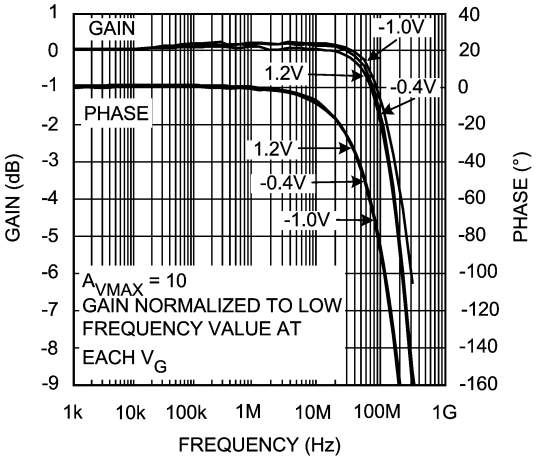
Frequency Response for Various V_G (A_{VMAX} = 10)



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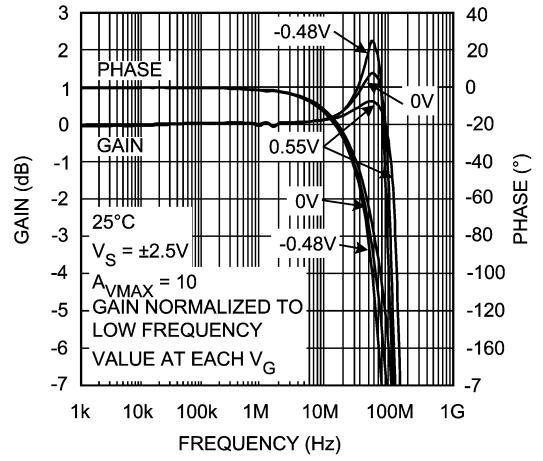
Frequency Response for Various V_G (A_{VMAX} = 10) (±2.5V)



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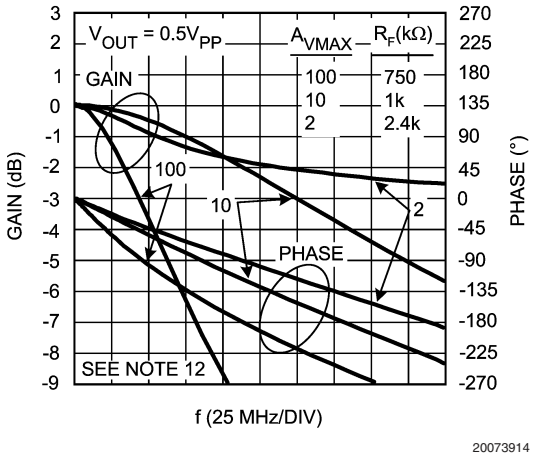
Small Signal Frequency Response



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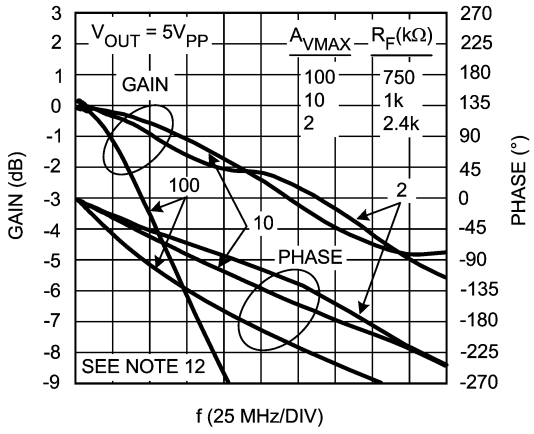
Typical Performance Charateristics

Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

Large Signal Frequency Response



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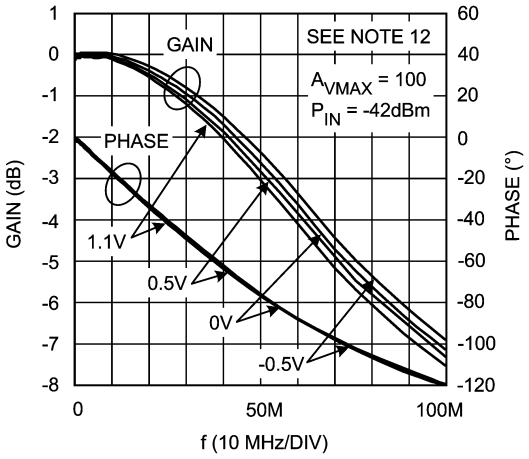
Frequency Response for Various V_G (A_{VMAX} = 100) (Small Signal)



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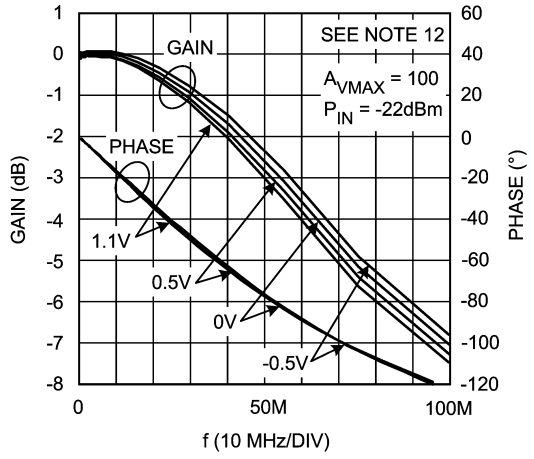
Frequency Response for Various V_G (A_{VMAX} = 100) (Large Signal)



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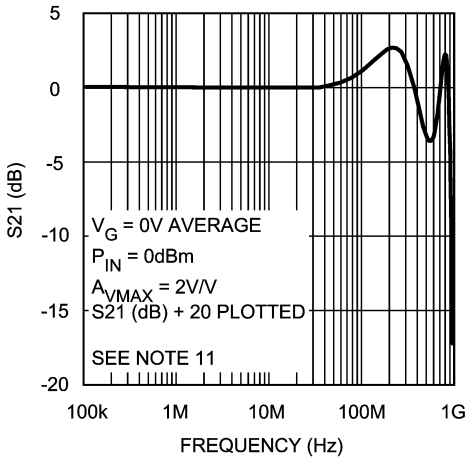
Gain Control Frequency Response



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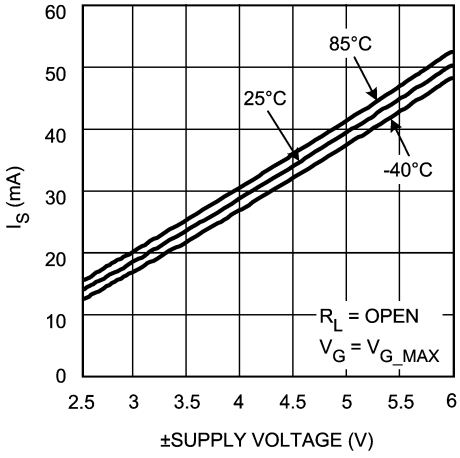
I_S vs. V_S



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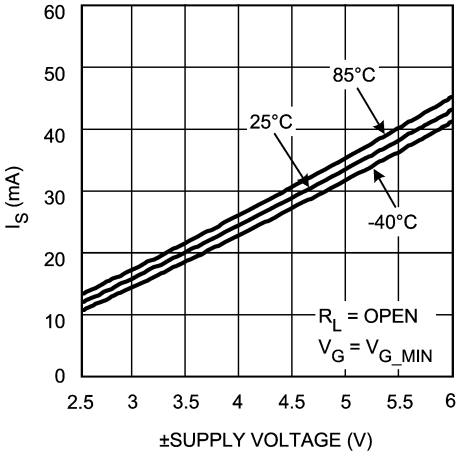
I_S vs. V_S



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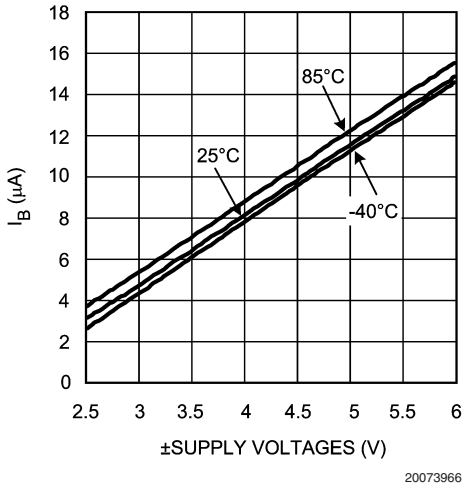
Typical Performance Charateristics

Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

Input Bias Current vs. V_S



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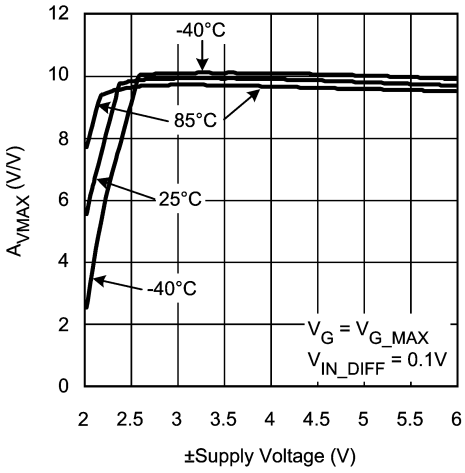
A_{VMAX} vs. V_S



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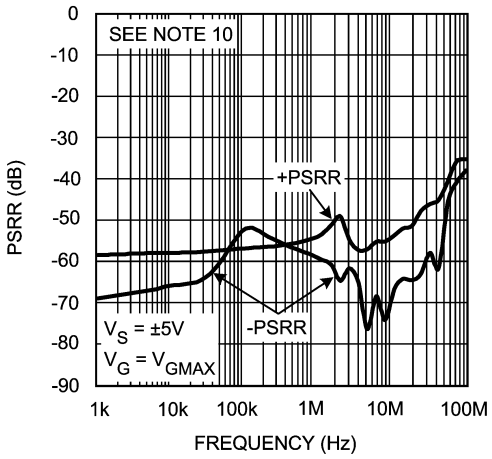
PSRR ±5V



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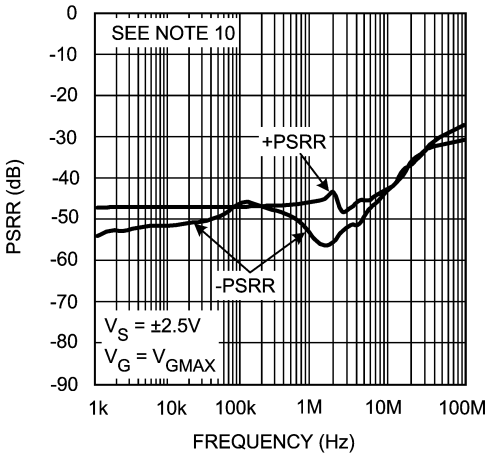
PSRR ±2.5V



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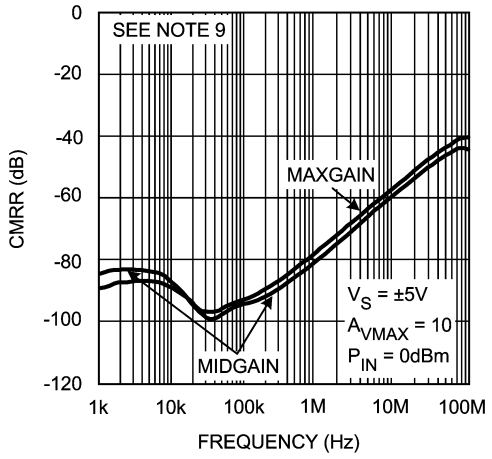
CMRR ±5V



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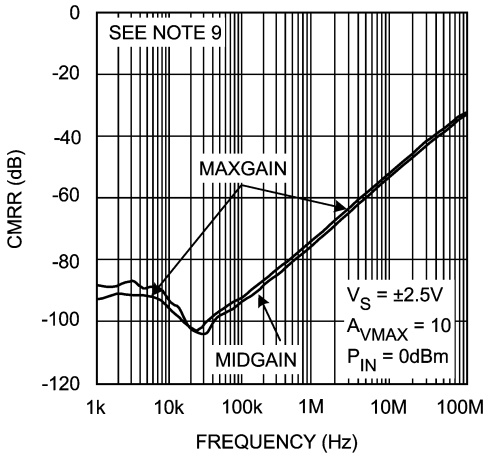
CMRR ±2.5V



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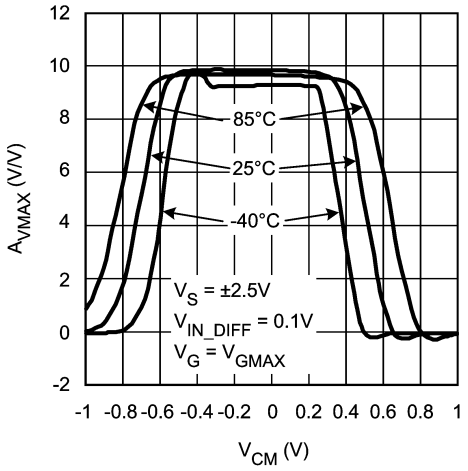
Typical Performance Charateristics

Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

A_{VMAX} vs. V_{CM}



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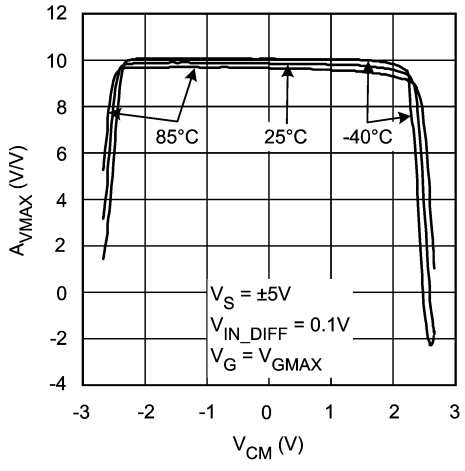
A_{VMAX} vs. V_{CM}



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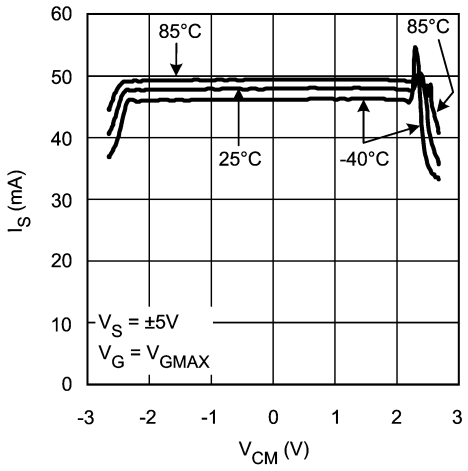
Supply Current vs. V_{CM}



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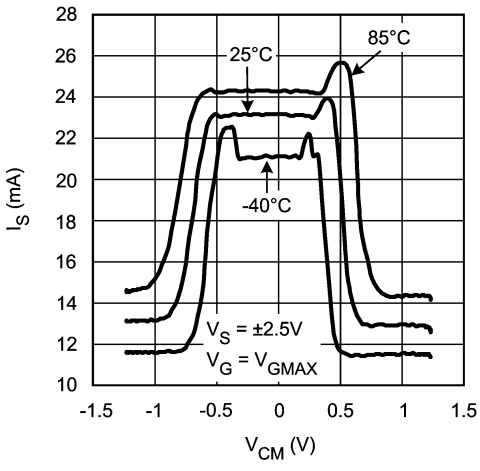
Supply Current vs. V_{CM}



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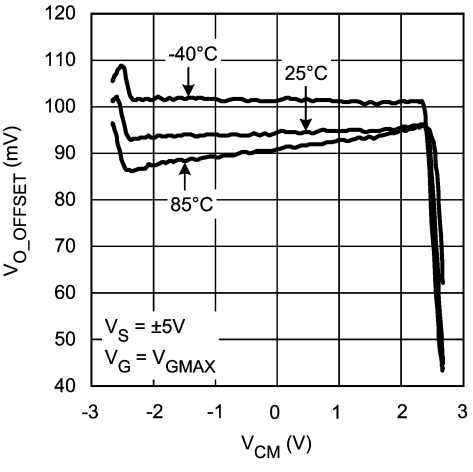
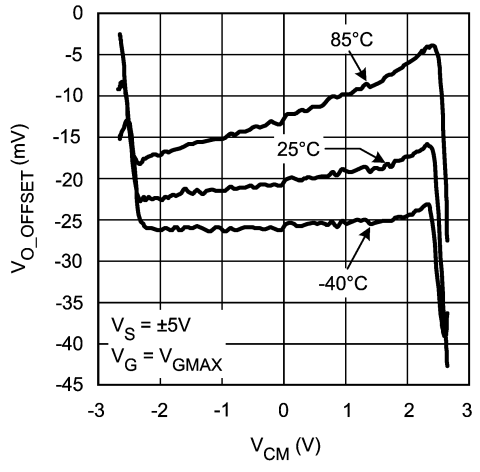
Output Offset Voltage vs.V_{CM} (Typical Unit 1)



20073975

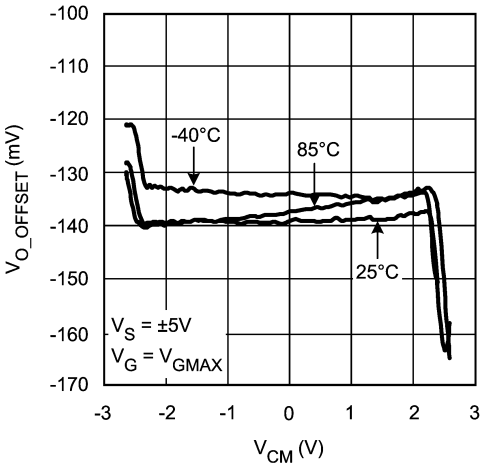
Output Offset Voltage vs.V_{CM} (Typical Unit 2)



20073976

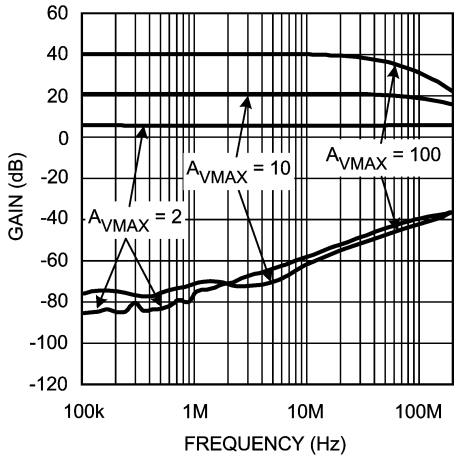
Typical Performance Charateristics Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

Output Offset Voltage vs.V_{CM} (Typical Unit 3)



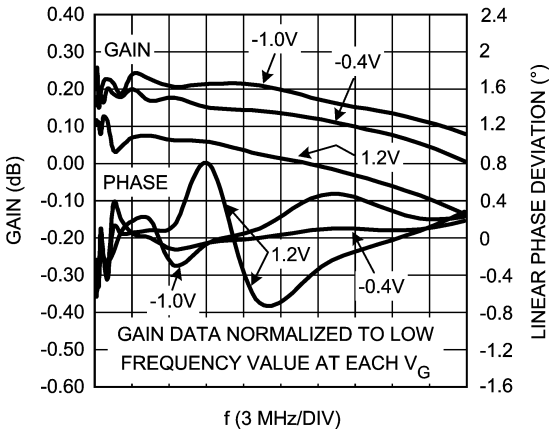
20073977

Feed through Isolation



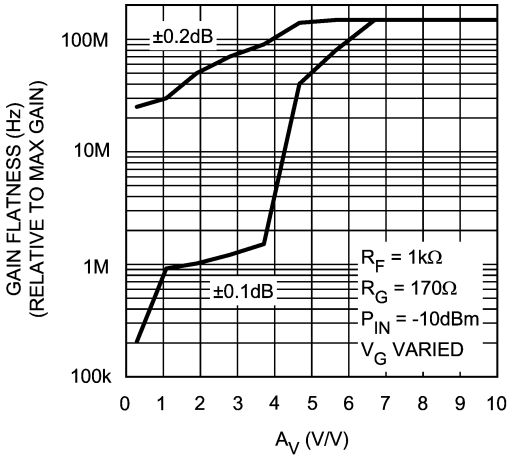
20073918

Gain Flatness and Linear Phase Deviation



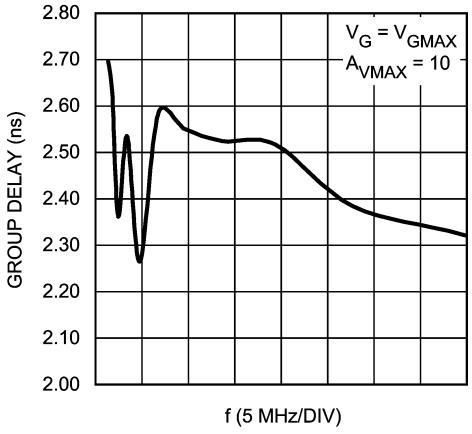
20073921

Gain Flatness Frequency vs. Gain (Note 13)



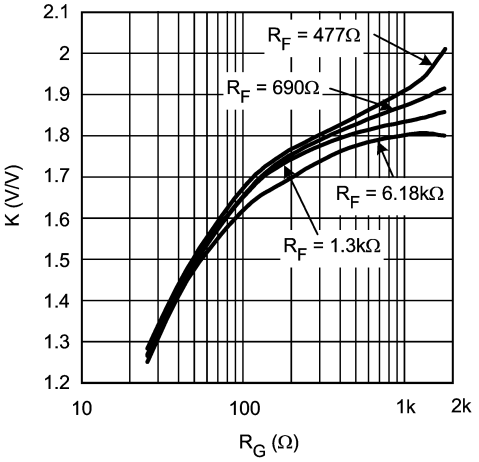
20073924

Group Delay vs. Frequency



20073927

K Factor vs. R_G

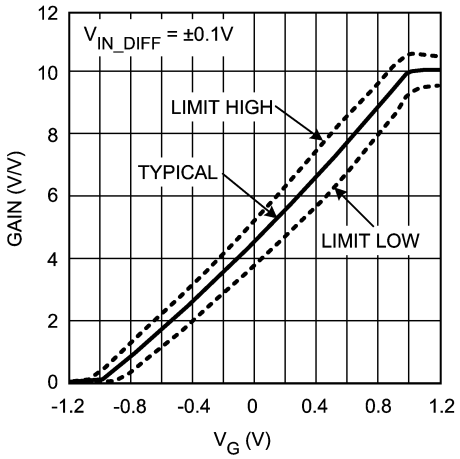


20073901

Typical Performance Charateristics

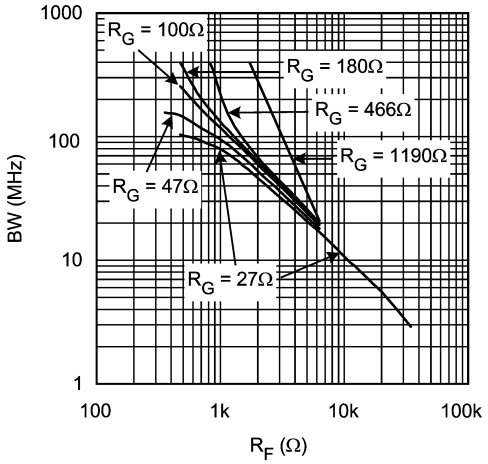
Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

Gain vs. V_G Including Limits



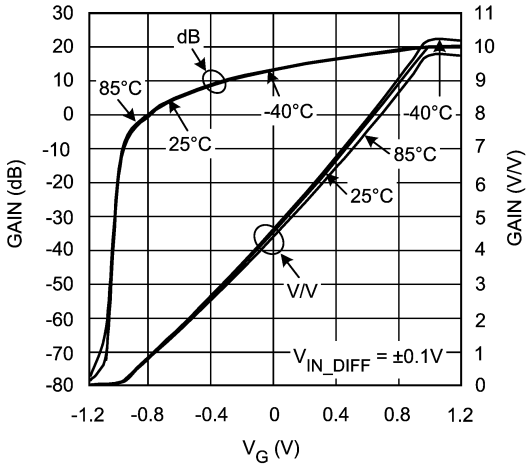
20073912

BW vs. R_F for Various R_G



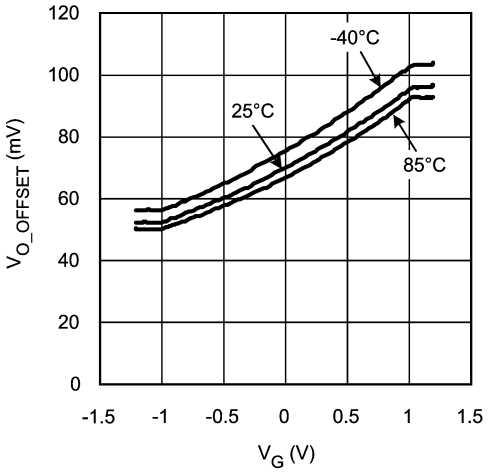
20073903

Gain vs. V_G (±5V)



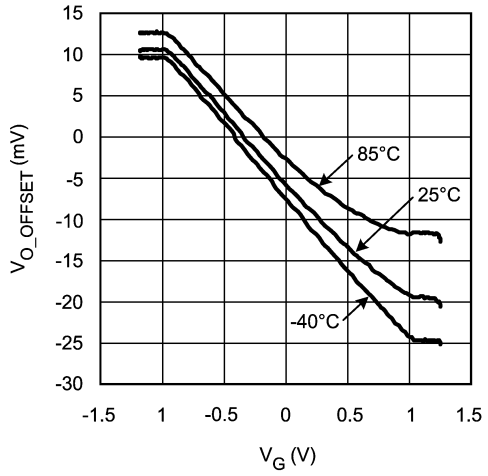
20073913

Output Offset Voltage vs. V_G (Typical Unit 1)



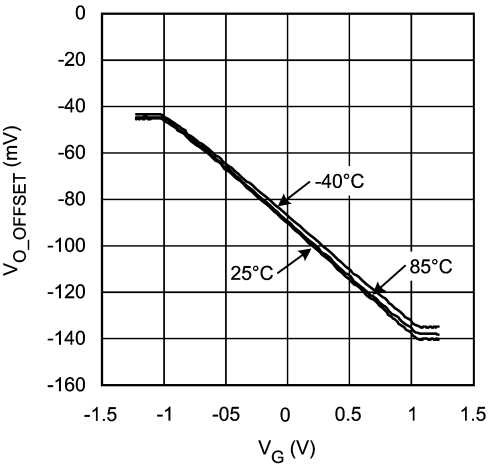
20073968

Output Offset Voltage vs. V_G (Typical Unit 2)



20073969

Output Offset Voltage vs. V_G (Typical Unit 3)

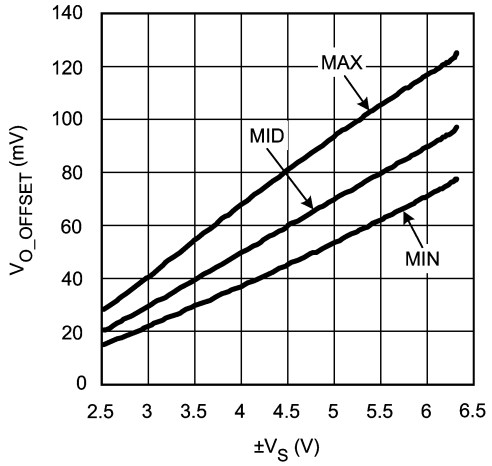


20073970

Typical Performance Charateristics

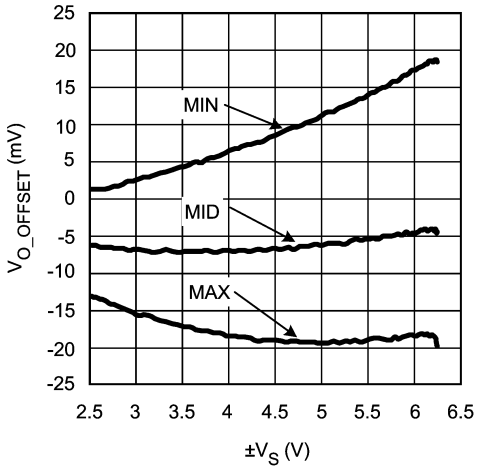
Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

Output Offset Voltage vs. ±V_S for Various V_G (Typical Unit 1)



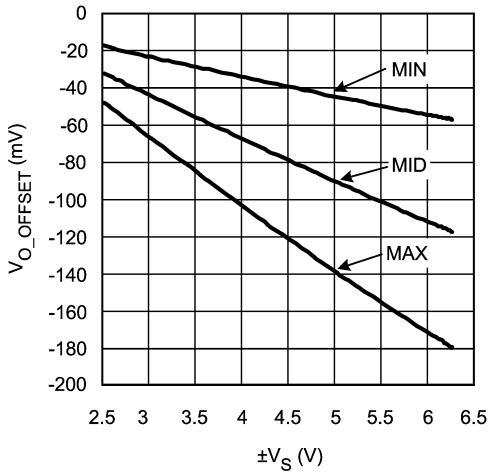
20073978

Output Offset Voltage vs. ±V_S for Various V_G (Typical Unit 2)



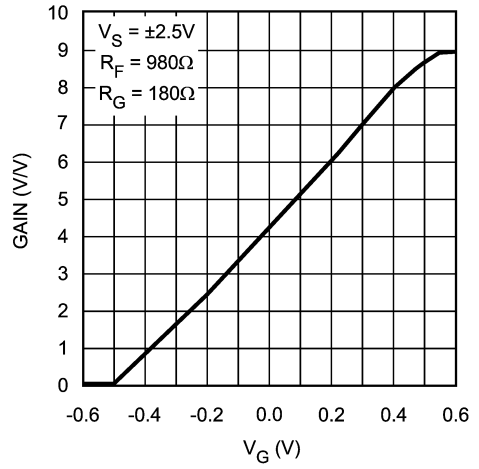
20073979

Output Offset Voltage vs. ±V_S for Various V_G (Typical Unit 3)



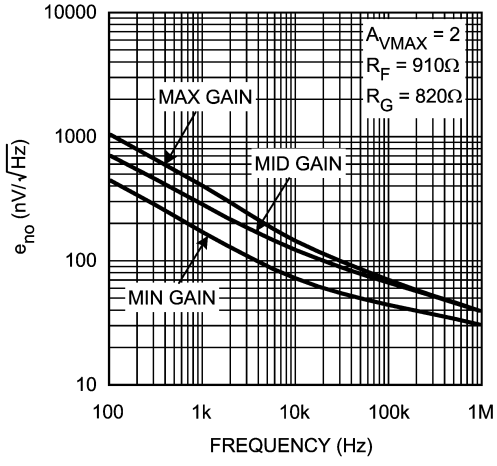
20073980

Gain vs. V_G (±2.5V)



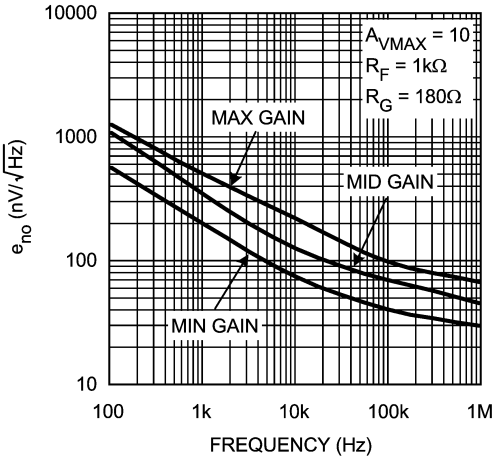
20073929

Noise vs. Frequency (A_{VMAX} = 2)



20073923

Noise vs. Frequency (A_{VMAX} = 10)

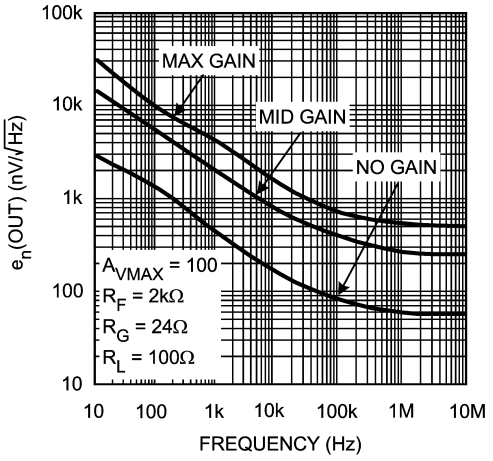


20073922

Typical Performance Charateristics

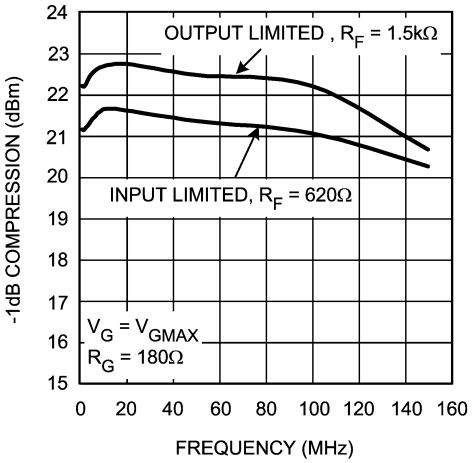
Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

Noise vs. Frequency (A_{VMAX} = 100)



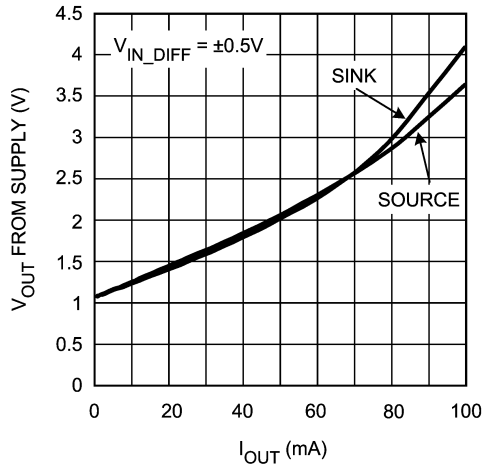
20073931

–1dB Compression



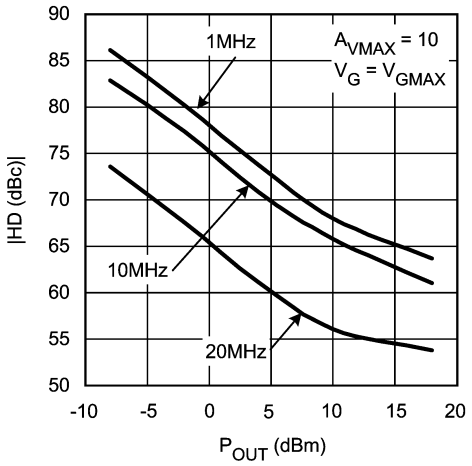
20073911

Output Voltage vs. Output Current



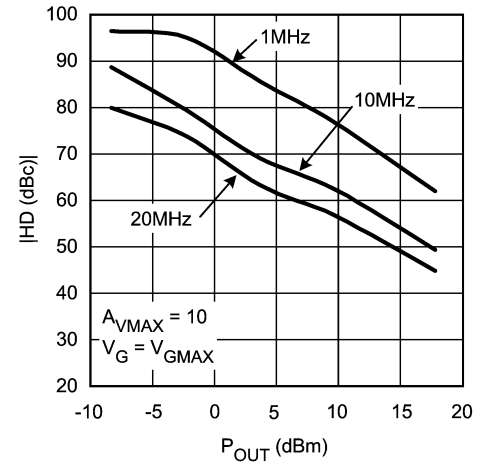
20073945

HD2 vs. P_{OUT}



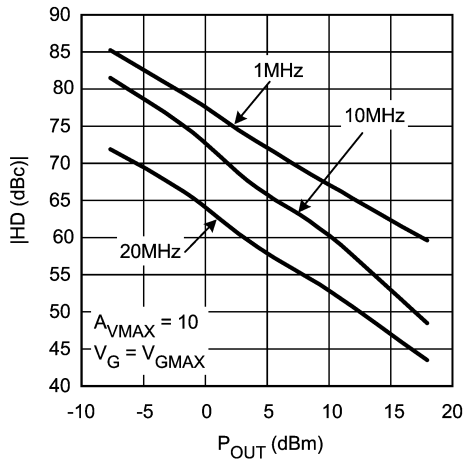
20073940

HD3 vs. P_{OUT}



20073941

THD vs. P_{OUT}

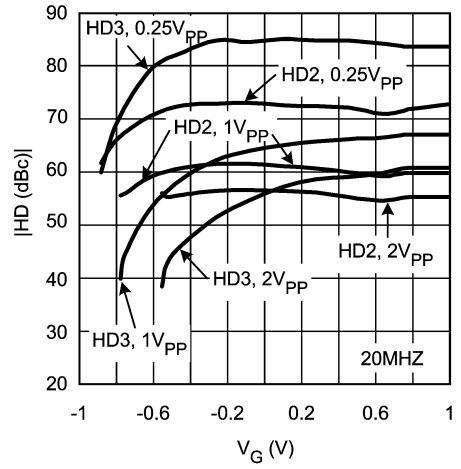


20073939

Typical Performance Charateristics

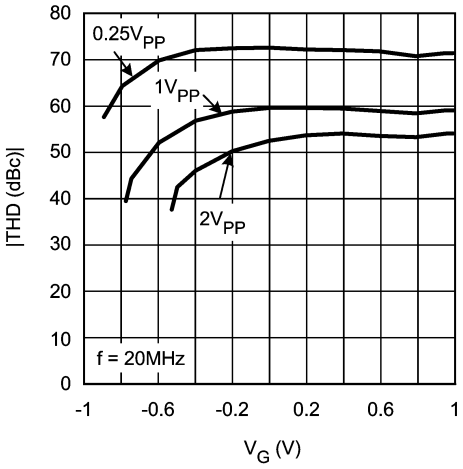
Unless otherwise specified: V_S = ±5V, 25˚C, V_G = V_{G_MAX}, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

HD2 & HD3 vs. V_G



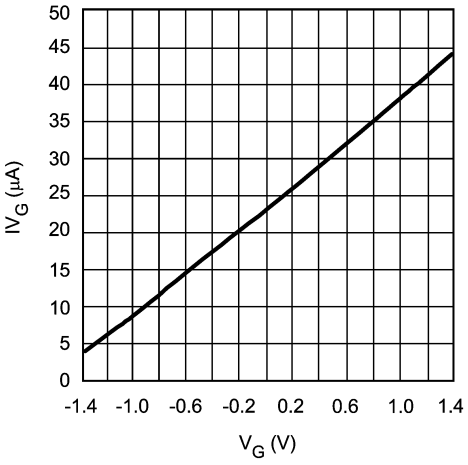
20073942

THD vs. V_G



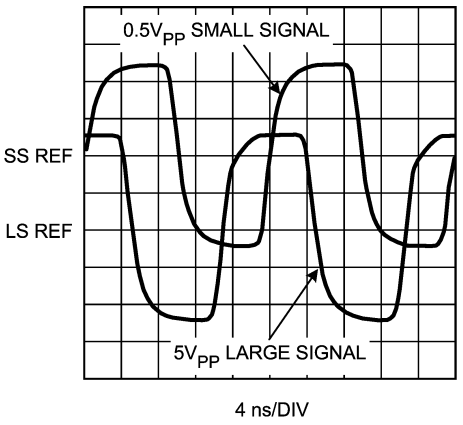
20073938

V_G Bias Current vs. V_G



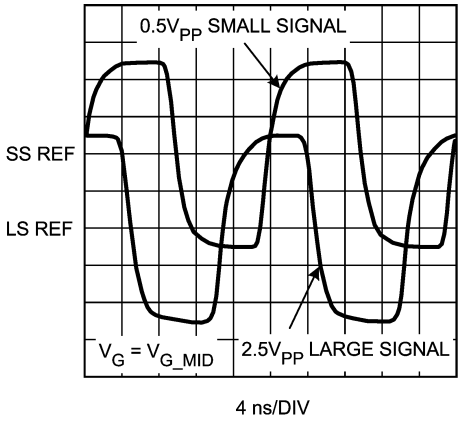
20073937

Step Response Plot



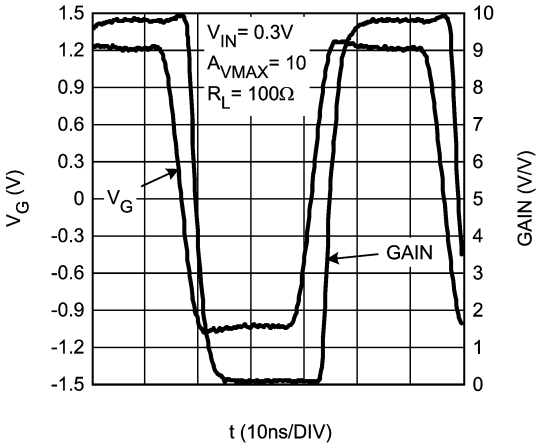
20073962

Step Response Plot



20073963

Gain vs. V_G Step

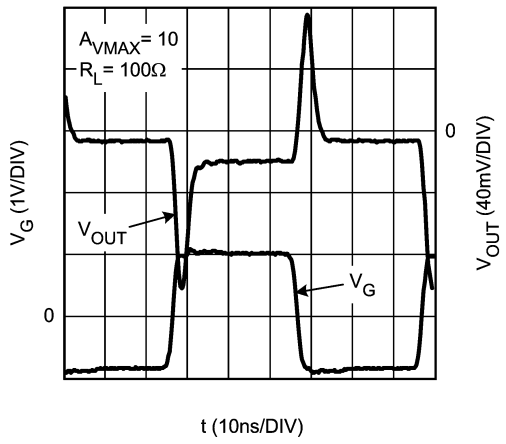


20073981

Typical Performance Charateristics

Unless otherwise specified: V_S = ±5V, 25˚C, $V_G = V_{G\_MAX}$, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, both inputs terminated in 50Ω, R_L = 100Ω, Typical values, results referred to device output: (Continued)

V_G Feedthrough



20073982

Application Information

THEORY OF OPERATION

The LMH6503 is a linear wideband variable-gain amplifier as illustrated in *Figure 1*. A voltage input signal may be applied differentially between the two inputs ($+V_{IN}$, $-V_{IN}$), or single-endedly by grounding one of the two unused inputs. The LMH6503 input buffers convert the input voltage to a current (I_{RG}) that is a function of the differential input voltage (V_{INPUT} = ($+V_{IN}$) - ($-V_{IN}$)) and the value of the gain setting resistor (R_G). This current (I_{RG}) is then mirrored to a gain stage with a current gain of K (1.72 nominal). The voltage controlled two-quadrant multiplier attenuates this current which is then converted to a voltage via the output amplifier. This output amplifier is a current feedback op amp configured as a Transimpedance amplifier. Its Transimpedance gain is the feedback resistor (R_F). The input signal, output, and gain control are all voltages. The output voltage can easily be calculated as shown in Equation 1:

$$V_{OUT} = I_{RG} \times K \times \left[\frac{V_G + 1}{2}\right] \times R_F \quad \text{FOR } -1 < V_G < +1 \tag{1}$$

Where K = 1.72 (Nominal)

since:

$$I_{RG} = \frac{V_{INPUT}}{R_G}$$

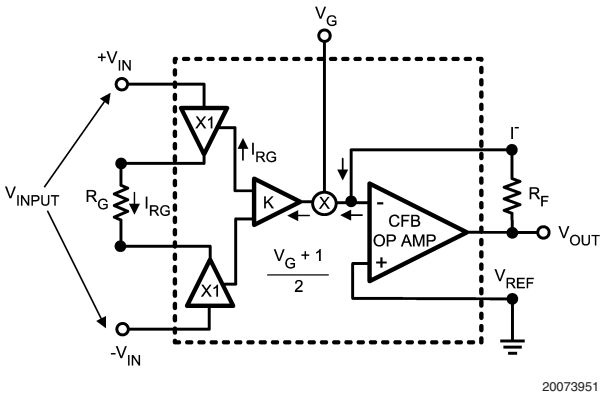
The gain of the LMH6503 is therefore a function of three external variables: R_G, R_F, and V_G as expressed in Equation 2:

$$A_V = \frac{R_F}{R_G} \times 1.72 \times \left[\frac{V_G + 1}{2}\right] \tag{2}$$

The gain control voltage (V_G) has an ideal input range of $-1V < V_G < +1V$. At V_G = +1V, the gain of the LMH6503 is at its maximum as expressed in Equation 3:

$$A_V = 1.72 \frac{R_F}{R_G} \tag{3}$$

Notice also that Equation 3 holds for both differential and single ended operation.



20073951

FIGURE 1. LMH6503 Functional Block Diagram

CHOOSING R_F AND R_G

R_G is calculated from Equation 4. $V_{INPUTMAX}$ is the maximum peak

$$R_G = \frac{V_{INPUT_{MAX}}}{I_{R_{GMAX}}} \tag{4}$$

input voltage (V_{pk}) determined by the application. I_{RGMAX} is the maximum allowable current through R_G and is typically 2.3mA. Once A_{VMAX} is determined from the minimum input and desired output voltages, R_F is then determined using Equation 5. These values of R_F and R_G are

Application Information (Continued)

$$R_F = \frac{1}{K} * R_G * A_{VMAX} \quad (5)$$

the minimum possible values that meet the input voltage and maximum gain constraints. Scaling the resistor values will decrease bandwidth and improve stability.

Figure 2 illustrates the resulting LMH6503 bandwidths as a function of the maximum (y axis) and minimum (related to x axis) input voltages when V_{OUT} is held constant at $1V_{PP}$.

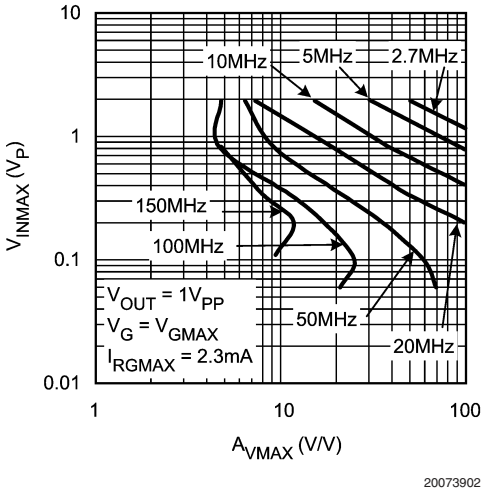


FIGURE 2. Bandwidth vs. V_{INMAX} and A_{VMAX}

ADJUSTING OFFSETS

Treating the offsets introduced by the input and output stages of the LMH6503 is accomplished with a two step process. The offset voltage of the output stage is treated by first applying −1.1V on V_G, which effectively isolates the input stage and multiplier core from the output stage. As illustrated in *Figure 3*, the trim pot located at R14 on the LMH6503 Evaluation Board (CLC730033) should then be adjusted in order to null the offset voltage seen at the LMH6503's output (pin 10).

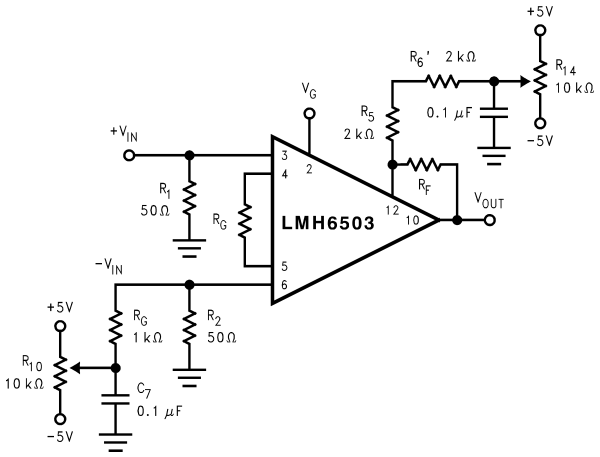


FIGURE 3. Nulling the Output Offset Voltage

Once this is accomplished, the offset errors introduced by the input stage and multiplier core can then be treated. The second step requires the absence of an input signal and matched source impedances on the two input pins in order to cancel the bias current errors. This done, then +1.1V should be applied to V_G and the trim pot located at R_{10} adjusted in order to null the offset voltage seen at the LMH6503's output. If a more limited gain range is anticipated, the above adjustments should be made at these operating points. These steps will minimize the output offset voltage. However, since the offset term itself varies with the gain setting, the correction is not perfect and some residual output offset will remain.

GAIN ACCURACY

Defined as the ratio of measured gain (V/V), at a certain V_G, to the best fit line drawn through the typical gain (V/V) distribution for $-1V < V_G < 1V$ (results expressed in dB) (See *Figure 4*). The best fit gain (A_V) is given by:

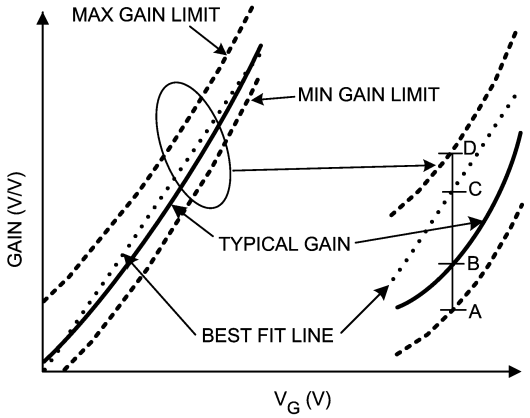
$$A_V \text{ (V/V)} = 4.87V_G + 4.61 \quad (6)$$

For: $-1V \le V_G \le +1V$, $R_F = 1k\Omega$, $R_G = 174\Omega$

For a V_G range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the worst case ratio between the "Typical Gain" and the best fit line. The "Max" value would be the worst case between the max/min gain limit and the best fit line.

GAIN MATCHING

Defined as the limit on gain variation at a certain V_G (expressed in dB) (See *Figure 4*). Specified as "Max" only (no "Typical"). For a V_G range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case ratio between the max/min gain limit and the typical gain.



PARAMETER:
GAIN ACCURACY (TYPICAL) = B/C (dB)
GAIN ACCURACY (+ & - LIMIT) = D/C & A/C (dB)
GAIN MATCHING (+ & - LIMIT) = D/B & A/B (dB)

20073955

FIGURE 4. Gain Accuracy and Gain Matching Parameters Defined

Application Information (Continued)

NOISE

Figure 5 describes the LMH6503's output-referred spot noise density as a function of frequency with A_{VMAX} = 10V/V. The plot includes all the noise contributing terms. However, with both inputs terminated in 50Ω, the input noise contribution is minimal. At A_{VMAX} = 10V/V, the LMH6503 has a typical flat-band input-referred spot noise density (e_{in}) of 6.6nV/$\sqrt{Hz}$. For applications with –3dB BW extending well into the flat-band region, the input RMS voltage noise can be determined from the following single-pole model:

$$V_{RMS} = e_{in} * \sqrt{1.57 * (-3dB\ BANDWIDTH)} \quad (7)$$

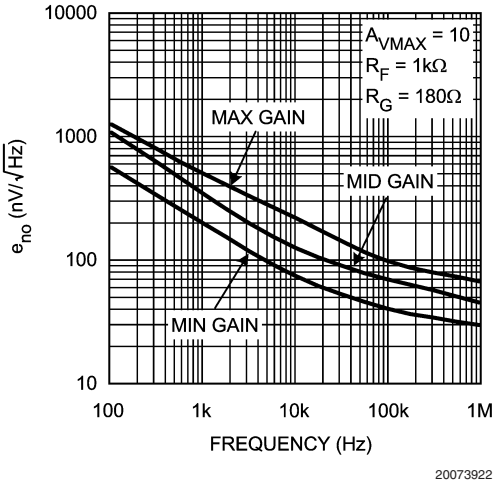


FIGURE 5. Output Referred Voltage Noise vs. Frequency

CIRCUIT LAYOUT CONSIDERATIONS

Good high-frequency operation requires all of the decoupling capacitors shown in *Figure 6* to be placed as close as possible to the power supply pins in order to insure a proper high-frequency low-impedance bypass. Adequate ground plane and low inductive power returns are also required of the layout. Minimizing the parasitic capacitances at pins 3, 4, 5, 6, 9, 10 and 12 will assure best high frequency performance. The parasitic inductance of component leads or traces to pins 4, 5 and 9 should also be kept to a minimum. Parasitic or load capacitance, C_L, on the output (pin 10) degrades phase margin and can lead to frequency response peaking or circuit oscillation. The LMH6503 is fully stable when driving a 100Ω load. With reduced load (e.g. 1kΩ) there is a possibility of instability at very high frequencies beyond 400MHz especially with a capacitive load. When the LMH6503 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100Ω and 39pF in series tied between the LMH6503 output and ground). C_L can also be isolated from the output by placing a small resistor in series with the output (pin 10).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

National Semiconductor suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6503MA	SOIC-14	CLC730033
LMH6503MT	TSSOP-14	CLC730146

The evaluation board is shipped when a device sample request is placed with National Semiconductor.

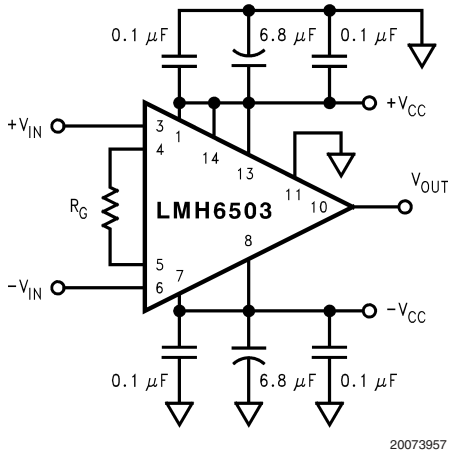


FIGURE 6. Required Power Supply Decoupling

SINGLE SUPPLY OPERATION

It is possible to operate the LMH6503 with a single supply. To do so, tie pin 11 (GND) to a potential about mid point between V^+ and V^-. Two examples are shown in *Figure 7* & *Figure 8*.

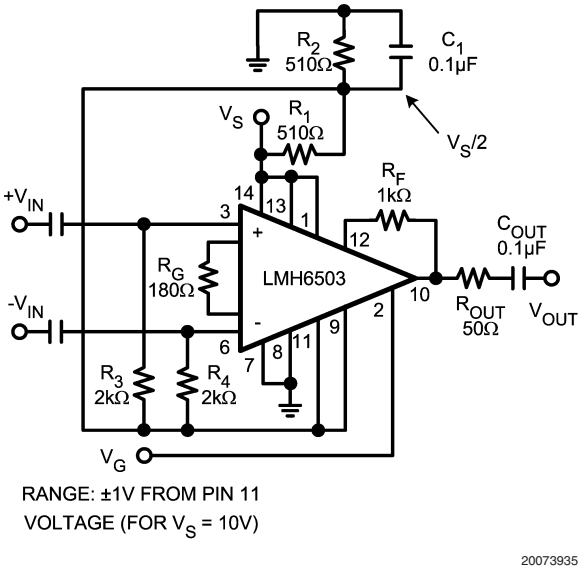


FIGURE 7. AC Coupled Single Supply VGA

Application Information (Continued)

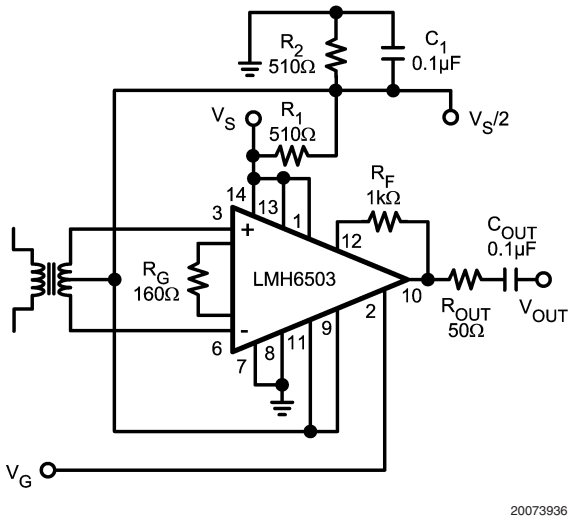


FIGURE 8. Transformer Coupled Single Supply VGA

OPERATING AT LOWER SUPPLY VOLTAGES

The LMH6503 is rated for operation down to 5V supplies (V^+ - V^-). There are some specifications shown for operation at ±2.5V within the data sheet (i.e. Frequency Response, CMRR, PSRR, Gain vs. V_G, etc.). Compared to ±5V operation, at lower supplies:

a) V_G range constricts. Referring to *Figure 9*, note that V_{G_MAX} (V_G voltage required to get maximum gain) is 0.5V (V_S = ±2.5V) compared to 1.0V for V_S = ±5V. At the same time, gain cut-off (V_{G_MIN}) would shift to –0.5V from - 1V with V_S = ±5V.

Table 1 shows the approximate expressions for various V_G voltages as a function of V^-:

Table 1: V_G Definition Based on V^-

V_G	Definition	Expression (V)
V_{G_MIN}	Gain Cut-off	0.2 x V^-
V_{G_MID}	$A_{VMAX}/2$	0
V_{G_MAX}	A_{VMAX}	–0.2 x V^-

b) V_{G_LIMIT} (maximum permissible voltage on V_G) is reduced. This is due to limitations within the device arising from transistor headroom. Beyond this limit, device performance will be affected (non-destructive). Referring to *Figure 9*, note that with V^+ = 2.5V, and V^- = –4V, V_{G_LIMIT} is approaching V_{G_MAX} and already "Max gain" is reduced by 1dB. This means that operating under these conditions has reduced the maximum permissible voltage on V_G to a level below what is needed to get Max gain. If supply voltages are asymmetrical, reference *Figure 9* and *Figure 10* plots to make sure the region of operation is not overly restricted by the "pinching" of V_{G_LIMIT}, and V_{G_MAX} curves.

c) "Max_gain" reduces. There is an intrinsic reduction in max gain when the total supply voltage is reduced (see Typical Performance Characteristics plots for Gain vs. V_G (V_S = ±2.5V). In addition, there is the more drastic mechanism described in "b" above and shown in *Figure 9*.

Similar plots for V^+ = 5V operation are shown in *Figure 10* for comparison and reference.

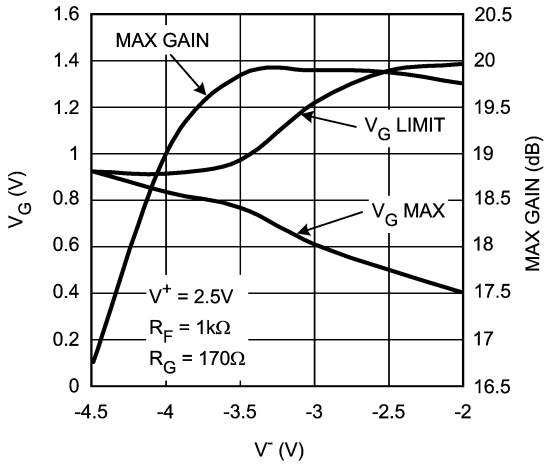


FIGURE 9. V_{G_MAX}, V_{G_LIMIT}, & Max-gain vs. V^- (V^+ = 2.5V)

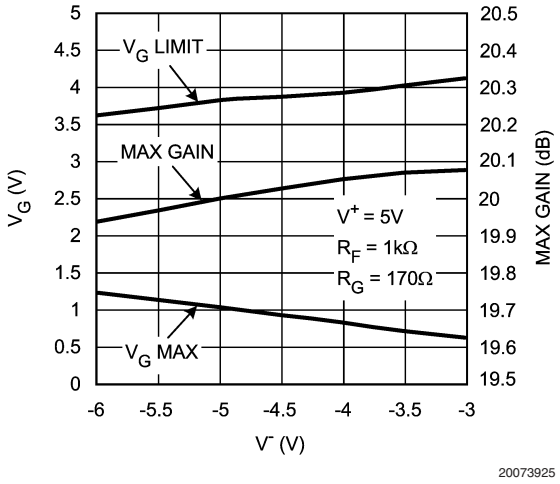


FIGURE 10. V_{G_MAX}, V_{G_LIMIT}, & Max-gain vs. V^- (V^+ = 5V)

Application Circuits

FOUR-QUADRANT MULTIPLIER

Applications requiring multiplication, squaring or other non-linear functions can be implemented with four-quadrant multipliers. The LMH6503 implements a four-quadrant multiplier as illustrated in *Figure 11*:

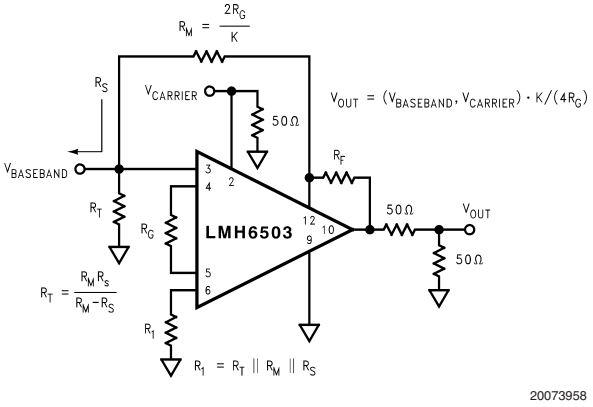


FIGURE 11. Four Quadrant Multiplier

FREQUENCY SHAPING

Frequency shaping and bandwidth extension of the LMH6503 can be accomplished using parallel networks connected across the R_G ports. The network shown in the *Figure 12* schematic will effectively extend the LMH6503's bandwidth.

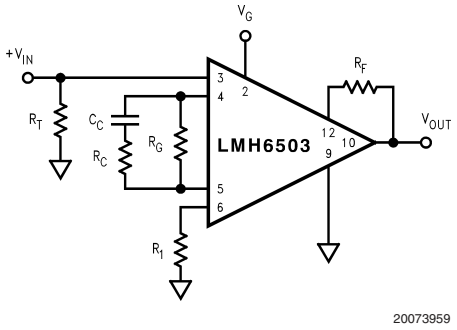
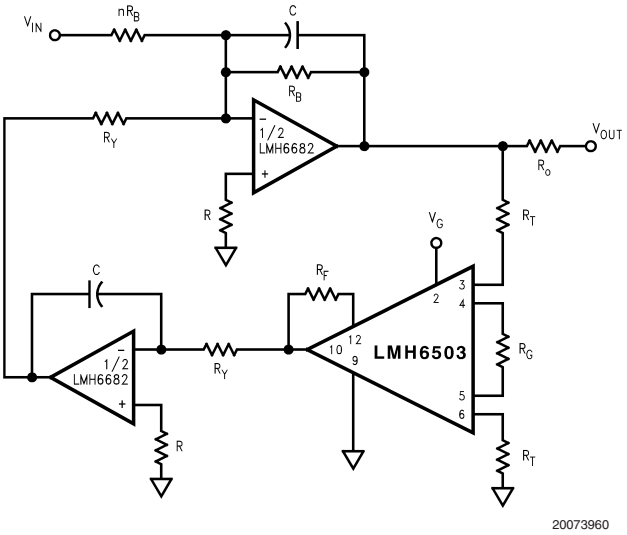


FIGURE 12. Frequency Shaping

2nd ORDER TUNABLE BANDPASS FILTER

The LMH6503 Variable-Gain Amplifier placed into a feedback loop provides signal processing function such as in a 2nd order tunable bandpass filter. The center frequency of the 2nd order bandpass shown in *Figure 13* is adjusted through the use of the LMH6503's gain control voltage, V_G. The integrators implemented with two sections of a LMH6682, provide the coefficients for the transfer function.



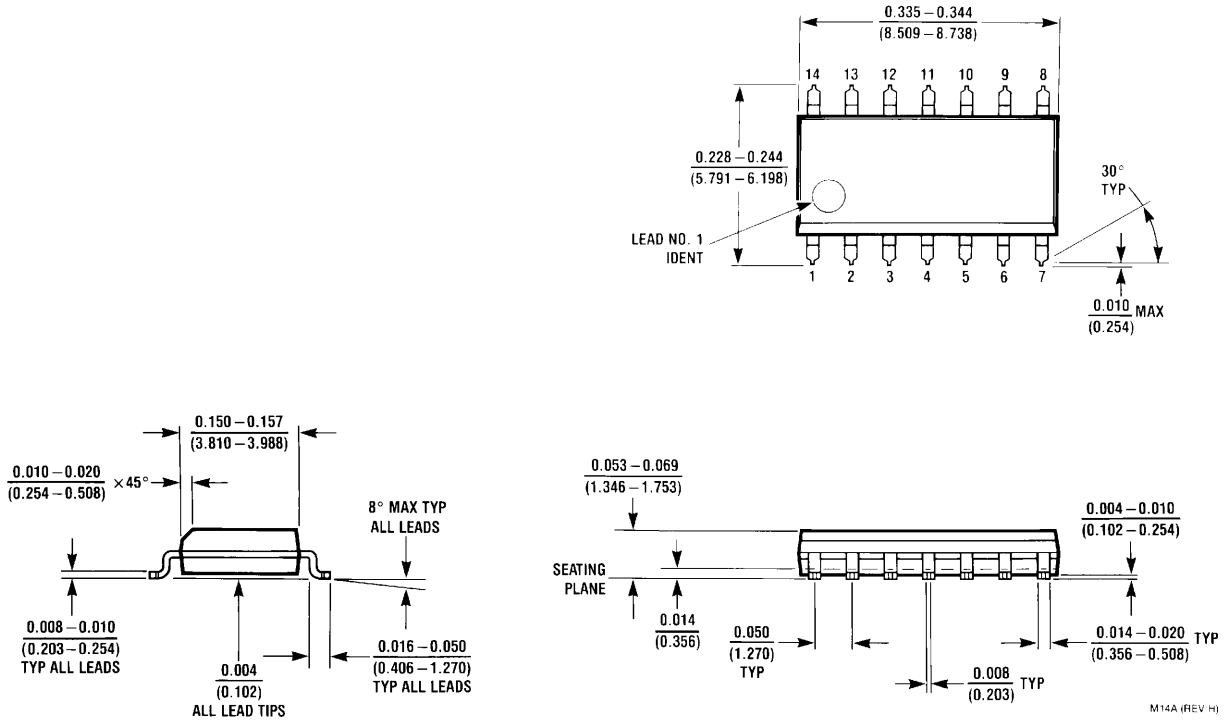
$$\frac{V_O}{V_{IN}} = \left[-\frac{1}{n}\right] \frac{s\frac{1}{CR_B}}{s^2 + s\frac{1}{CR_B} + \frac{p}{C^2R_Y^2}}$$

$$p = 1.72\,\frac{R_F}{R_Y},\ Q = \frac{\sqrt{pR_B}}{R_Y},\ \omega_O = \frac{\sqrt{p}}{CR_Y}$$

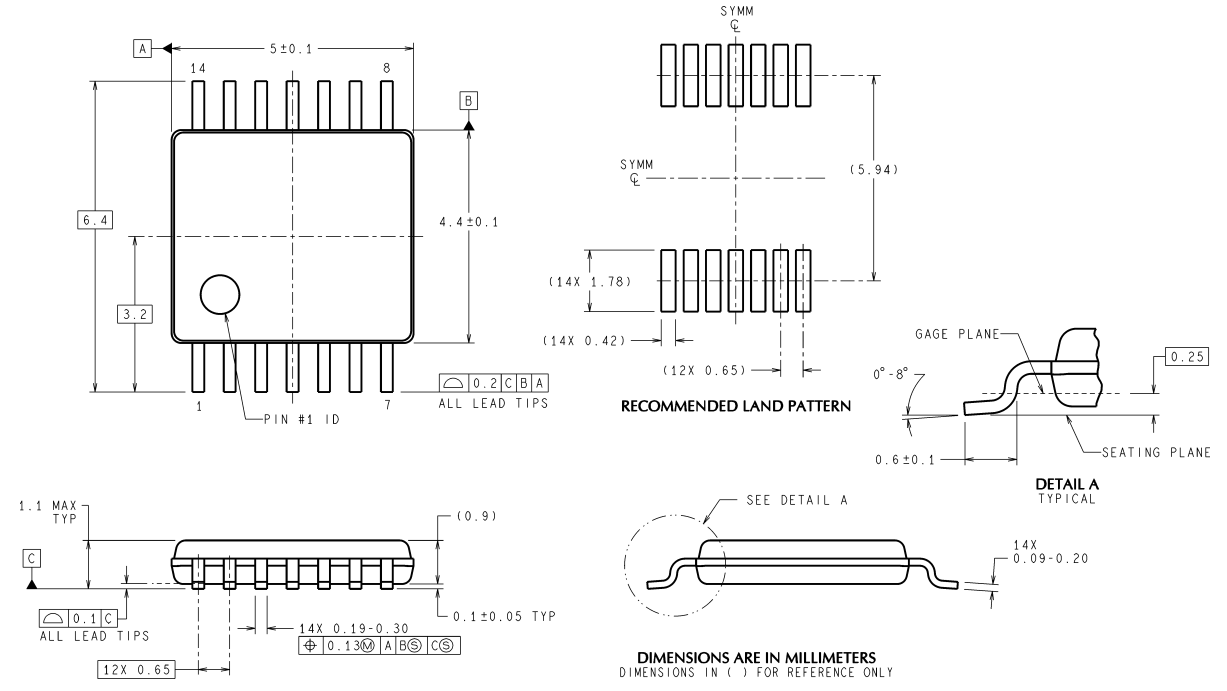
20073961

FIGURE 13. Tunable Bandpass Filter

Physical Dimensions inches (millimeters) unless otherwise noted



14-Pin SOIC
NS Package Number M14A



14-Pin TSSOP
NS Package Number MTC14

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