

SN74LS640, SN74LS641, SN74LS642, SN74LS645

Octal Bus Transceivers

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input (\bar{G}) can disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION	
\bar{G}	DIR	LS640 LS642	LS641 LS645
L	L	\bar{B} data to A bus	B data to A bus
L	H	\bar{A} data to B bus	A data to B bus
H	X	Isolation	Isolation

H = HIGH Level, L = LOW Level, X = Irrelevant

GUARANTEED OPERATING RANGES (SN74LS640, SN74LS645)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-3.0	mA
				-15	mA
I_{OL}	Output Current – Low			24	mA

GUARANTEED OPERATING RANGES (SN74LS641, SN74LS642)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
V_{OH}	Output Voltage – High			5.5	V
I_{OL}	Output Current – Low			24	mA

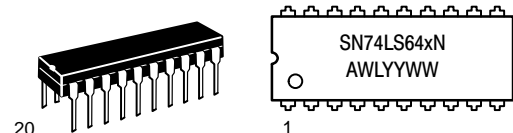


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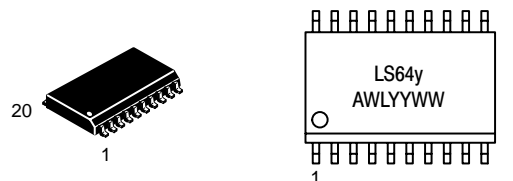
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LOW POWER SCHOTTKY

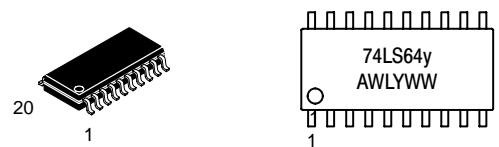
MARKING DIAGRAMS



PDIP-20
N SUFFIX
CASE 738



SOIC-20
DW SUFFIX
CASE 751D



SOEIAJ-20
M SUFFIX
CASE 967

x = 0, 1, 2, or 5
y = 0, 1, or 2
A = Assembly Location
WL = Wafer Lot
Y, YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

CONNECTION DIAGRAMS DIP (TOP VIEW)

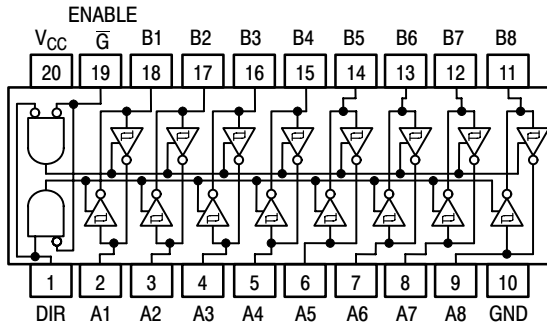


Figure 1. SN74LS640
SN74LS642

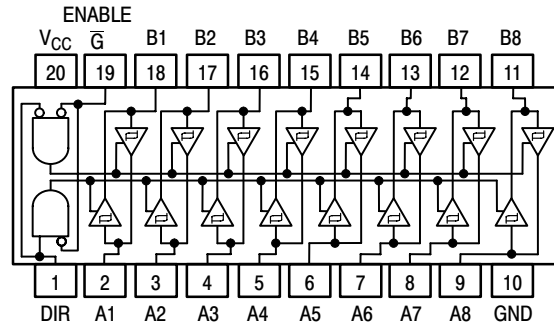


Figure 2. SN74LS641
SN74LS645

SN74LS640 • SN74LS645

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	3.4		V	V _{CC} = MIN, I _{OH} = 3.0 mA
		2.0			V	V _{CC} = MIN, I _{OH} = MAX
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 12 mA
			0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW			-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current	A or B, DIR or \overline{G}		20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		DIR or \overline{G}		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		A or B		0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current (Note 1)	-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current					
	Total Output HIGH			70	mA	V _{CC} = MAX
	Total, Output LOW			90		
Total at HIGH Z			95			

1. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS640			LS645				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay A to B		6.0	10		8.0	15	ns	C _L = 45 pF, R _L = 667 Ω
			8.0	15		11	15		
t _{PLH} t _{PHL}	Propagation Delay B to A		6.0	10		8.0	15		
			8.0	15		11	15		
t _{PZL} t _{PZH}	Output Enable Time \overline{G} , DIR to A		31	40		31	40		
			23	40		26	40		
t _{PZL} t _{PZH}	Output Enable Time \overline{G} , DIR to B		31	40		31	40		
			23	40		26	40		
t _{PLZ} t _{PHZ}	Output Disable Time \overline{G} , DIR to A		15	25		15	25	ns	C _L = 5.0 pF
			15	25		15	25		
t _{PLZ} t _{PHZ}	Output Disable Time \overline{G} , DIR to B		15	25		15	25		
			15	25		15	25		

SN74LS641 • SN74LS642

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.6	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current			100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 12 mA
			0.35	0.5	V	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				-0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current Total, Output HIGH			70	mA	V _{CC} = MAX
	Total, Output LOW			90		
	Total at HIGH Z			95		

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS641			LS642				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, B to A		17 16	25 25		19 14	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, \bar{G} , DIR to A		23 34	40 50		26 43	40 60	ns	
t _{PLH} t _{PHL}	Propagation Delay, \bar{G} , DIR to B		25 37	40 50		28 39	40 60	ns	

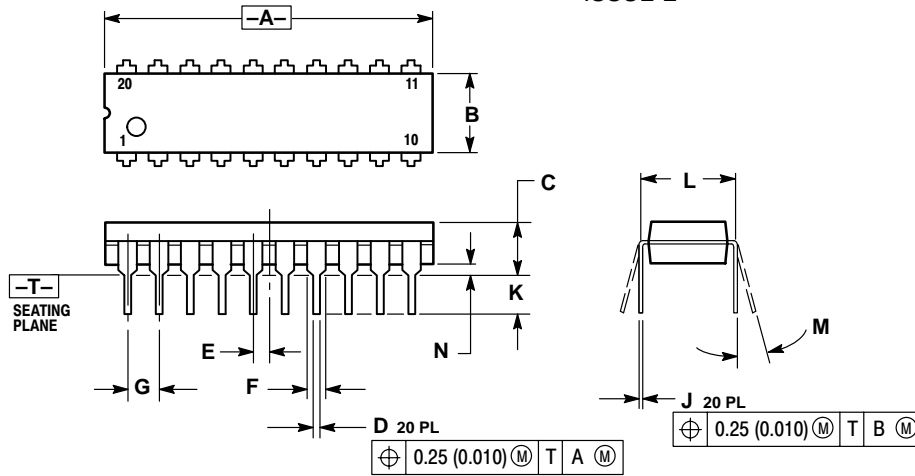
DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size
SN74LS640N	PDIP-20	1440 Units/Box
SN74LS640DW	SOIC-WIDE	2500/Tape and Reel
SN74LS640DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS640M	SOEIAJ-20	See Note 2
SN74LS640MEL	SOEIAJ-20	See Note 2
SN74LS641N	PDIP-20	1440 Units/Box
SN74LS641DW	SOIC-WIDE	2500/Tape and Reel
SN74LS641DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS641M	SOEIAJ-20	See Note 2
SN74LS641MEL	SOEIAJ-20	See Note 2
SN74LS642N	PDIP-20	1440 Units/Box
SN74LS642DW	SOIC-WIDE	2500/Tape and Reel
SN74LS642DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS642M	SOEIAJ-20	See Note 2
SN74LS642MEL	SOEIAJ-20	See Note 2
SN74LS645N	PDIP-20	1440 Units/Box

2. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

PACKAGE DIMENSIONS

N SUFFIX PLASTIC PACKAGE CASE 738-03 ISSUE E



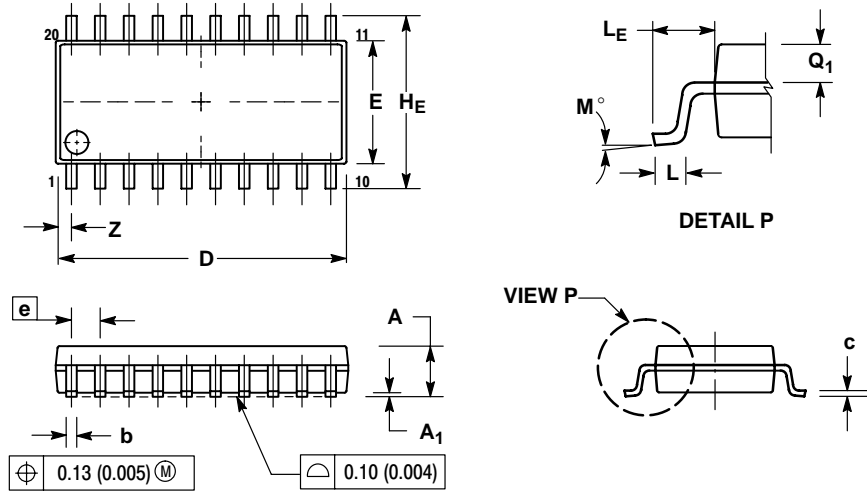
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

M SUFFIX SOEIAJ PACKAGE CASE 967-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	----	2.05	----	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	----	0.81	----	0.032

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