

BUK71/7908-40AIE

TrenchPLUS standard level FET

Rev. 02 — 24 October 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance, TrenchPLUS current sensing and diodes for ESD protection.

1.2 Features

- ESD protection
- Integrated current sensor
- Q101 compliant
- Standard level compatible.

1.3 Applications

- Variable Valve Timing for engines
- Electrical Power Assisted Steering.

1.4 Quick reference data

- $V_{DS} \leq 40$ V
- $I_D \leq 117$ A
- $R_{DSon} = 6$ m Ω (typ)
- $I_D/I_{sense} = 500$ (typ).

2. Pinning information

Table 1: Pinning - SOT426 and SOT263B, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	sense current (I_{sense})		
3	drain (d)		
4	Kelvin source		
5	source (s)		
mb	mounting base; connected to drain (d)		
		SOT426 (D2-PAK)	SOT263B (TO-220AB)



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
BUK7108-40AIE	D ² -PAK	Plastic single-ended surface mounted package; 5 leads (one lead cropped)	SOT426
BUK7908-40AIE	TO-220	Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-leads	SOT263B

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	40	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; Figure 2 and 3	[1] -	117	A
			[2] -	75	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; Figure 2	[2] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; Figure 3	-	468	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Figure 1	-	221	W
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA
		$t_p = 5 \text{ ms}$; $\delta = 0.01$	-	50	mA
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$
T_j	junction temperature		-55	+175	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1] -	117	A
			[2] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	468	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75 \text{ A}$; $V_{DS} \leq 40 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \text{ }\Omega$; starting $T_j = 25 \text{ }^\circ\text{C}$	-	0.63	J
Electrostatic discharge					
V_{esd}	electrostatic discharge voltage; all pins	Human Body Model; $C = 100 \text{ pF}$; $R = 1.5 \text{ k}\Omega$	-	6	kV

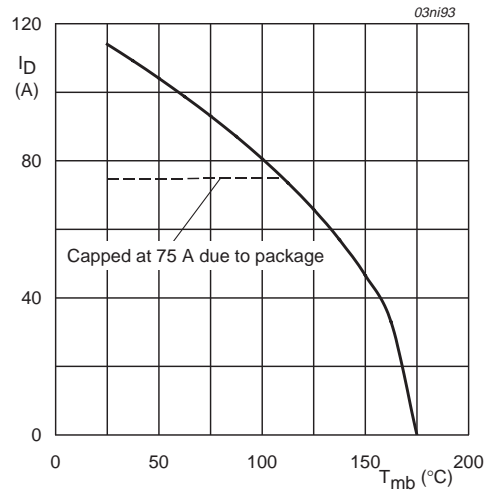
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



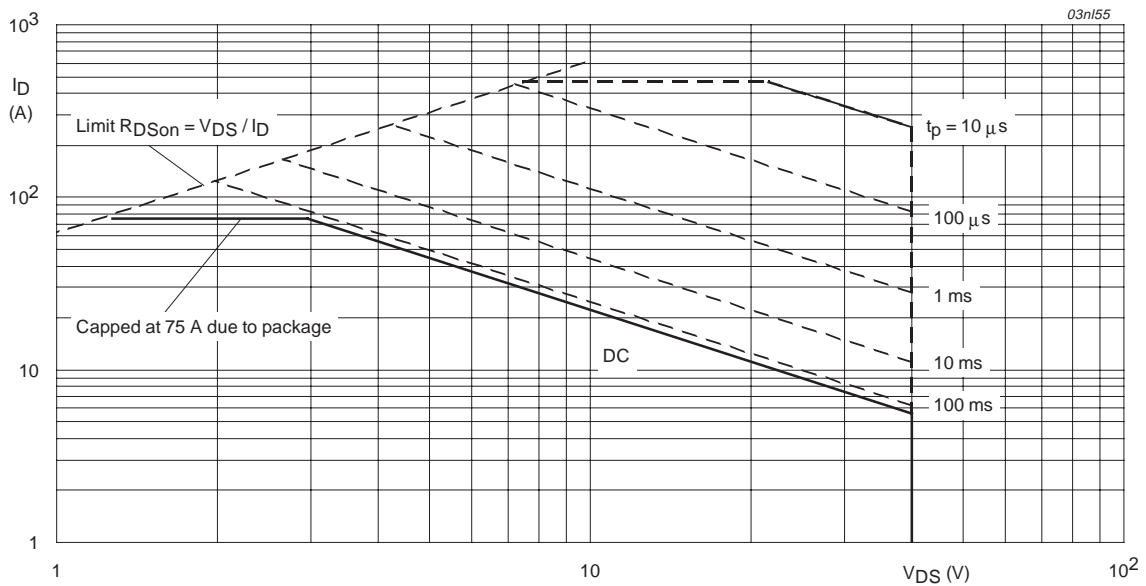
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT263B	vertical in still air	-	60	-	K/W
	SOT426	minimum footprint; mounted on a PCB	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.68	K/W

5.1 Transient thermal impedance

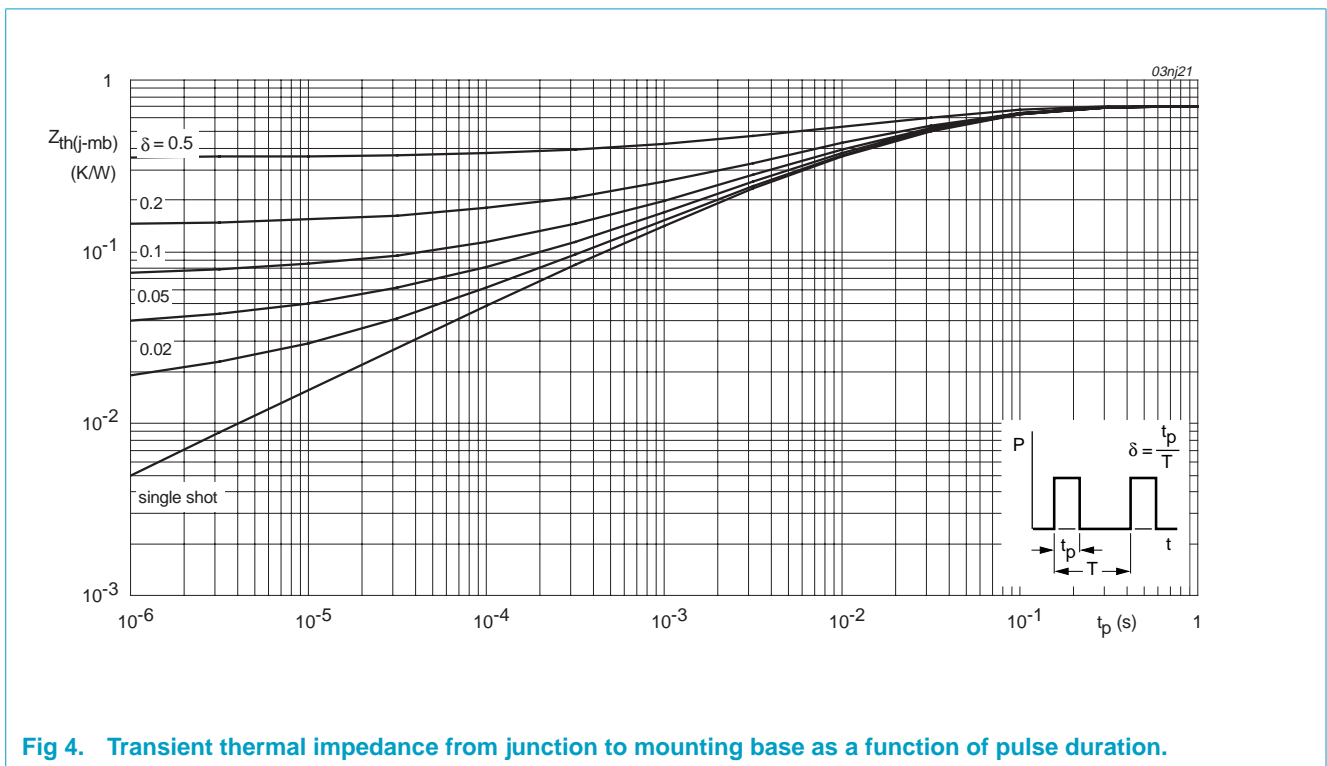


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

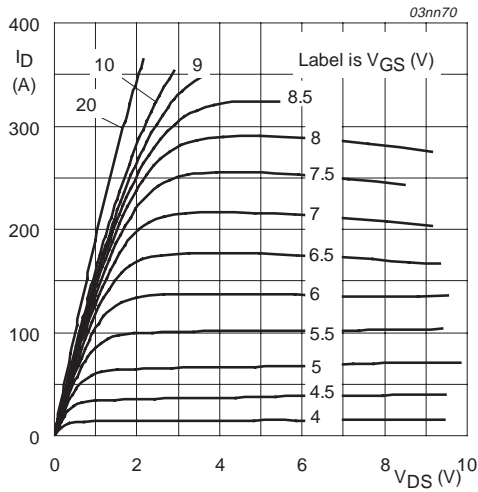
6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	40	-	-	V
		$T_j = -55\text{ °C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 40\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.1	10	μA
		$T_j = 175\text{ °C}$	-	-	250	μA
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$ $-55\text{ °C} < T_j < 175\text{ °C}$	20	22	-	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	22	300	nA
		$T_j = 175\text{ °C}$	-	-	10	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 50\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	6	8	m Ω
		$T_j = 175\text{ °C}$	-	-	15.2	m Ω
$R_{D(I_s)on}$	drain- I_{sense} on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ mA};$ Figure 16				
		$T_j = 25\text{ °C}$	1.59	1.87	2.20	Ω
		$T_j = 175\text{ °C}$	3.02	3.55	4.18	Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} > 10\text{ V}; R_{sense} = 0\text{ }\Omega;$ $-55\text{ °C} < T_j < 175\text{ °C}$	450	500	550	
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; V_{DS} = 32\text{ V};$	-	78	84	nC
Q_{gs}	gate-source charge	$I_D = 25\text{ A};$ Figure 14	-	14	16	nC
Q_{gd}	gate-drain (Miller) charge		-	34	36	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$	-	2670	3140	pF
C_{oss}	output capacitance	$f = 1\text{ MHz};$ Figure 12	-	900	1053	pF
C_{rss}	reverse transfer capacitance		-	560	653	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	-	19	-	ns
t_r	rise time	$V_{GS} = 10\text{ V}; R_G = 10\text{ }\Omega$	-	76	-	ns
$t_{d(off)}$	turn-off delay time		-	121	-	ns
t_f	fall time		-	122	-	ns

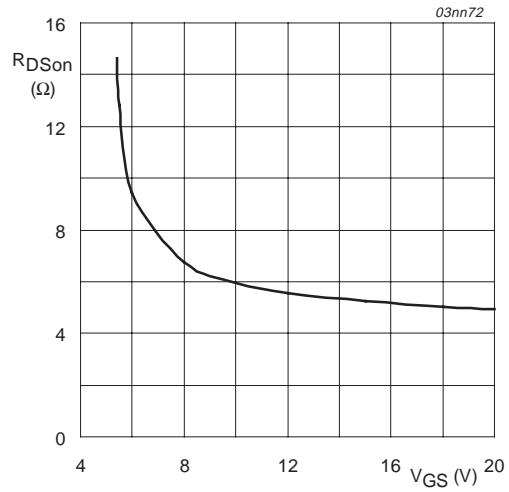
Table 5: Characteristics...continued*T_j = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L _d	internal drain inductance	measured from upper edge of drain mounting base to center of die	-	2.5	-	nH
L _s	internal source inductance	measured from source lead to source bond pad; lead length 6 mm	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 40 A; V _{GS} = 0 V; Figure 17	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs	-	55	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V	-	30	-	nC



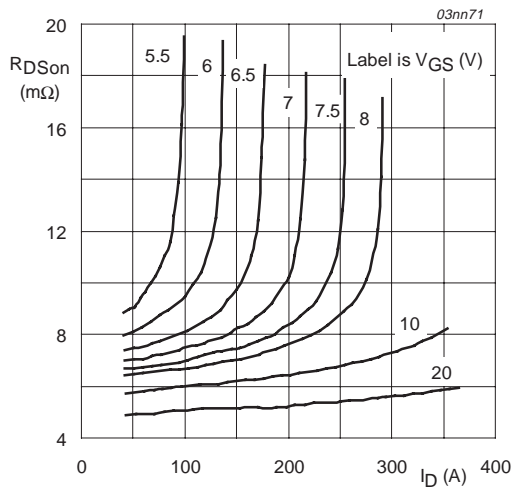
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



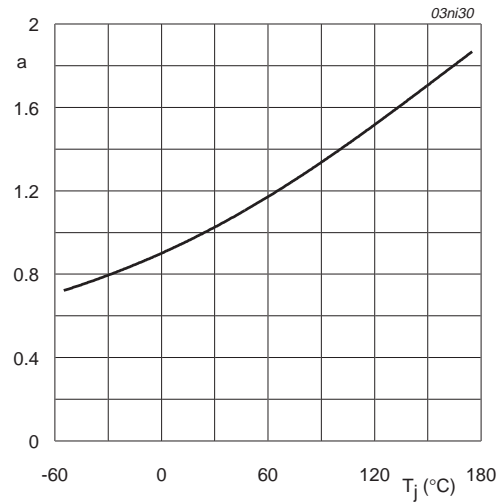
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 50\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



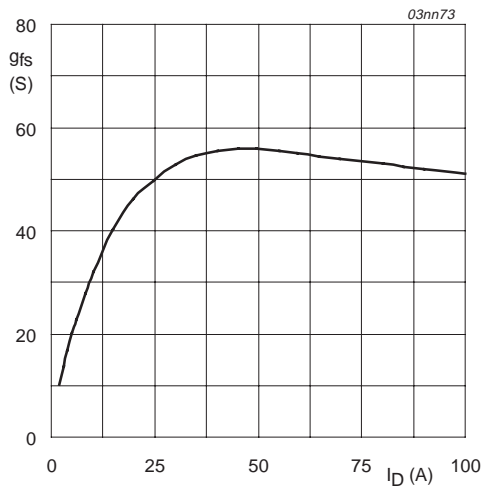
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



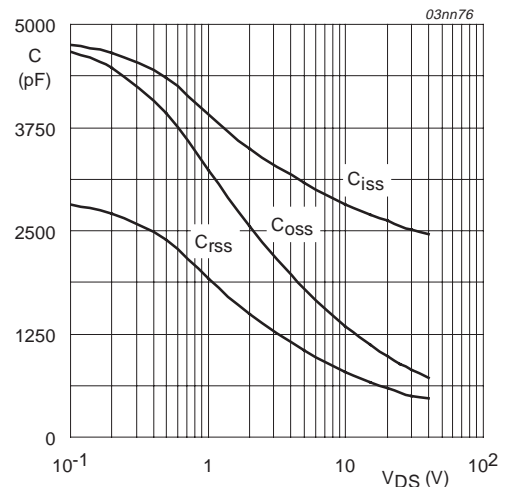
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



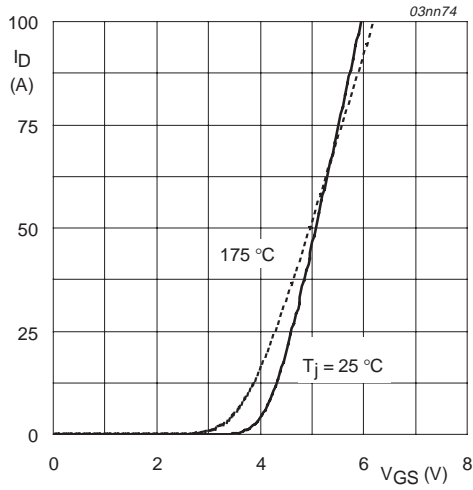
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



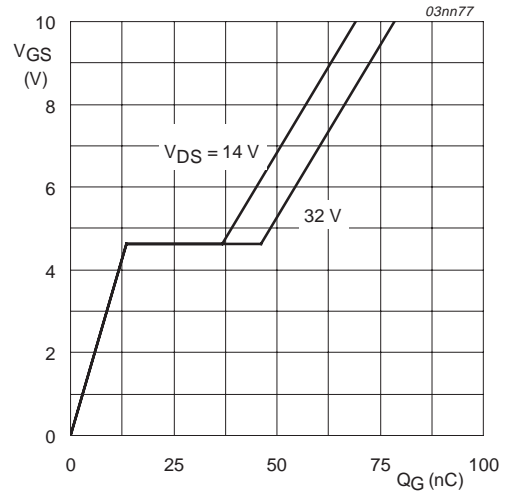
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



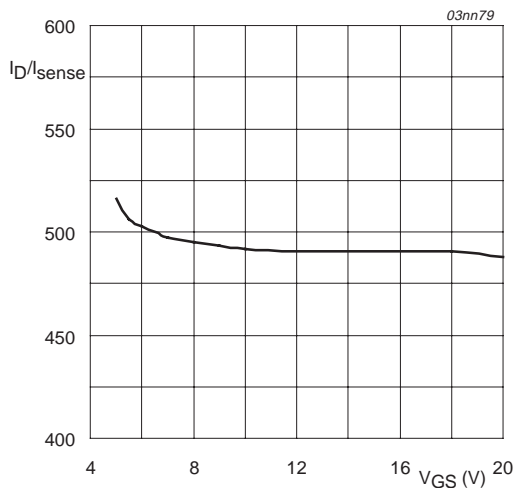
$V_{DS} = 25$ V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



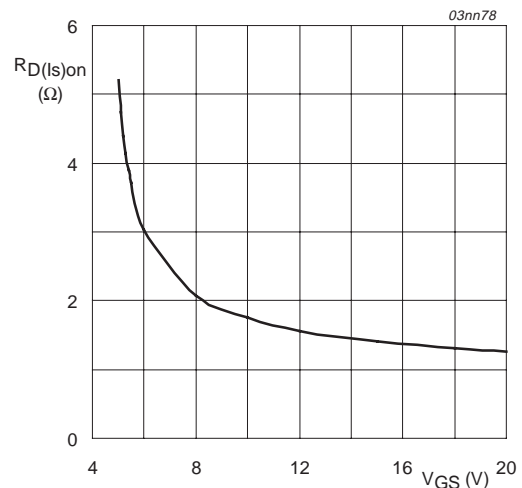
$T_j = 25$ °C; $I_D = 25$ A

Fig 14. Gate-source voltage as a function of gate charge; typical values.



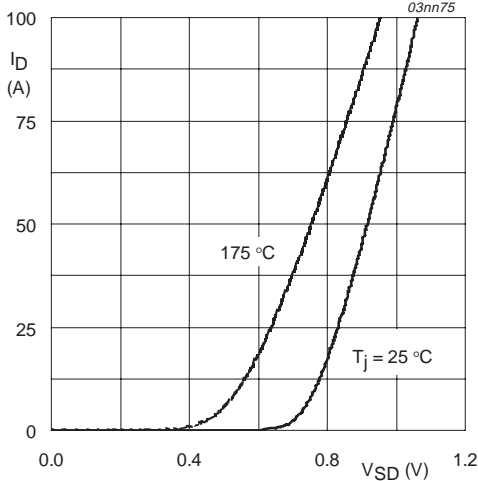
$I_D = 25$ A; $R_{sense} = 0$ Ω

Fig 15. Drain-sense current ratio as a function of gate-source voltage; typical values.



$I_{sense} = 25$ mA

Fig 16. Drain- I_{sense} on-state resistance as function of gate-source voltage; typical values.



$V_{GS} = 0\text{ V}$

Fig 17. Drain current as a function of source-drain diode voltage; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 5 leads (one lead cropped)

SOT426

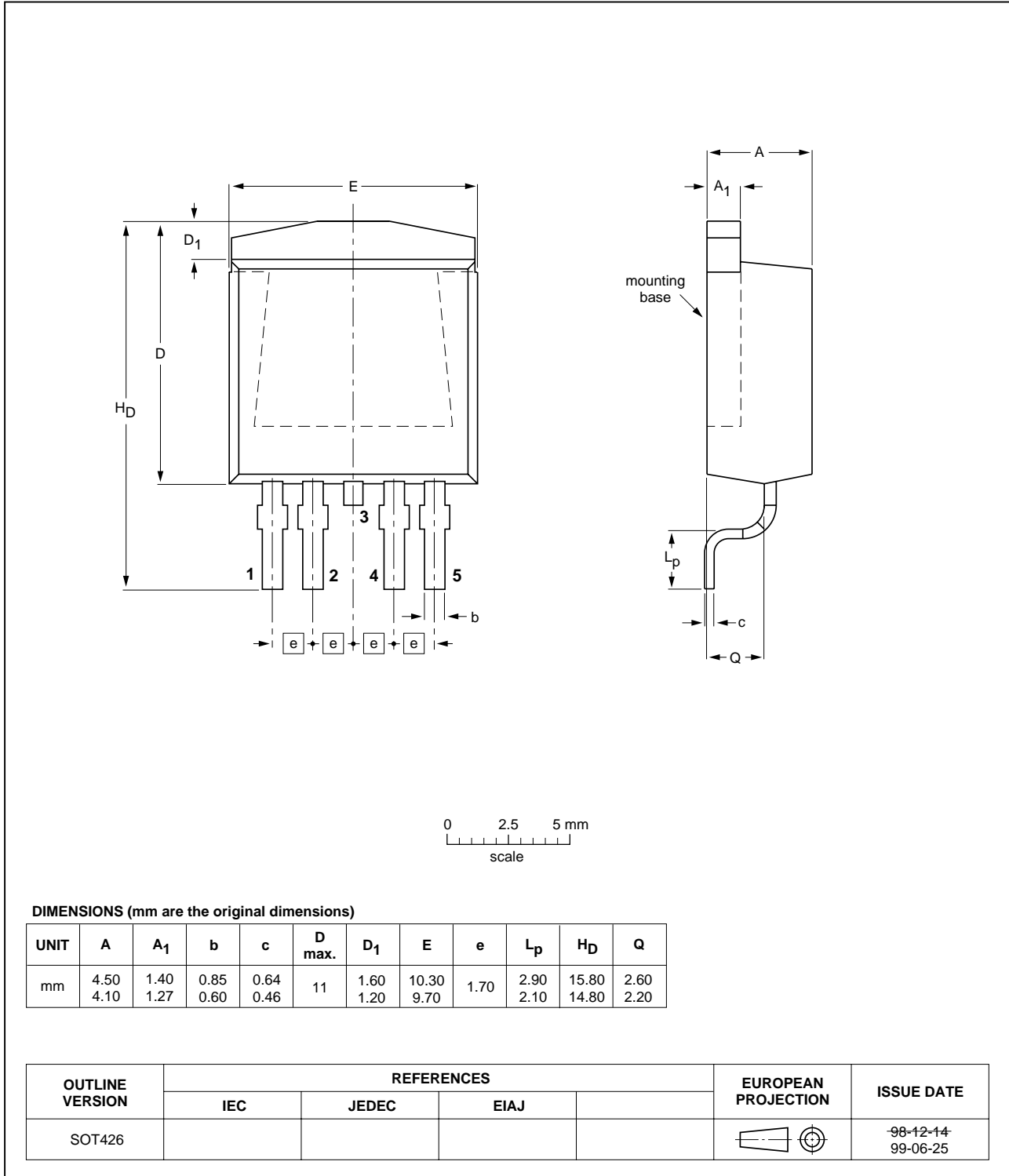


Fig 18. SOT426 (D²-PAK).

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220

SOT263B

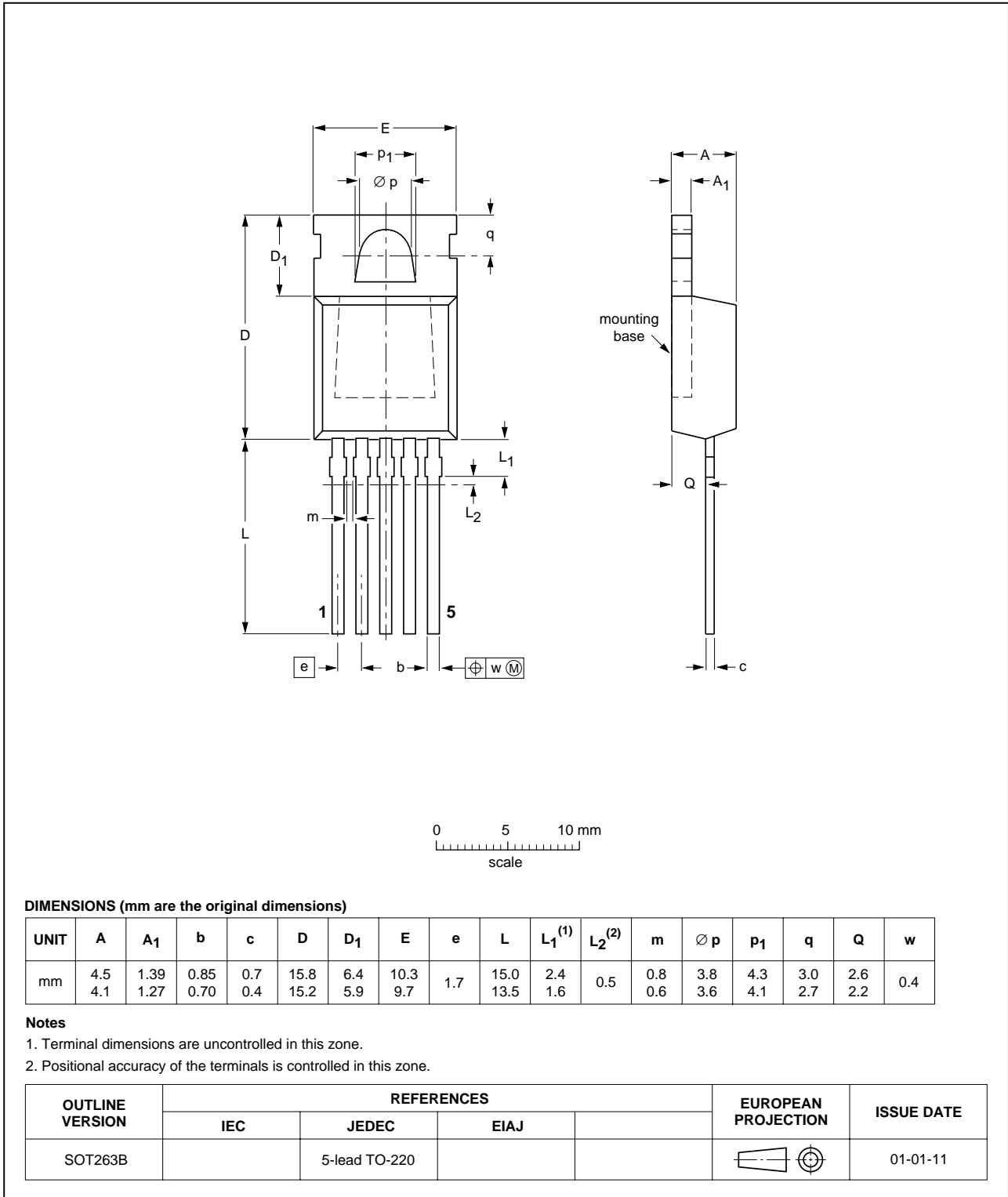
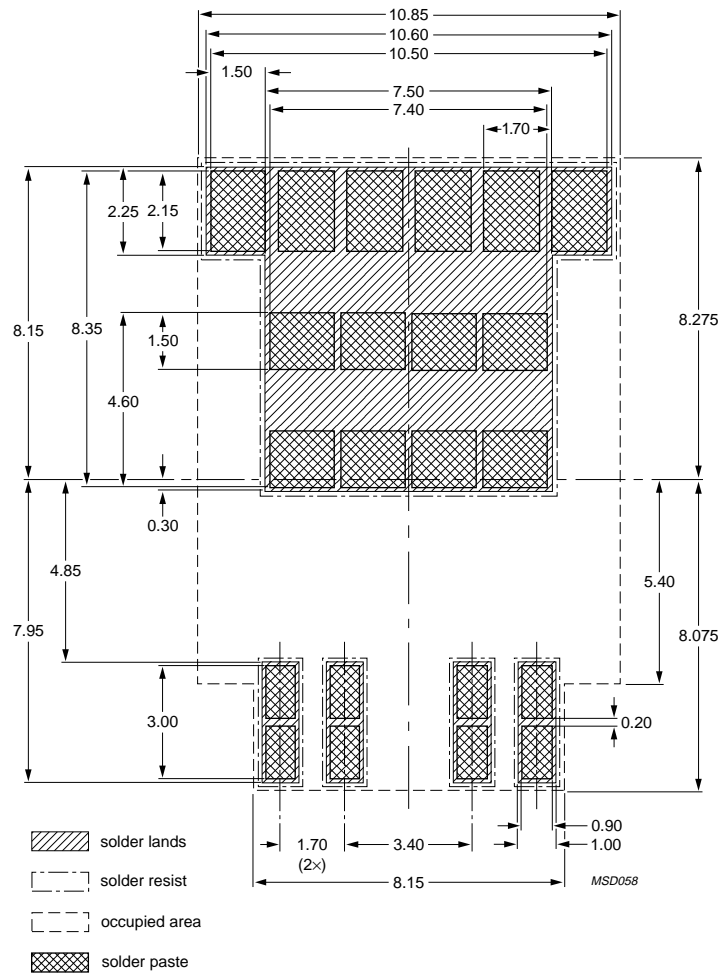


Fig 19. SOT263B (TO-220).

8. Soldering



Dimensions in mm.

Fig 20. Reflow soldering footprint for SOT426.

9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20031024	-	Product data; (9397 750 12086) Modifications: <ul style="list-style-type: none">• I_{GSS} limit changed in Table 5• Section 3 “Ordering information” added• Correction to title of Figure 19
01	20030819	-	Product data; (9397 750 11695)

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

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