R2020C
Data Sheet
FAST ETHERNET RISC PROCESSOR

RDC ***RISC DSP Communication***

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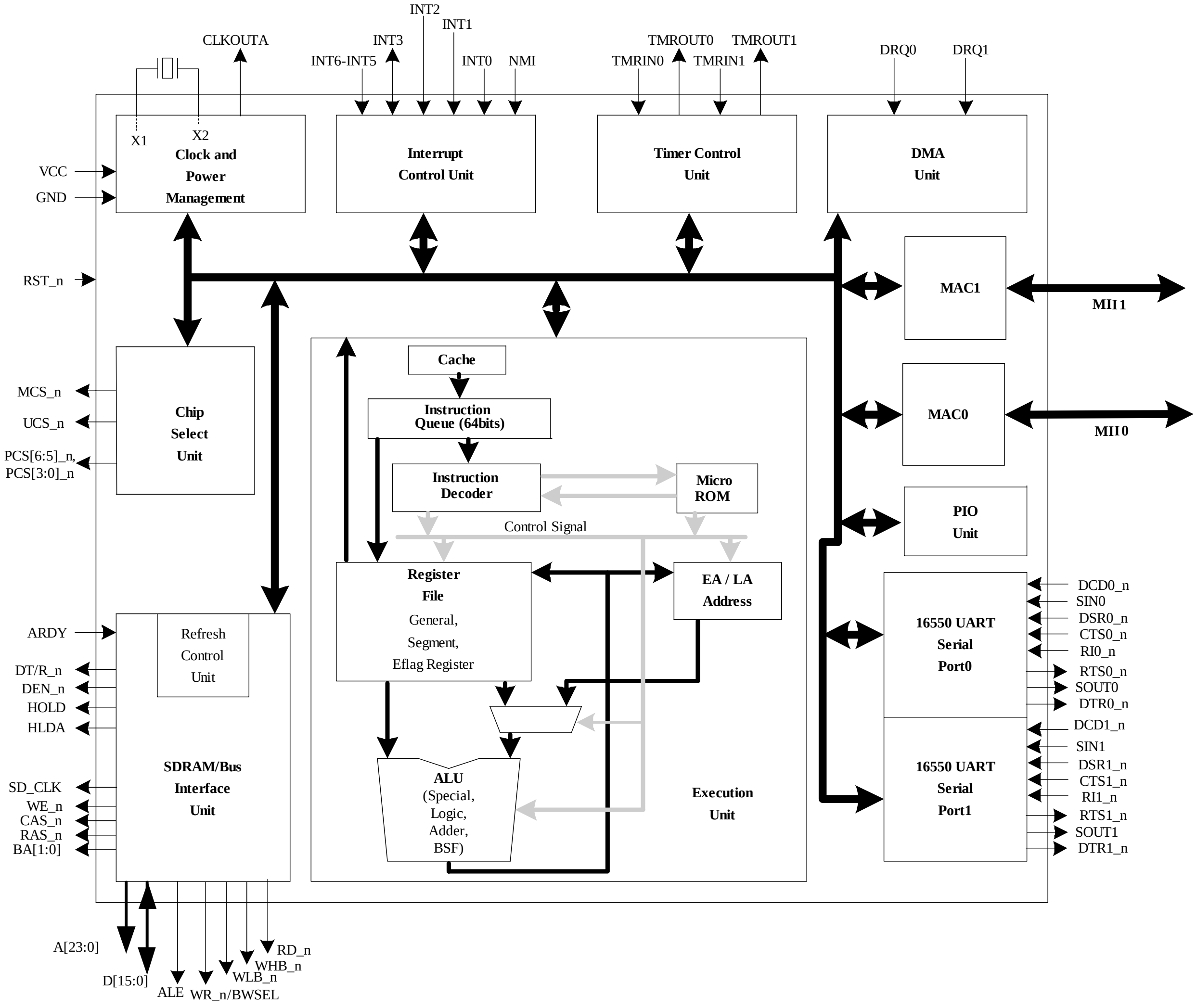
1. Features

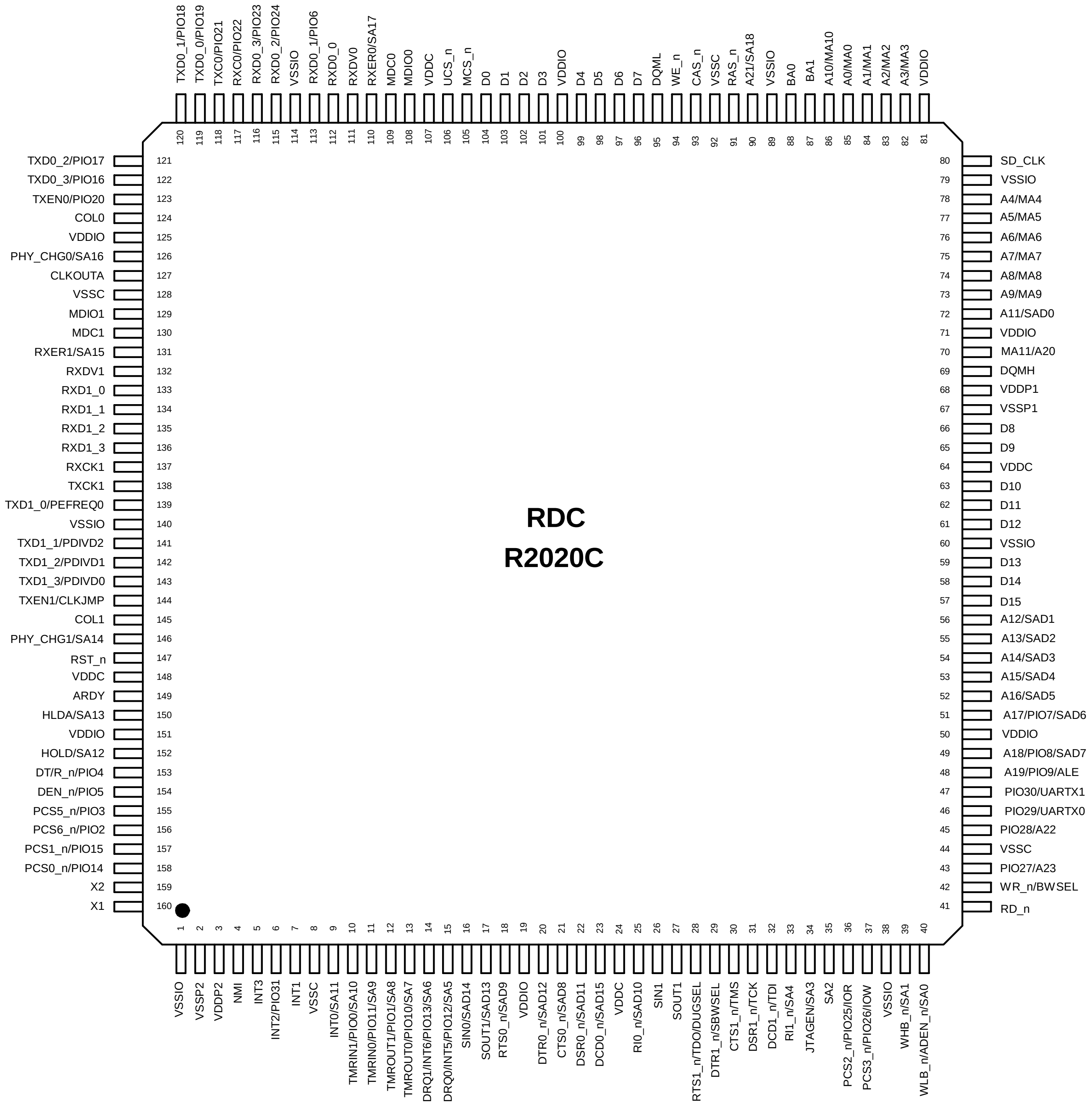
- Five-stage pipeline
- RISC architecture
- Bus interface
  - Multiplexed address and Data bus
  - Supports non-multiplexed address bus A [23:0]
  - 8-bit or 16-bit external bus dynamic access
  - 16M-byte memory address space
  - 64K-byte I/O space
  - Supports an independent data/address bus for external I/O device
- Supports two compatible UART serial channels with 16-byte FIFO and hardware flow-control.
- Supports CPU ID
- Supports a glueless and simplified 16-bit PCMCIA bus interface
- Supports 32 PIO pins
- SDRAM control Interface
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with six maskable external interrupts and one non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- With 8-bit or 16-bit Boot ROM bus size
- 2-Port Fast Ethernet MAC with MII interface
- Supports an 8K-byte Uniform cache
- With 25MHz input frequency and up to 100MHz maximum internal frequency.
- Compatible with 3.3V I/O and 2.5V core voltage.
- Package Type includes 160-pin PQFP.

2. Block Diagram



3. Pin Description

3.1 Pin Placement



3.2 Functional Description

I = Input;

O = Output;

PU = Pull up 75KΩ;

PD = Pull down 75KΩ;

PU* = Pull up 75KΩ when the PIOn pin is used;

PD* = Pull down 75KΩ when the PIOn pin is used;

- **CPU Core**

PIN No.	Symbol	Type	Description
147	RST_n	I/PU	Reset input with Schmitt trigger. When RST_n is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and changes the address to the reset address FFFF00h.
160	X1	I	25MHz frequency input, <u>within 100 ppm tolerance</u>, to the amplifier (oscillator).
159	X2	O	Frequency output from the inverting amplifier (oscillator).
127	CLKOUTA	O	The CLKOUTA output frequency is the same as the X1 input frequency. When high, the CLKOUTA is from Multiple-PLL. When low, the CLKOUTA is from X1.

Bus Interface

PIN No.	Symbol	Type	Description
39	WHB_n/SA1	O	Write high byte. This pin indicates that the high byte data (D[15:8]) on the bus is to be written to a memory or an I/O device. This pin floats during reset or bus hold conditions. SA1: The slow bus address 1
40	WLB_n/SA0	O/PU	Write low byte. This pin indicates that the low byte data (D[7:0]) on the bus is to be written to a memory or an I/O device. This pin floats during reset or bus hold conditions. **This pin must be pulled low.** SA0: The slow bus address 0
41	RD_n	O	Read Strobe. One active low signal indicates that the microcontroller is performing a memory or I/O read cycle. The RD_n floats during a bus hold or reset.
42	WR_n/BWSEL	O/PU	Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. WR_n is active during T2, T3, and Tw of any write cycle, floating during a bus hold or reset. BWSEL is used to decide the boot ROM bus width when RST_n goes from low to high. If BWSEL is with an external pull-low resistor (4.7k ohm), the boot ROM bus width is 8 bits. Otherwise the boot ROM width is 16 bits.

149	ARDY	I/PU	Asynchronous ready. This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge of input that is asynchronous to SD_CLK and is active high. However, the falling edge of ARDY must be synchronized to SD_CLK. Tie ARDY high, so the microcontroller is always asserted in the ready condition. To guarantee the wait states inserted, ARDY must be pulled low before to phase 2 of T2 or phase 1 of T3. Please note that the ARDY signal is internally pulled high.
48 49 51 52 53 54 55 56 72 86 73 74 75 76 77 78 82 83 84 85	A19/PIO9/ALE A18/PIO8/SAD7 A17/ PIO7/SAD6 A16/SAD5 A15/SAD4 A14/SAD3 A13/SAD2 A12/SAD1 A11/SAD0 A10/MA10 A9/MA9 A8/MA8 A7/MA7 A6/MA6 A5/MA5 A4MA4 A3/MA3 A2/MA2 A1/MA1 A0/MA0	I/O	Address bus. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset. SAD [7:0]: The combination pins with addresses and data. They are designed for slower peripheral bus. ALE: Address latch enable. Active high. This pin indicates an address output on the D bus. Address is guaranteed to be valid on the trailing edge of ALE. MA [10:0]: The SDRAM raw and column address output.
104 103 102 101 99 98 97 96 66 65 63 62 61 59 58 57	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	I/O	Data bus for memory or I/O access. The D bus is in a floating state during a bus hold or reset condition and this bus can also be used to load system configuration information (with pull-up or pull-low resistor) into the RESCON register when RST_n goes from low to high and the Watchdog timeout is reset.
150	HLDA/SA13	I/O	Bus Hold Acknowledge. Active high. The microcontroller will issue a HLDA in response to a HOLD request by external bus master at the end of T4 or Ti. When the microcontroller is in a hold state (HLDA is high), the D[15:0], A[19:0], WR_n, RD_n, DEN_n, DT/R_n, WHB_n and WLB_n are floating, and the UCS_n, PCS6_n – PCS5_n, MCS_n and PCS3_n – PCS0_n will

			be driven high. After HOLD is detected as being low, the microcontroller will lower HLDA. SA13: The slow bus address 13
152	HOLD/SA12	I/O/PD	Bus Hold request with internal pull-down resistor. Active high. This pin indicates that another bus master is requesting the local bus. If the external bus master has controlled the system bus, it must be responsible for SDRAM refresh operation SA12: The slow bus address 12
153	DT/R_n/PIO4	I/O/PU*	Data transmit or receive. This pin indicates the direction of data flow through an external data-bus transceiver. When DT/R_n is low, the microcontroller receives data. When DT/R is high, the microcontroller drives data to the data bus.
154	DEN_n/PIO5	I/O/PU*	Data Enable. This pin is provided as a data bus transceiver output enable. DEN_n is asserted during memory and I/O access. DEN_n is deserted when DT/R_n changes states. It floats during bus hold or reset conditions.
Chip Select Unit Interface			
PIN No.	**Symbol**	**Type**	**Description**
106	UCS_n	O/PU	Upper memory chip select. For UCS_n, this pin is active low when the system accesses the defined portion of the upper 8M bytes (800000-FFFFFF) memory block. UCS_n defaulted active address region is from FF0000h to FFFFFFh after power-on reset. The address range for UCS_n is programmed by software. This pin incorporates a weak pull-up resistor.
105	MCS_n	O/PU	Midrange Memory Chip Select For MCS_n feature, this pin is active low when the microcontroller accesses the defined portion of memory region.
156 155	PCS6_n/PIO2 PCS5_n/PIO3	I/O/PU*	Peripheral chip selects/latched address bit. For PCS_n feature, these pins are active low when the micro-controller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of PCS_n is programmable. These pins are asserted with the multiplexed D address bus and do not float during bus hold conditions.
157 158	PCS1_n/PIO15 PCS0_n/PIO14	I/O/PU*	Peripheral chip selects. These pins are active low when the microcontroller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 16M-Byte memory address region. These pins are asserted with the multiplexed D address bus and do not float during bus holds.
36 37	PCS2_n/PIO25/IOR_n PCS3_n/PIO26/IOW_n	I/O/PU*	Peripheral chip selects. These pins are active low when the micro controller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 16M-Byte memory address region. These pins are asserted with the multiplexed D address bus and do not float during bus holds. When register FFEAh bit is set, PIN36 is IOR_n and PIN37 is IOW_n. IOR_n/IOW_n are for PCMCIA bus.
Interrupt Control Unit Interface			
PIN No.	**Symbol**	**Type**	**Description**
4	NMI	I/PD	Non-maskable Interrupt. The NMI is the highest priority hardware

			interrupt and is non-mask able. When this pin is asserted (NMI transition from low to high), the micro controller always transfers the address bus to the location specified by the non-mask able interrupt vector in the micro controller interrupt vector table. The NMI pin must be asserted for at least one SD_CLK period to guarantee that the interrupt is recognized.
5	INT3	I/PD	Maskable Interrupt Request 3. It's active high. The interrupt input can be configured to be either edge-triggered or level-triggered. The requesting device must hold the INT3 until the request is acknowledged to guarantee interrupt recognition.
6	INT2/PIO31	I/O/PU*	Maskable Interrupt Request 2. Except the differences of the interrupt line and interrupt address vector, the function of INT2 is the same as that of INT3.
7	INT1	I/PD	Mask able Interrupt Request 1/slave select. For INT1, except the differences of the interrupt line and interrupt address vector, the function of INT1 is the same as that of INT3.
9	INT0/SA11	I/PD	Mask able interrupt request 0. Except the differences of the interrupt line and interrupt address vector, the function of INT0 is the same as that of INT3. SA11: The slow bus address 11

Timer Control Unit Interface

PIN No.	Symbol	Type	Description
10 11	TMRIN1/PIO0/SA10 TMRIN0/PIO11/SA9	I/O/PU*	Timer input. These pins can be used as clock or control signal input, depending upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. **These pins must be pulled up if not being used.** SA[10:9]: The slow bus address 10 and 9
12 13	TMROUT1/PIO1/SA8 TMROUT0/PIO10/SA7	I/O/PD*	Timer output. Depending on timer mode select. These pins provide single pulse or continuous waveform. The duty cycle of the waveform is programmable. These pins are floated during a bus hold or reset. SA[8:7]: The slow bus address 8 and 7

DMA Unit Interface

14 15	DRQ1/INT6/PIO13/SA6 DRQ0/INT5/PIO12/SA5	I/O/PU*	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until serviced. For INT6/INT5: When the DMA function is not used, the INT6 and INT5 can be used as an additional external interrupt request. And they share the corresponding interrupt type and register control bits. The INT6/5 are level-triggered only. SA[6:5]: The slow bus address 6 and 5

- **16550 UART**

PIN No.	Symbol	Type	Description
16	SIN0/SAD14	I/O/PU	SIN0: Serial Input. Serial Data Input from the communications link. SAD14: The combination pin with Address and Data. It is for slower device bus.
17	SOUT0/SAD13	I/O/PU	SOUT0: Serial Output. Composite serial data output to the communications link. SAD13: The combination pin with Address and Data. It is for slower device bus.
18	RTS0_n/SAD9	I/O/PU	RTS0_n: Request To Send. When low, this indicates to MODEM or data set that URAT is ready to exchange data. SAD9: The combination pin with Address and Data. It is for slower device bus.
20	DTR0_n/SAD12	I/O/PU	DTR0_n: Data Terminal Ready. When low, this informs the MODEM or data set that UART is ready to establish a communication link. SAD12: The combination pin with Address and Data. It is for slower device bus.
21	CTS0_n/SAD8	I/O/PU	CTS0_n: Clear To Send. When low, this indicates to UART that MODEM or data set is ready to exchange data. SAD8: The combination pin with Address and Data. It is for slower device bus.
22	DSR0_n/SAD11	I/O/PU	DSR0_n: Data Set Ready. When low, this indicates that MODEM or data set is ready to establish the communication link with UART. SAD11: The combination pin with Address and Data. It is for slower device bus.
23	DCD0_n/SAD15	I/O/PU	DCD0_n: Data Carry Detection. When low, it indicates that the data carrier has been detected by the MODEM or data set. SAD15: The combination pin with Address and Data. It is for slower device bus.
25	RI0_n /SAD10	I/O/PU	RI0_n: Ring Indicator. This indicates that a telephone-ringing signal has been received by the MODEM or data set. SAD10: The combination pin with Address and Data. It is for slower device bus.
26	SIN1	I	SIN1: Serial Data Input.
27	SOUT1	O	SOUT1: Serial Data Output. **This pin must be pulled low.**
28	RTS1_n/TDO	O	RTS1_n: Request To Send. TDO: JTAG test data output pin.
29	DTR1_n/SBWSEL	I/O/PU	DTR1_n: Data Terminal Ready. SBWSEL is to decide the SAD bus width when the RST_n pin goes from low to high. If SBWSEL is with a pull-low resistor (4.7k ohm), the SAD bus width is 8 bits and 16550's Port 0 is active. Otherwise the SAD bus width is 16 bits and 16550 Port 0 is inactive.
30	CTS1_n/TMS	I/PU	CTS1_n: Clear To Send. JTAG Test mode select pin
31	DSR1_n/TCK	I/PU	DSR1_n: Data Set Ready. TCK: JTAG test clock input pin

32	DCD1_n/TDI	I/PU	DCD1_n: Carry Sense Detection. TDI: JTAG test data input pin
33	RI1_n/SA4	I/O/PU	RI1_n: Ring Input. SA4: The slow bus address 4

- **MII Interface**

PIN No.	Symbol	Type	Description
122 121 120 119	TXD0_3/PIO16 TXD0_2/PIO17 TXD0_1/PIO18 TXD0_0/PIO19	I/O/PU*	Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal. PIO: General purpose PIN.
123	TXEN0/PIO20	I/O/PU*	This pin functions as transmit enable. It indicates that a transmission to an external PHY device is active on the MII port. PIO: General purpose PIN.
118	TXC0/PIO21	I/O	Supports the transmit clock supplied by the external PMD device. This clock should always be active. PIO: General purpose PIN.
117	RXC0/PIO22	I/O/PU*	Supports the receive clock supplied by the external PMD device. This clock should always be active.
116 115	RXD0_3/PIO23 RXD0_2/PIO24	I/O/PU*	Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal.
113	RXD0_1/PIO6	I/O/PU*	
112	RXD0_0	I/PD	
111	RXDV0	I/PD	Data valid is asserted by an external PHY when the received data is present on the RXD [3:0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
110	RXER0/SA17	I/PD	Receiver error shall be asserted to indicate to MAC that an error was detected. This signal should be synchronized with the RXC signal.
124	COL0	I/PD	This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
109	MDC0	O	MII management data clock is sourced by the R2020C to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
108	MDIO0	I/O/PD	MII management data input/output transfers control information and status between the external PHY and the R2020C.
143 139	TXD1_3/PDIVD0 TXD1_0/PEFREQ0	I/O/PU	Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal. PDIVD [2:0] & PFEREQ [0] are hardware configured pins during reset for Multiple PLL. (See Chapter.5) PDIVD [2:0]: Multiple selections. PFEREQ [0]: Input clock range selection.
142 141	TXD1_2/PDIVD1 TXD1_1/PDIVD2	I/O/PD	
144	TXEN1/CLKJMP	I/O/PD	This pin functions as transmit enable. It indicates that a transmission is active on the MII port to an external PHY device. CLKJMP: It is a hardware-configured pin, used to select the CLKOUTA output from internal Multiple PLL or X1. When high, the CLKOUTA is from Multiple-PLL. When low, the CLKOUTA is from X1.

138	TXC1	I/PD	Supports the transmit clock supplied by the external PMD device. This clock should always be active.
137	RXC1	I/PD	Supports the receive clock supplied by the external PMD device. This clock should always be active.
136 135 134 133	RXD1_3 RXD1_2 RXD1_1 RXD1_0	I/PD	Four parallel receive data lines. This data is driven by an external PHY that the media is attached and should be synchronized with the RXC signal.
132	RXDV1	I/PD	Data valid is asserted by an external PHY when the received data is present on the RXD1 [3:0] lines and is de-asserted at the end of the packet.
131	RXER1/SA15	I/PD	Receiver error shall be asserted to indicate to MAC that an error was detected. This signal should be synchronized with the RXC signal.
145	COL1	I/PD	This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
130	MDC1	O	MII management data clock is sourced by the R2020C to the external PHY devices as a timing reference for the information transfer on the MDIO signal.
129	MDIO1	I/O/PD	MII management data input/output transfers control information and status between the external PHY and the R2020C.
126	PHY_CHG0/SA16	I/O/PD	To indicate PHY status changed. SA16: The slow bus address 16
146	PHY_CHG1/SA14	I/O/PD	To indicate PHY status changed. SA14: The slow bus address 14

- **JTAG /SCAN Chain Enable Pin**

PIN No.	Symbol	Type	Description
34	JTAGEN/SA3	I/O/PD	JTAG function enable. Default is pulled low and disabled. SA3: The slow bus address 3
35	SA2	O/PD	SA2: The slow bus address 2

- **SDRAM Interface**

PIN No.	Symbol	Type	Description
80	SD_CLK	O	SDRAM clock output. This clock output is from internal De-skew PLL. It can be one to four multiple of input clock X1, depending on the setting of PFEREQ [0] during power-on resets.
70	MA11/A20	O	MA [11]: The SDRAM raw and column address output Address bus 20. SDRAM module CKE must be tied high.
90	A21/SA18	O	Address bus 21. SA18: the slow bus address 18.
94	WE_n	O	SDRAM/EDO write enable.
93	CAS_n	O	SDRAM column address selector.
91	RAS_n	O	SDRAM raw address selector.
88	BA0	O	SDRAM bank address 0.
87	BA1	O	SDRAM bank address 1.
95	DQML	O	Input/Output mask.
69	DQMH	O	Input/Output mask.

- **GPIO Interface**

PIN No.	Symbol	Type	Description
43	PIO27/A23	I/O/PU*	General purpose PIN/Address bus 23.
45	PIO28/A22	I/O/PU*	General purpose PIN/Address bus 22.
46	PIO29/UARTX0	I/O/PD*	General purpose PIN. UARTX0: URAT0 transmission indication for observation.
47	PIO30/UARTX1	I/O/PD*	General purpose PIN. UARTX1: URAT1 transmission indication for observation.

- **Power Pins**

PIN No.	Symbol	Type	Description
19,50,71,81,100,125,151	VDDIO	I	I/O power pin, pure 3.3V.
1,38,60,79,89,114,140	VSSIO	I	I/O ground pin.
24,64,107,148	VDDC	I	Core power pin, pure 2.5V.
8,44,92,128	VSSC	I	Core ground pin.
68	VDDP1	I	De-skew PLL power pin, pure 2.5V.
67	VSSP1	I	De-skew PLL ground pin.
3	VDDP2	I	Multiple PLL power pin, pure 2.5V.
2	VSSP2	I	Multiple PLL ground pin.

Notes:

1. When the PIO Mode register and PIO Direction register are configured as PIO modes, the 32 MUX definition pins can be used as PIO pins. For example, the DEN_n/PIO5 (Pin 154) can be used as a PIO5.
2. The PIO status during Power-On reset:

   (1) PIO1, PIO6 and PIO10 are inputs with pull-down.

   (2) PIO4, PIO5, PIO7, PIO8, PIO9, PIO21 and PIO22 are normal operations.

   (3) Other PIOs are inputs with pull-up.
3. In Slow Bus Mode (Bus Mode 0):

   I/O bus is mapped to SAD [15:0] or SAD [7:0]. It depends on the hardware setting of DTR1_n/SBWSEL Pin (Pin 29) during power-on reset to select 16-bit mode or 8-bit mode.

   Memory bus is mapped to A [10:0]/D [15:0].
4. In Normal Bus Mode (Bus Mode 1):

   I/O bus and Memory bus are all mapped to A [19:0] and D [15:0]. The SAD [15:0] bus is inactive in this mode.
5. Change Bus Mode 0 and Bus Mode 1 by means of setting the internal Bus Control Register. This action must be initialized by software.

6. As all/partial Slow Bus Address, SA[18:0], on multiplexed pins are required, Bus Control Register should be enabled, then the default settings are disabled.

3.3 PIN Capacitance Description

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance		2.8		pF
C_{OUT}	3.3V Output Capacitance	2.7		4.9	pF
C_{BID}	3.3V Bi-directional Capacitance	2.7		4.9	pF

3.4 PIN Pull-up/Pull-down Description

PIN Name	Pin No.	Pull-up	Pull-down	Schmitt Trigger	5V I/O Tolerant	Description
RST_n ARDY	147 149	1	0	1	1	
HOLD/SA12 NMI INT0/SA11 INT1	152 4 9 7	0	1	0	1	
WR_n/BWSEL WLB_n/SA0	42 40	1	0	0	1	
TMROUT0/SA7 TMROUT1/SA8 /PIO	13 12	0	PIO10 PIO1	0	1	When set in normal operation, these two pins are with neither pull-up nor pull-down resistors. However, when set in PIO, they are input with pull-down resistors.
INT3	5	0	1	0	1	
UCS_n MCS_n	106 105	1	0	1	0	
PIO27 PIO28	43 45	PIO27 PIO28	0	0	1	
PIO29/UARTX0 PIO30/UARTX1	46 47	0	PIO29 PIO30	0	1	
INT2 DEN_n DT/R_n PCS0_n PCS1_n PCS2_n/IOR_n PCS3_n/IOW_n PCS5_n	6 154 153 158 157 36 37 155	PIO31 PIO5 PIO4 PIO14 PIO15 PIO25 PIO26 PIO3	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1	When set in normal operation, these pins are with neither pull-up nor pull-down resistors. However, when set in PIO, they are input with pull-up, pull-down, or schimitt trigger as listed in the left table.

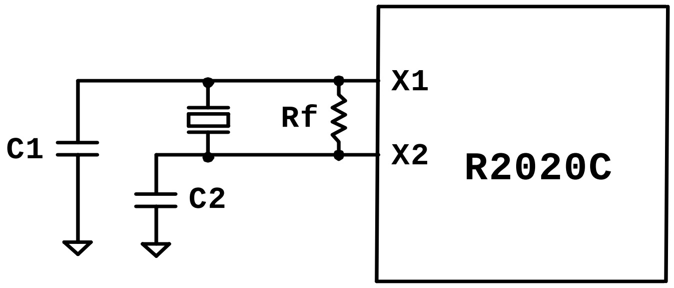
PCS6_n	156	PIO2	0	0		
TMRIN0/SA9	11	PIO11	0	0		
TMRIN1/SA10	10	PIO0	0	0		
DRQ0/INT5/SA5	15	PIO12	0	0		
DRQ1/INT6/SA6	14	PIO13	0	0		
TXD0_3	122	PIO16	0	0		
TXD0_2	121	PIO17	0	0		
TXD0_1	120	PIO18	0	0		
TXD0_0	119	PIO19	0	0		
TXC0	118	0	0	PIO21		
RXC0	117	PIO22	0	0		
RXD0_3	116	PIO23	0	0		
RXD0_2	115	PIO24	0	0		
RXD0_1	113	PIO6	0	0		
TXEN0	123	0	PIO20	0		
/PIO						
DCD0_n SIN0 SOUT0 DTR0_n DSR0_n RI0_n RTS0_n CTS0_n /SAD15-8	23 16 17 20 22 25 18 21	1	0	0	1	
SOUT1 DSR1_n/TCK DCD1_n/TDI CTS1_n/TMS RI1_n/SA4	27 31 32 30 33	1	0	0	1	
DTR1_n/SBWSEL	29	1	0	0	1	
RXD0_0 RXDV0 COL0	112 111 124	0	1	0	1	
TXC1 RXC1	138 137	0	1	1	1	
RXD1_3 RXD1_2 RXD1_1 RXD1_0 RXDV1 RXER1 COL1 RXER0/SA17	136 135 134 133 132 131 145 110	0	1	0	1	
TXD1_3/PDIVID0 TXD1_0/PFREQ0	143 139	1	0	0	1	
TXD1_2/PDIVID1 TXD1_1/PDIVID2 TXEN1/CLKJMP	142 141 144	0	1	0	1	
MDIO0 MDIO1	108 129	0	1	0	1	
JTAGEN/SA3	34	0	1	1	1	

SA2	35				0	
PHY_CHG0/SA16 PHY_CHG1/SA14	126 146	0	1	0	1	
CLKOUTA	127	0	0	0	0	
WHB_n/SA1	39	0	0	0	0	
RD_n	41	0	0	0	1	
A[17:19]/PIO	51,49,48	0	0	0	0	
A[0:10]	73~78 82~86	0	0	0	0	
A[11:16]	52~56 72	0	0	0	0	
D[0:15]	57~59 61~63 65~66 96~99 101~104	0	0	0	0	
HLDA/SA13	150	0	0	0	0	
SIN1	26	0	0	0	1	
RTS1_n/TDO /DUGSEL	28	0	0	0	1	
MDC0 MDC1	109 130	0	0	0	0	
SD_CLK	80	0	0	0	0	
WE_n CAS_n RAS_N BA[0:1] DQML DQMH	94 93 91 87~88 95 69	0	0	0	0	
A20/MA11 A21/SA18	70 90	0	0	0	0	

Note: The pins never in the pull-up, pull-down, schimitt trigger, and I/O pad status are not shown in the above table.

4. Oscillator Characteristics

4.1 Fundamental Mode



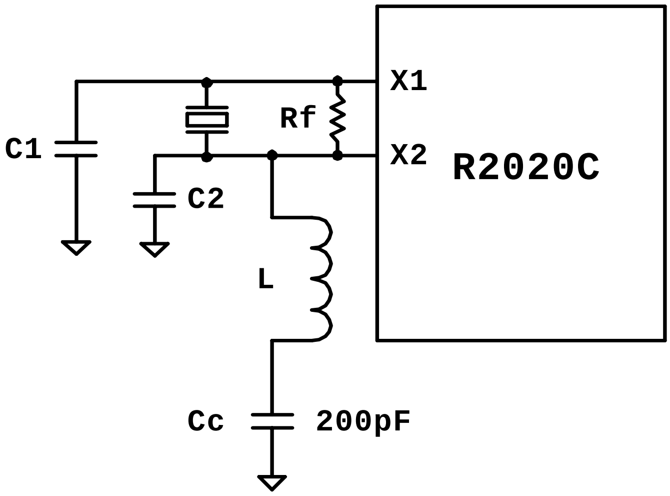
C1 -------------- 20pF ± 20%

C2 -------------- 20pF ± 20%

Rf -------------- 1 mega-ohm

4.2 Third-Overtone Mode

Normally, high frequency use for third overtone mode can get price advantage, but additional L and Cc are needed.



Typical value suggestions are as follows:

C1 -------------- 20pF ± 20%

C2 -------------- 20pF ± 20%

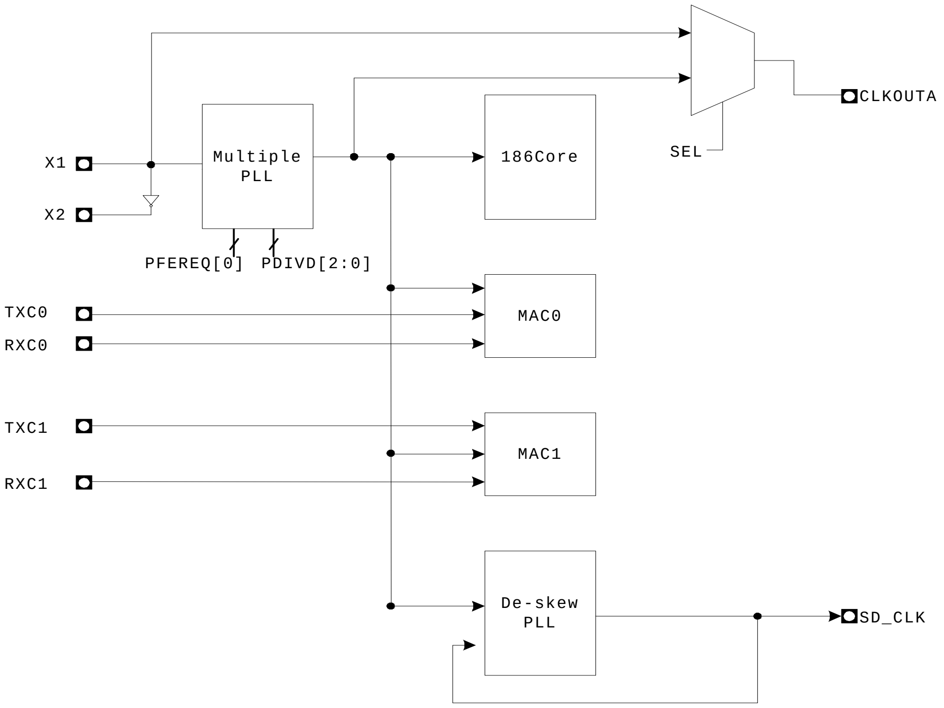
Cc -------------- 200pF± 20%

Rf --------------- 1 Mega-Ohm

L ---------------- 4.7uH, 6.8uH, 8.2uH, 10uH (25MHz)

Note: X1 input clock must be within + - 100ppm tolerance.

5. Clock Unit



PLL Configuration Table:

Input Clock Range (Mhz)	PFEREQ[0]	PDIVD[2:0]			Multiple	Output Clock (Mhz)
25	1	0	0	0	1	Reserved
		0	0	1	2	50
		0	1	0	3	75
		0	1	1	4	100
		1	0	0		Reserved
		1	0	1		Reserved
		1	1	0		Reserved
		1	1	1		Reserved
40	0	0	0	0	1	40
		0	0	1	2	80
		0	1	0		Reserved
		0	1	1		Reserved
		1	0	0		Reserved
		1	0	1		Reserved
		1	1	0		Reserved
		1	1	1		Reserved

For example: If input clock =25 Mhz, then set PFEREQ=1b.

If PDIVD[2:0]=000b, then PLL output clock =25 Mhz

If PDIVD[2:0]=011b, then PLL output clock =100 Mhz

6. Execution UNIT

6.1 General Registers

The R2020C has eight 16-bit general registers. And the AX, BX, CX, and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows:

AX: Word Divide, Word Multiply, Word I/O operation.

AH: Byte Divide, Byte Multiply, Byte I/O, Decimal Arithmetic, Translate operation.

AL: Byte Divide, Byte Multiply operation.

BX: Translate operation.

CX: Loops, String operation

CL: Variable Shift and Rotate operation.

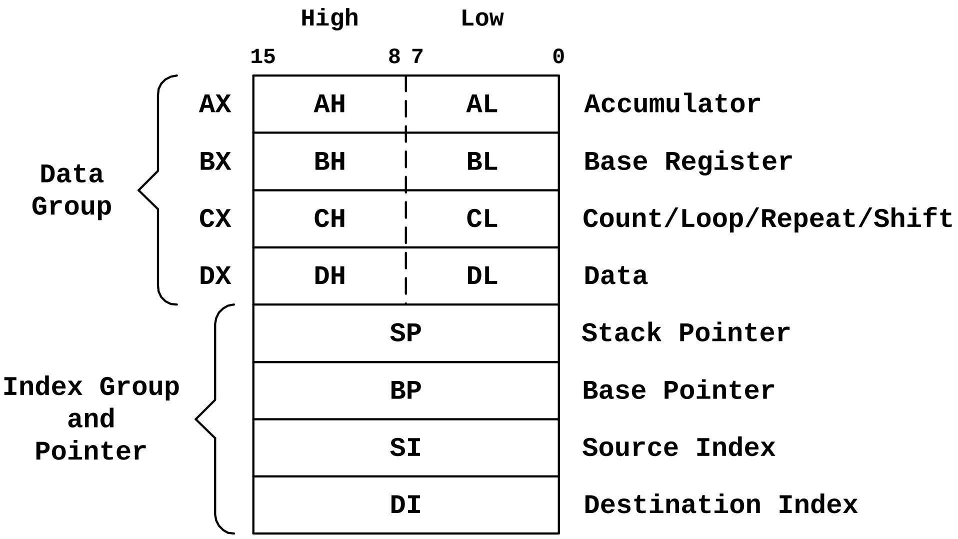
DX: Word Divide, Word Multiply, Indirect I/O operation

SP: Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

BP: General-purpose registers which can be used to determine offset address of operands in Memory.

SI: String operations

DI: String operations



GENERAL REGISTERS

6.2 Segment Registers

R2020C has four 16-bit segment registers: CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

CS (Code Segment): The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instructions is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000H.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000H.

ES (Extra Segment): The ES register points to the current extra segment, which is typically for data storage, such as large string operations and large data structures. The ES register is initialized to 0000H.

15 8 7 0	
CS	Code Segment
DS	Data Segment
SS	Stack Segment
ES	Extra Segment

SEGMENT REGISTERS

6.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register and it contains the offset of the next instruction to be fetched. The IP register cannot be directly accessed by software. This register is update by the bus interface unit. It can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000H and the starting execution address for CS:IP is at 0FFFF00H.

Register Name: Processor Status Flags Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Rsvd	AF	Rsvd	PF	Rsvd	CF

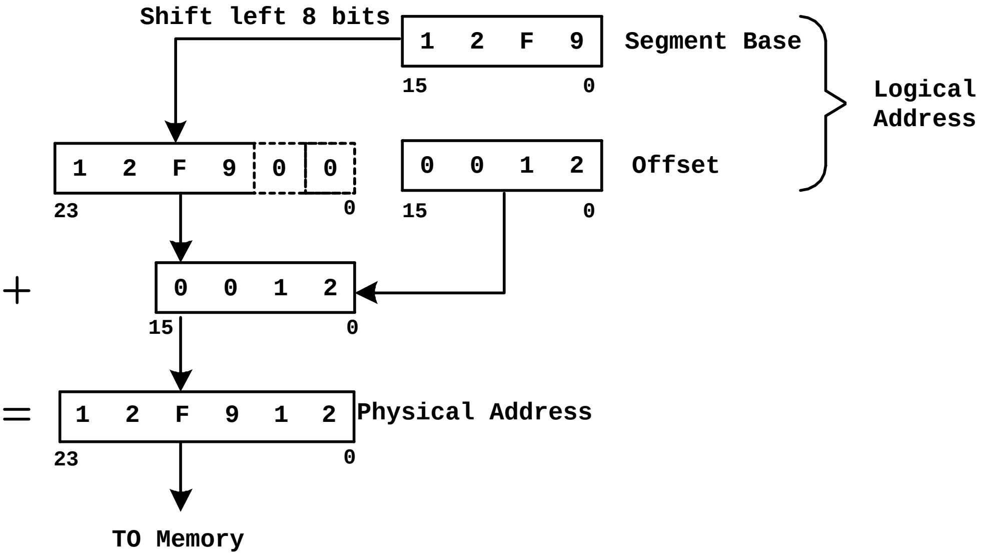
These flags reflect the status after the Execution Unit is executed.

Bit	Name	Description
15-12	Rsvd	Reserved.
11	OF	Overflow Flag. If an arithmetic overflow occurs, this flag will be set.
10	DF	Direction Flag. If this flag is set, the string instructions are in the process of incrementing address. If DF is cleared, the string instructions are in the process of decrementing address. Refer to the STD and CLD instructions for how to set and clear the DF flag.
9	IF	Interrupt-Enable Flag. Refer to the STI and CLI instructions for how to set and clear the IF flag. Set to 1: The CPU enables the mask able interrupt request. Set to 0: The CPU disables the mask able interrupt request.
8	TF	Trace Flag. Set to enable single-step mode for debugging; Clear to disable the single-step mode. If an application program sets the TF flag with POPF or IRET instruction, a debug exception is

		generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.
7	SF	Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1, indicating the state of being negative.
6	ZF	Zero Flag. If this flag is set, the result of operation will be zero.
5	Rsvd	Reserved
4	AF	Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low nibble of the AL general-purpose register. It is used in BCD operation.
3	Rsvd	Reserved
2	PF	This flag will be set if the result of the low-order 8 bits operation has even parity.
1	Rsvd	Reserved
0	CF	Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

6.4 Address Generation

The Execution Unit generates a 24-bit physical address to Bus Interface Unit by the Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



Physical Address Generation

7. Peripheral Register List

The Peripheral Control Block can be mapped into either Memory or I/O space by programming the Peripheral Control Block Relocation Register (FEh). After reset, the default Legacy Peripheral Control Block offset is located at FF00h in I/O space, the SDRAM Control Register, EDO, Cache and Low speed clock is located at FE00h in I/O space, and Ethernet Control Register is located at FD00h and FE00h in I/O space.

The following table lists are all the definitions of the Peripheral Control Block Registers, and the detailed descriptions will be arranged on the related Block Unit.

7.1 Legacy Peripheral Registers (Base Address FF00h)

Offset (HEX)	**Register Name**	**Page**	Offset (HEX)	**Register Name**	**Page**
FE	Peripheral Control Block Relocation Register	30	72	PIO Direction 0 Register	94
F8	Processor Extended ID Register	31	70	PIO Mode 0 Register	95
F6	Reset Configuration Register	33	66	Timer 2 Mode / Control Register	74
F4	Processor Release Level Register	30	62	Timer 2 Maxcount Compare A Register	75
F2	Auxiliary configuration Register	39	60	Timer 2 Count Register	75
EA	Bus Control Register	34	5E	Timer 1 Mode / Control Register	72
E6	Watchdog Timer Control Register	76	5C	Timer 1 Maxcount Compare B Register	74
E4	Enable RCU Register	47	5A	Timer 1 Maxcount Compare A Register	73
E2	Clock Prescalar Register	47	58	Timer 1 Count Register	73
DA	DMA1 Control Register	64	56	Timer 0 Mode/Control Register	70
D8	DMA1 Transfer Count Register	66	54	Timer 0 Maxcount Compare B Register	71
D6	DMA1 Destination Address High Register	66	52	Timer 0 Maxcount Compare A Register	71
D4	DMA1 Destination Address Low Register	66	50	Timer 0 Count Register	71
D2	DMA1 Source Address High Register	67	44	Serial Port 0 interrupt control register	50
D0	DMA1 Source Address Low Register	67	42	Serial port 1 interrupt control register	50
CA	DMA0 Control Register	62	40	MAC Interrupt Control Register	51
C8	DMA0 Transfer Count Register	62	3E	INT3 Control Register	52
C6	DMA0 Destination Address High Register	63	3C	INT2 Control Register	52
C4	DMA0 Destination Address Low Register	63	3A	INT1 Control Register	53
C2	DMA0 Source Address High Register	63	38	INT0 Control Register	53
C0	DMA0 Source Address Low Register	64	36	DMA1/INT6 Interrupt Control Register	54
AC	MCS_n Extended Register	45	34	DMA0/INT5 Interrupt Control Register	55
AA	Chip Size Multiplier Register	46	32	Timer Interrupt Control Register	55
A8	PCS_n and MCS_n Auxiliary Register	44	30	Interrupt Status Register	56
A6	Midrange Chip Select Register	43	2E	Interrupt Request Register	56
A4	Peripheral Chip Select Register 0	42	2C	Interrupt In-service Register	57
A2	Low Memory Chip Select Register	41	2A	Interrupt Priority Mask Register	58
A0	Upper Memory Chip Select Register	40	28	Interrupt Mask Register	58
88	(See 7.2)	27	26	Interrupt Poll Status Register	59
86	(See 7.2)	27	24	Interrupt Poll Register	59
84	(See 7.2)	27	22	Interrupt End-of-Interrupt	60

82	(See 7.2)	27	18	(See 7.2)	27
80	(See 7.2)	27	16	(See 7.2)	27
7A	PIO Data 1 Register	93	14	(See 7.2)	27
78	PIO Direction 1 Register	93	12	(See 7.2)	27
76	PIO Mode 1 Register	94	10	(See 7.2)	27
74	PIO Data 0 Register	94			

7.2 16550 UART Register Definitions (Base Address FF00h)

Offset (HEX)	**Register Name**	**Mnemonic**	**Page**
80h	A Receiver Buffer Register (when DLAB=0 & Read)	**RBR0**	79
	UART0 Transmitter Holding Register (when DLAB=0 & Write)	**THR0**	80
	UART0 Divisor Latch [Low Byte] (when DLAB=1)	**DLL0**	80
82h	UART0 Interrupt Enable Register (when DLAB=0)	**IER0**	81
	UART0 Divisor Latch [High Byte] (when DLAB=1)	**DLH0**	80
84h	UART0 Interrupt Identification Register (when Read)	**IIR0**	82
	UART0 FIFO Control Register (when Write)	**FCR0**	83
86h	UART0 Line Control Register	**LCR0**	84
88h	UART0 MODEM Control Register	**MCR0**	85
8Ah	UART0 Line Status Register	**LSR0**	86
8Ch	UART0 MODEM Status Register	**MSR0**	88
8Eh	UART0 Scratch Register	**SCR0**	89
10h	UART1 Receiver Buffer Register (when DLAB=0 & Read)	**RBR1**	79
	UART1 Transmitter Holding Register (when DLAB=0 & Write)	**THR1**	80
	UART1 Divisor Latch [Low Byte] (when DLAB=1)	**DLL1**	80
12h	UART1 Interrupt Enable Register (when DLAB=0)	**IER1**	81
	UART1 Divisor Latch [High Byte] (when DLAB=1)	**DLH1**	80
14h	UART1 Interrupt Identification Register (when Read)	**IIR1**	82
	UART1 FIFO Control Register (when Write)	**FCR1**	83
16h	UART1 Line Control Register	**LCR1**	84
18h	UART1 MODEM Control Register	**MCR1**	85
1Ah	UART1 Line Status Register	**LSR1**	86
1Ch	UART1 MODEM Status Register	**MSR1**	88
1Eh	UART1 Scratch Register	**SCR1**	89

7.3 Cache Control Register (Base Address FEC0h)

Offset (HEX)	**Register Name**	**Mnemonic**	**Page**
C0h	Cache control register	**CCR**	96
C4h	Non-Cache region0 Starts Address High	**NCR0SH**	97
C2h	Non-Cache region0 Starts Address Low	**NCR0SL**	96
C8h	Non-Cache region0 End Address High	**NCR0EH**	97
C6h	Non-Cache region0 End Address Low	**NCR0EL**	97
CCh	Non-Cache region1 Starts Address High	**NCR1SH**	98
CAh	Non-Cache region1 Starts Address Low	**NCR1SL**	98
D0h	Non-Cache region1 End Address High	**NCR1EH**	99
CEh	Non-Cache region1 End Address Low	**NCR1EL**	98
D4h	Non-Cache region2 Starts Address High	**NCR2SH**	99

D2h	Non-Cache region2 Starts Address Low	**NCR2SL**	99
D8h	Non-Cache region2 End Address High	**NCR2EH**	100
D6h	Non-Cache region2 End Address Low	**NCR2EL**	100
DCh	Non-Cache region3 Starts Address High	**NCR3SH**	101
DAh	Non-Cache region3 Starts Address Low	**NCR3SL**	100
E0h	Non-Cache region3 End Address High	**NCR3EH**	101
DEh	Non-Cache region3 End Address Low	**NCR3EL**	101
E4h	Write-Invalidate region Starts Address High	**WIRSH**	102
E2h	Write-Invalidate region Starts Address Low	**WIRSL**	102
E8h	Write-Invalidate region End Address High	**WIREH**	103
E6h	Write-Invalidate region End Address Low	**WIREL**	102

7.4 SDRAM Control Registers (Base Address FE00h)

Offset (HEX)	**Register Name**	**Mnemonic**	**Page**
F2h	SDRAM Mode Set Register	**SDRAMMSR**	104
F4h	SDRAM Control Register	**SDRAMCR**	104
F6h	SDRAM Timing Parameter Register	**SDRAMTPR**	105

7.5 Fast Ethernet MAC Control Registers (Base Address: MAC0 / FD00h & MAC1 / FE00h)

Offset (HEX)	**Register Name**	**Mnemonic**	**Page**
00h	MAC Control Register 0	**MCR0**	111
04h	MAC Control Register 1	**MCR1**	112
08h	MAC Bus Control Register	**MBCR**	113
0Ch	TX Interrupt Control Register	**MTICR**	114
10h	RX Interrupt Control Register	**MRICR**	114
14h	TX Poll Command Register	**MTPR**	115
18h	RX Buffer Size Register	**MRBSR**	115
1Ah	RX Descriptor Control Register	**MRDCR**	116
1Ch	MAC Last Status Register	**MLSR**	116
20h	MAC MDIO Control Register	**MMDIO**	117
24h	MAC MII Read Data Register	**MMRD**	118
28h	MAC MII Write Data Register	**MMWD**	118
2Ch	MAC TX Descriptor Start Address Register	**MTDSA0**	119
30h	MAC TX Descriptor Start Address Register	**MTDSA1**	119
34h	MAC RX Descriptor Start Address Register	**MRDSA0**	120
38h	MAC RX Descriptor Start Address Register	**MRDSA1**	120
3Ch	MAC INT Status Register	**MISR**	121
40h	MAC INT Enable Register	**MIER**	121
44h	MAC Event Counter INT Status Register	**MECISR**	122
48h	MAC Event Counter INT Mask Register	**MECIER**	123
50h	MAC Successfully Received Packet Counter	**MRCNT**	123
52h	MAC Event Counter 0 Register	**MECNT0**	124
54h	MAC Event Counter 1 Register	**MECNT1**	124
56h	MAC Event Counter 2 Register	**MECNT2**	124
58h	MAC Event Counter 3 Register	**MECNT3**	125
5Ah	MAC Successfully Transmit Packet Counter Register	**MTCNT**	125

5Ch	MAC Event Counter 4 Register	**MECNT4**	126
5Eh	MAC Pause Frame Counter Register	**MPCNT**	126
60h	MAC Hash Table Word 0	**MAR0**	126
62h	MAC Hash Table Word 1	**MAR1**	127
64h	MAC Hash Table Word 2	**MAR2**	127
66h	MAC Hash Table Word 3	**MAR3**	127
68h	MAC Multicast Address first two bytes Register	**MID0L**	128
6Ah	MAC Multicast Address second two bytes Register	**MID0M**	128
6Ch	MAC Multicast Address last two bytes Register	**MID0H**	128
70h	MAC Multicast Address first two bytes Register	**MID1L**	129
72h	MAC Multicast Address second two bytes Register	**MID1M**	129
74h	MAC Multicast Address last two bytes Register	**MID1H**	129
78h	MAC Multicast Address first two bytes Register	**MID2L**	130
7Ah	MAC Multicast Address second two bytes Register	**MID2M**	130
7Ch	MAC Multicast Address last two bytes Register	**MID2H**	130
80h	MAC Multicast Address first two bytes Register	**MID3L**	131
82h	MAC Multicast Address second two bytes Register	**MID3M**	131
84h	MAC Multicast Address last two bytes Register	**MID3H**	131

8. Peripheral Control Block Registers

The peripheral control block can be mapped into either memory or I/O space by programming the Peripheral Control Block Registers (FEh Registers). It starts at FF00h in I/O space after reset.

Register Offset: FEh
Register Name: Peripheral Control Block Relocation Register
Reset Value : 20FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M/IO_n	R[23:12] or R[19:8]											

The Peripheral Control Block (PCB) is mapped into either memory or I/O space by programming this register. When the other chip selects (PCSx_n) are programmed to zero wait state and the external ready is ignored, PCSx_n can overlap the control block.

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved.
12	M/IO_n	R/W	Memory/IO space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space. Set 1: The PCB is located in memory space. Set 0: The PCB is located in I/O space (Default).
11-0	R[23:12] or R[19:8]	R/W	Relocation Address Bits. The upper address bits of the PCB base address. In IO space, the lower eight bits are defaulted to 00h. When the PCB is mapped into I/O space, the R[19:16] must be programmed to 0000b. In memory space, R[19:8] are mapped into A[23:12] and the lower twelve bits are defaulted to 000h.

Register Offset: F4h
Register Name: Processor Release Level Register
Reset Value : 1AD9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0	1	1	0	1	1	0	0	1

The read only registers specify the processor release version and RDC identification number.

Bit	Name	Attribute	Description
15-12	PRL	RO	4’b0001
11-8	PV	RO	Processor version.
7-0	ID	RO	RDC identification number 8’hD9.

Register Offset: F8h

Register Name: Processor Extended ID Register

Reset Value : 1602h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEID															

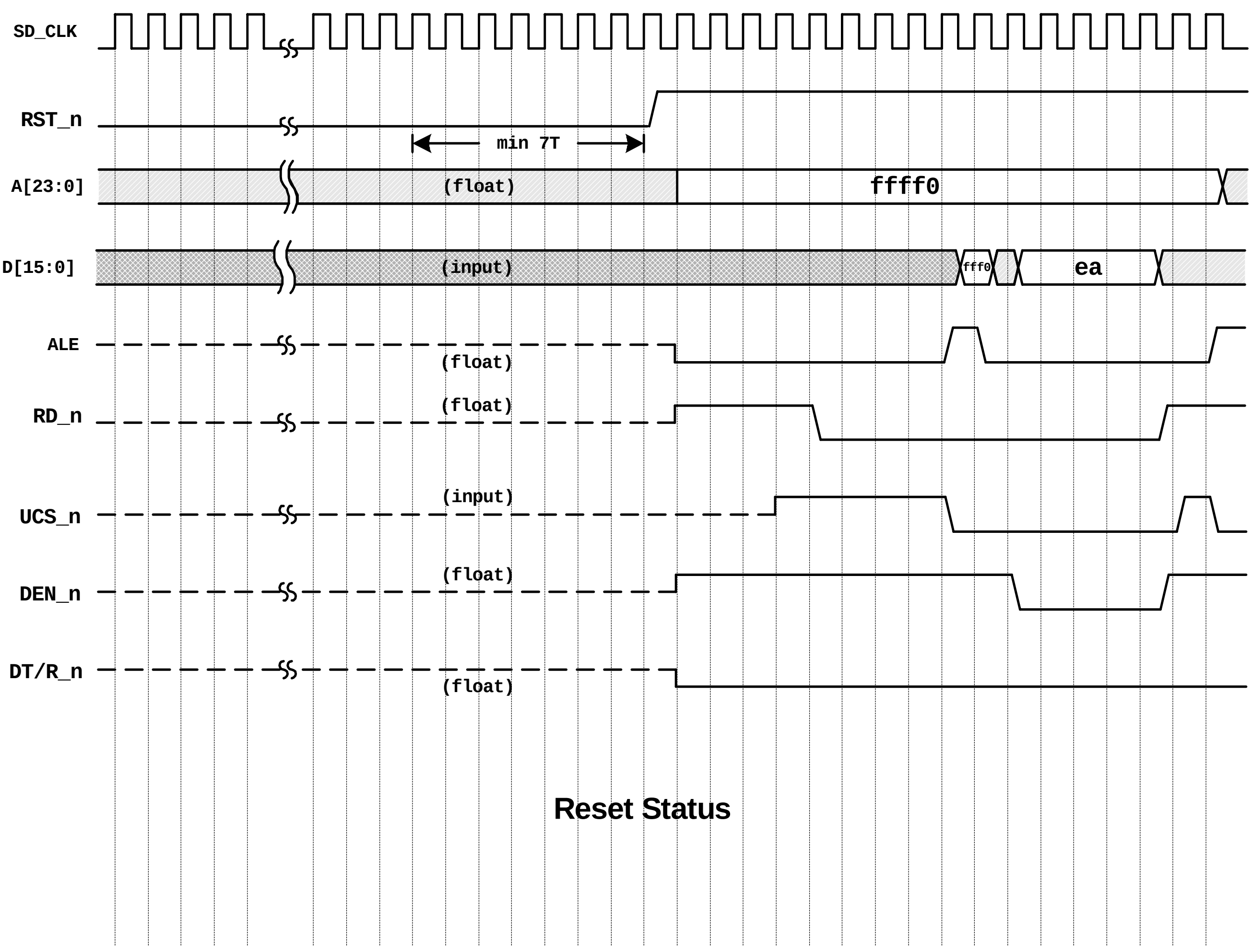
Bit	Name	Attribute	Description
15-0	PEID	RO	This read only register specifies the RDC identification extended number.

9. Reset

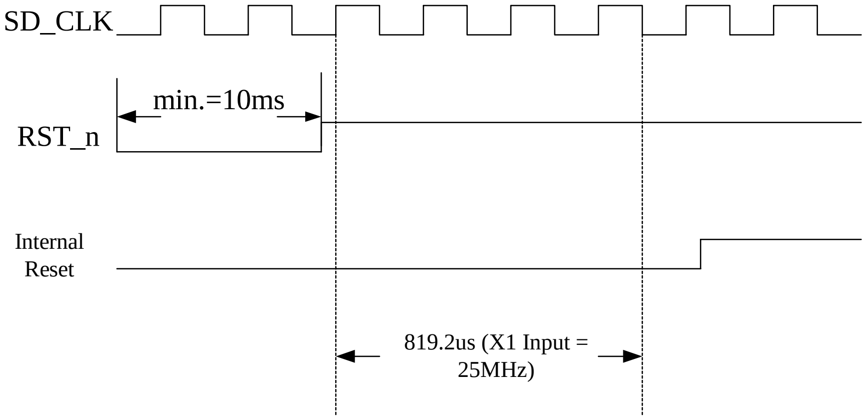
Processor initialization is accomplished with activation of the RST_n pin. To reset the processor, this pin should be held how for at least seven oscillator periods. The Reset Status Figure shows the status of the RST_n pin and the other related pins.

When RST_n goes from low to high, the state of input pins (with weak pull-up or pull-down resistors) will be latched, and each pin will perform the individual function. The D[15:0] will be latched into the register F6h. The D[15:0] bus will not drive the address phase but the data phase during UCS_n and LCS_n cycles if WLB_n is with a pull-high resistor.

9.1 Power-up Reset



Reset Status



Power-up Reset Timing

Register Offset: F6h

Register Name: Reset Configuration Register

Reset Value : D[15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC															

Bit	Name	Attribute	Description
15-0	RC	RO	Reset Configuration D[15:0]. The D[15:0] must be with weak pull-up or pull-down resistors to correspond the contents when they are latched into this register as the RST_n signal goes from low to high. The value of the reset configuration register provides the system information when the software reads this register. This register is read only and the contents remain valid until next processor reset.

10. Bus Interface UNIT

10.1 Slow Bus

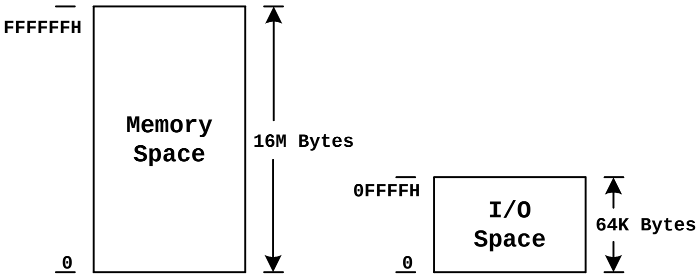
Register Offset: EAh
Register Name: Bus Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMOD	Reserved								PCSE	SLAS			Reserved		

Bit	Name	Attribute	Description
15	BMOD	R/W	Bus Mode Select bit. Set 0: Slow bus mode. When the PCS/MCS regions are accessed, the bus cycle is mapped to SAD [15:0] or SAD [7:0]. Set 1: Normal bus mode. When the PCS/MCS regions are accessed, the bus cycle is mapped to A [23:0] and D [15:0]. The SAD bus is inactive in this mode.
14-7	Rsvd	R	Reserved
6	PCSE	R/W	IOR_n, IOW_n control signal enable When this bit is set. PIN36 is IOR_n and PIN37 is IOW_n. When this bit is clear. PIN36 is PCS2/PIO25 and PIN37 is PCS3/PIO26.
5-3	SLAS	R/W	SLA bus address selection bits 000: No slow bus address. 001: SLA5..0 010: SLA7..0 011: SLA11..0 100: SLA18..0
2-0	Rsvd	R	Reserved

10.2 Memory and I/O Interface

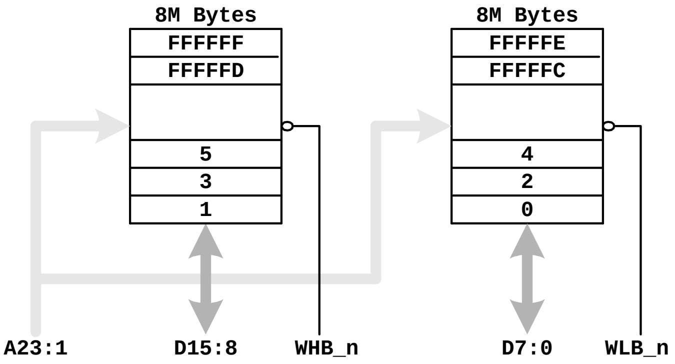
The memory space consists of 16M bytes (8M 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A[23:16] to low level.



Memory and I/O Space

10.3 Data Bus

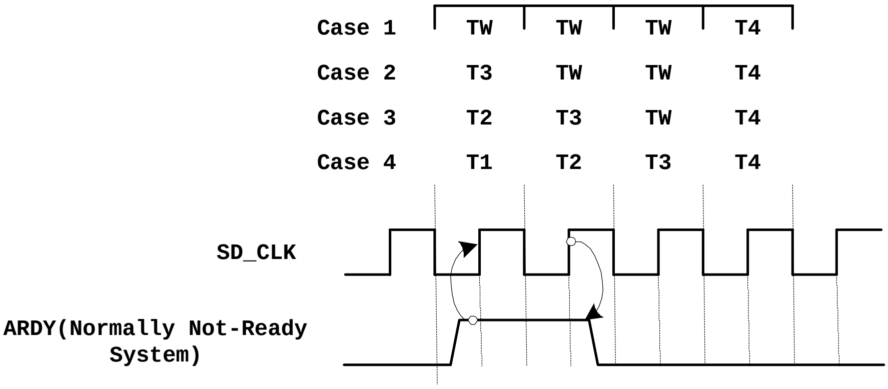
The memory address space data bus is physically implemented by dividing the address space into two banks of up to 8M bytes. Each bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0). The other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). WHB_n and WLB_n determine whether one bank or both banks participate in the data transfer.



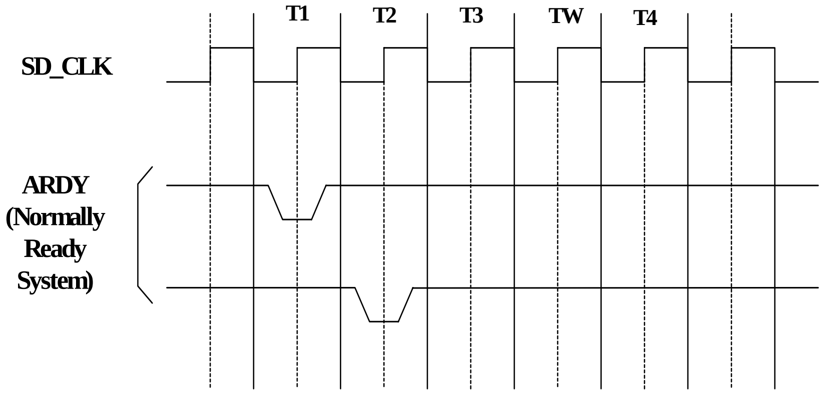
Physical Data Bus Models

10.4 Wait States

Wait states extend the data phase of the bus cycle. The ARDY input with low level will insert wait states. To avoid wait states, ARDY must be high within a specified setup time prior to phase 2 of T1 and keep to phase 2 of T2. To insert wait states, ARDY must be driven low within a specified setup time prior to phase 2 of T1 or phase 2 of T2. When the SDRAMEN bit in the SDRAM Control Register (FEF4h) is set to 1, the external ready ARDY and internal wait states are ignored while accessing the SDRAMs.



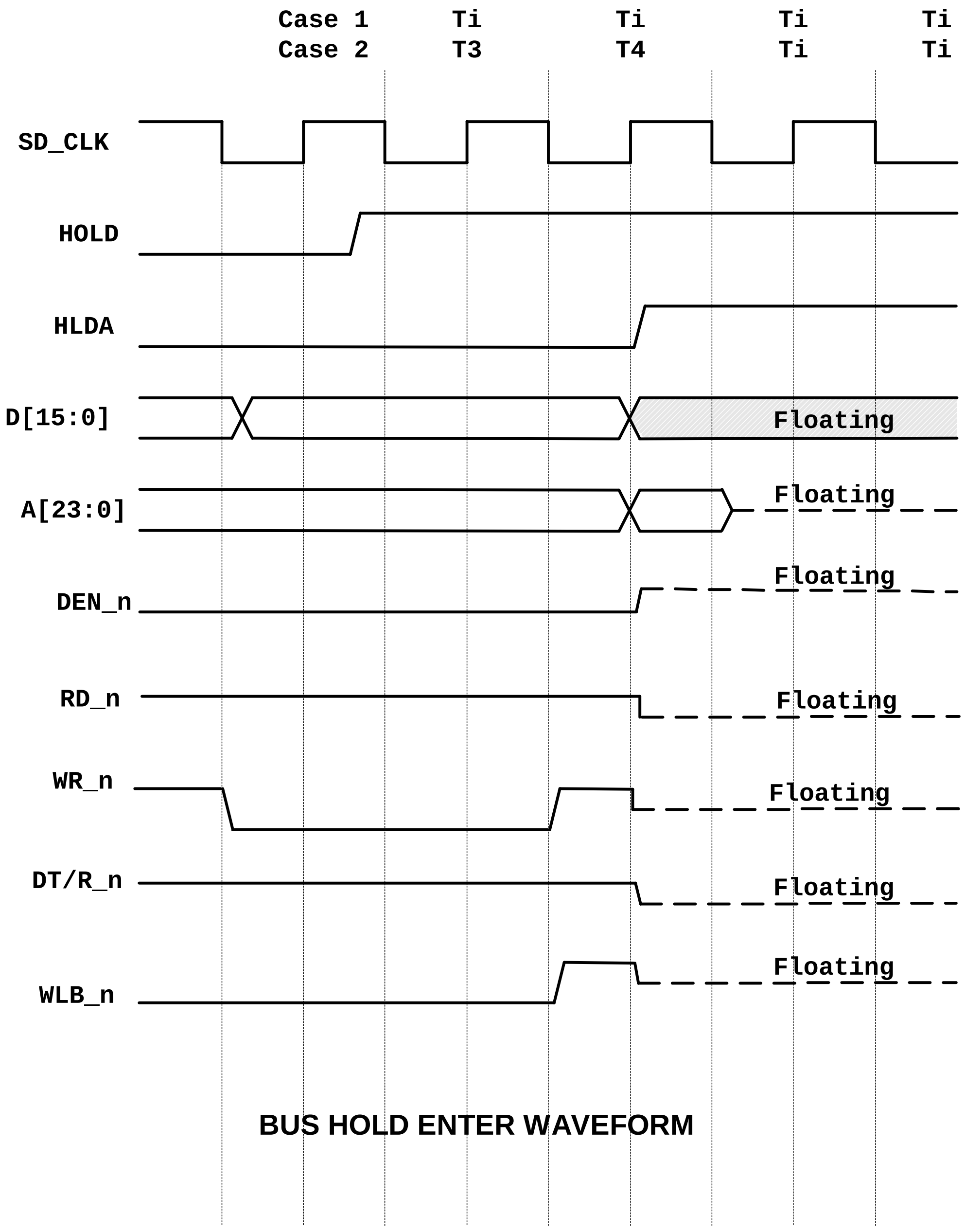
Asynchronous Ready Waveforms



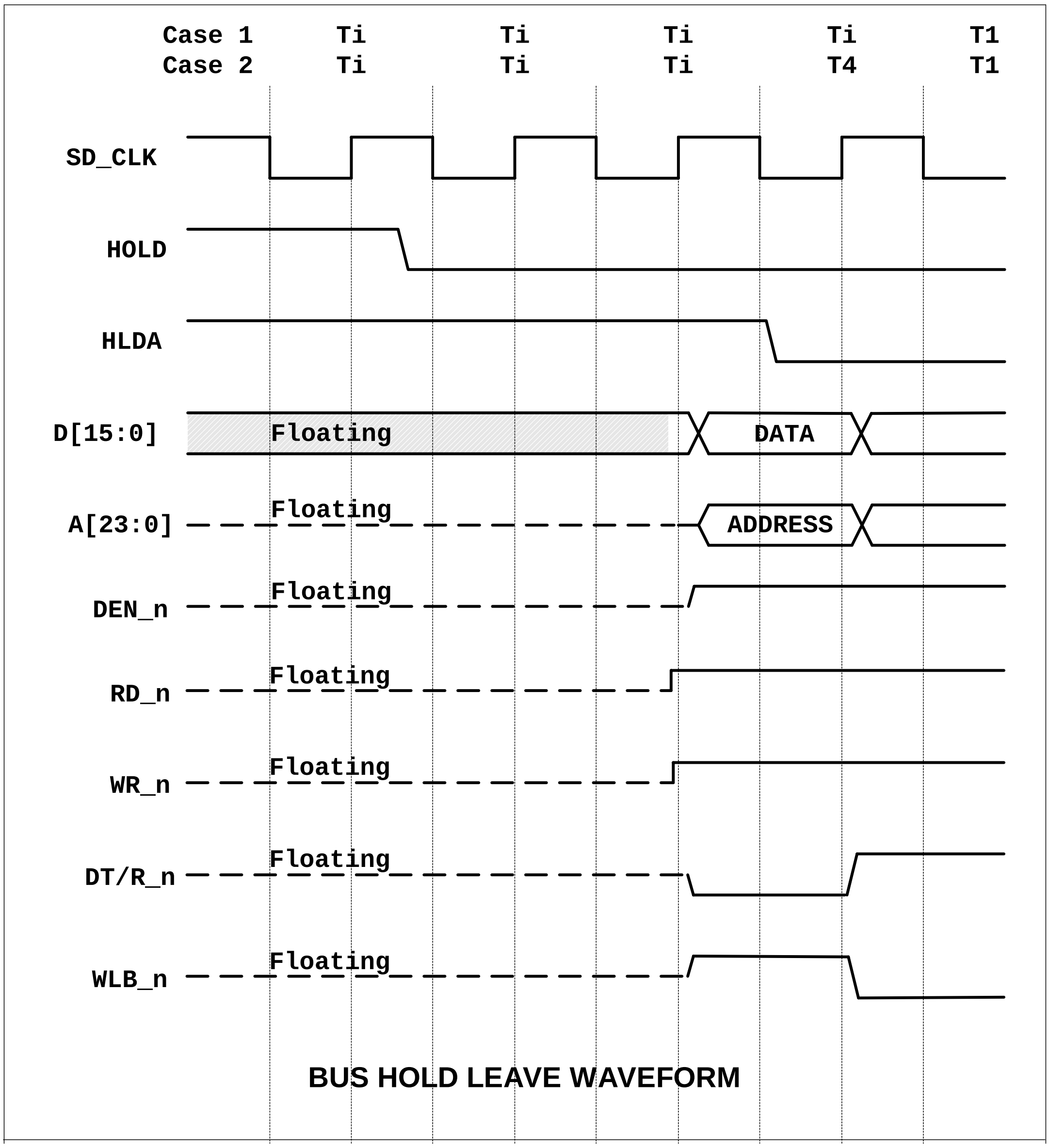
Asynchronous Ready Waveforms

10.5 Bus Hold

When the bus hold is requested (as HOLD pin and being active high) by another bus master, the microprocessor will issue a HLDA in response to a HOLD request at the end of T4 or Ti. When the microprocessor is in hold status (HLDA is high), the D[15:0], A[23:0], WR_n, RD_n, DEN_n, S1_n – S0_n, S6_n, DT/R_n, WHB_n, and WLB_n will be floating, and the UCS_n, PCS6_n – PCS5_n, and PCS3_n – PCS0_n will be driven high. After HOLD is detected as being low, the microprocessor will lower the HLDA.



BUS HOLD ENTER WAVEFORM



BUS HOLD LEAVE WAVEFORM

10.6 Bus Width

The R2020C default is 16-bit bus access and the bus can be programmed as 8-bit or 16-bit access during memory or I/O access is located in the LCS_n or PCSx_n address space. The UCS_n code- fetched selection can be 8-bit or 16-bit bus width, which is decided by the BWSEL pin (pin42) input status when the RST_n pin goes from low to high. When the BWSEL pin is with a pull-low resistor, the bus width for the code-fetched selection is 8 bits. The SDRAM bus width is unchangeable 16 bits. If the R2020C has been set as 16-bit mode, it cannot be changed to 8-bit mode.

Register Offset: F2h
Register Name: Auxiliary Configuration Register
Reset Value : 0080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCS6	PCS5	PCS3	PCS2	PCS1	Reserved			USIZ	0	0	0	0	0	MSIZ	PCS0

Bit	Name	Attribute	Description
15	PCS6	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
14	PCS5	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
13	PCS3	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
12	PCS2	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
11	PCS1	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
10-8	Rsvd	RO	Reserved
7	USIZ	RO	Boot code bus width. This bit reflects the BWSEL pin input status when the RST_n pin goes from low to high. Set 0: 16-bit bus width booting when the BWSEL pin is **without a pull-low** resistor. (Default: It is an internal pull-high resistor.) Set 1: 8-bit bus width booting when the BWSEL pin is with a 4.7k ohm external pull-low resistor.
6-2	Rsvd	RO	Reserved
1	MSIZ	R/W	Midrange Data Bus Size selection. This bit determines the width of the data bus for all MCS and PCS space accesses (if mapped to memory space). 1: 8-bit data bus access. 0: 16-bit data bus access.
0	PCS0	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.

11. Chip Select UNIT

The Chip Select Unit provides 9 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through four peripheral control registers (A0h, A2h, A4h and A8h) and all the chip selects can insert wait states by programming the peripheral control registers.

11.1 UCS_n

The UCS_n default is active on reset for Code access. The active memory range is upper 8M (800000h – FFFFFFh), which is programmable. And the default memory active range of UCS_n is 64k (FF0000h – FFFFFFh). UCS_n will drive low within four SD_CLK cycles when active if no wait state is inserted. There are fifteen wait states inserted to UCS_n active cycle on reset.

Register Offset: A0h
Register Name: Upper Memory Chip Select Register
Reset Value : F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB[2:0]			0	0	0	0	0	0	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	LB[2:0]	R/W	**LB[2:0]**, Memory block size selection for UCS_n chip select pin. The active region of the UCS_n chip select pin can be configured by LB[2:0]. The default memory block size is from 800000h to FFFFFFh. Please refer to the following **Upper Memory Block Size** table for register FFAAh bit 5-3.
11-4	Rsvd	RO	Reserved
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the UCS# chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit3, Bit 1-0: R3, R1-R0**, Wait-State value. R2020C can insert wait states for an access to the UCS_n memory cycle. The reset value for (R3, R1, R0) is (1, 1, 1). **R3, R1, R0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5 1, 0, 1 -- 7

			1, 1, 0 -- 9 1, 1, 1 -- 15

Upper Memory Block Size table:

LB[2:0] FFAAh bit 5-3	000	100	110	111
000	512K	256K	128k	64k
001	1M	512K	256K	128k
010	2M	1M	512K	256K
011	4M	2M	1M	512K
100	8M	4M	2M	1M

11.2 LCS_n

LCS_n means the lower memory region chip selects. The active memory range is lower 8M (000000h – 7FFFFFh), which is programmable. It can be expanded to 8M bytes by FFAAh b2:0.

Register Offset:	A2h
Register Name:	Low Memory Chip Select Register
Reset Value :	——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LB[2:0]			0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-12	LB[2:0]	R/W	**LB[2:0]**, Memory block size selection for the LCS_n chip select pin. The active region of the LCS_n chip select pin can be configured by LB[2:0].The LCS_n pin is not active on reset, but any read or write access to the Low Memory Chip Select Register (A2h) activates this pin. Please refer to the following **Low Memory Block Size** table for register FFAAh bit 2-0.
11-0	Rsvd	RO	Reserved

Low Memory Block Size table:

LB[2:0] FFAAh bit2-0	000	001	011	111
000	64K	128K	256K	512K
001	128K	256K	512K	1M
010	256K	512K	1M	2M
011	512K	1M	2M	4M
100	1M	2M	4M	8M

11.3 PCSx_n

In order to define these pins, the peripheral or memory chip selects are programmed through A4h and A8h registers. The base address memory block can be located anywhere within the 1M bytes memory space, exclusive of the areas associated with LCS_n and UCS_n. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS6_n – PCS5_n can be configured from (0 to 31wait states) + (1 to 225 wait states). PCS3_n – PCS0_n can be configured from (1 to 31 wait states) + (1 to 225 wait states). The PCSx_n pins are not active on reset. The PCSx_n pins are activated as chip selects by writing to the peripheral chip select register 0 and 1.

Register Offset: A4h
Register Name: Peripheral Chip Select Register 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:12]								BA23	BA22	BA21	BA20	R3	R2	R1	R0

Bit	Name	Attribute	Description
15-8	BA[19:12]	R/W	Base Address. BA[23:12] corresponds to Bit [23:12] of the 16M-Byte(24-bits) programmable base address of the PCS_n chip select block. When the PCS_n chip selects are mapped to I/O space, BA[23:16] must be written to 0000b because the I/O address bus is only 64K bytes (16-bits) wide. Please refer to the following **Peripheral Chip Size** table for register FFAAh bit 8-6.
7-4	BA[23:20]	R/W	
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the PCS3_n – PCS0_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Values. PR4 (refer to Bit 5 in the A8h register), R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS3_n – PCS0_n access. **PR4, R3, R1, R0 -- Wait States** 0, 0, 0, 0 -- 1 0, 0, 0, 1 -- 3 0, 0, 1, 0 -- 5 0, 0, 1, 1 -- 7 0, 1, 0, 0 -- 9 0, 1, 0, 1 -- 15 0, 1, 1, 0 -- 25 0, 1, 1, 1 -- 40 1, 0, 0, 0 -- 60 1, 0, 0, 1 -- 80 1, 0, 1, 0 -- 100 1, 0, 1, 1 -- 125 1, 1, 0, 0 -- 150 1, 1, 0, 1 -- 180

			1, 1, 1, 0 -- 210 1, 1, 1, 1 -- 255

Peripheral Chip Size table:

FFAAh bit8-6	PCS0	PCS1	PCS2	PCS3	PCS5	PCS6
000	BASE	BASE+256	BASE+512	BASE+768	BASE+1280	BASE+1536
001	BASE	BASE+512	BASE+1024	BASE+1536	BASE+2560	BASE+3072
010	BASE	BASE+1024	BASE+2048	BASE+3072	BASE+5120	BASE+6144
011	BASE	BASE+2048	BASE+4096	BASE+6144	BASE+10240	BASE+12288
100	BASE	BASE+4096	BASE+8192	BASE+12288	BASE+20480	BASE+24576

11.4 MCS_n

Register Offset: A6h
Register Name: Midrange Chip Select Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:12]								BA23	BA22	BA21	BA20	R3	R2	R1	R0

The base address can be set to any integer multiple of the size of the memory block size selected in this Midrange Chip Select Register. For example, if the midrange block is 16Kbytes, the block could be located at 100000h, 104000h, or 108000h, but not at 102000h.

Bit	Name	Attribute	Description
15-4	BA[19:12]	R/W	Base Address. BA[23:12] corresponds to Bit [23:12] of the 16M-Byte (24-bits) programmable base address of the MCS chip select block.
7-4	BA[23:20]	R/W	
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the MCS chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Values. R3, R1, and R0 determine the number of wait states inserted into T3 of the MCS_n access. With regard to the values of R4, please refer to bit 4 in the FFACh register. **R4, R3, R1, R0 -- Wait States** 0, 0, 0, 0 -- 1 0, 0, 0, 1 -- 3 0, 0, 1, 0 -- 5 0, 0, 1, 1 -- 7 0, 1, 0, 0 -- 9 0, 1, 0, 1 -- 15 0, 1, 1, 0 -- 25 0, 1, 1, 1 -- 40

			1, 0, 0, 0 -- 60 1, 0, 0, 1 -- 80 1, 0, 1, 0 -- 100 1, 0, 1, 1 -- 125 1, 1, 0, 0 -- 150 1, 1, 0, 1 -- 180 1, 1, 1, 0 -- 210 1, 1, 1, 1 -- 255

Register Offset: A8h

Register Name: PCS_n and MCS_n Auxiliary Register

Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M[6:0]							Rsvd	MS	PR4	R4	R3	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-8	M[6:0]	R/W	MCS_n Block Size (M[6:0]). Please refer to the following **Midrange Memory Block Size** table for register FFAAh bit 11-9.
7	Rsvd	RO	Reserved
6	MS	R/W	Memory or IO space selector. This bit determines whether the PCS_n pins are active during memory bus cycle or IO bus cycle. Set 1: PCS_n active for memory cycle. Set 0: PCS_n active for IO cycle.
5	PR4	R/W	See bit[1:0] in the A4h register.
4-3	R[4:3]	R/W	See bit[1:0]
2	R2	R/W	Ready Mode. This bit only applies to the PCS6_n – PCS5_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 4-3 and Bit 1-0: R4, R3, R1, R0**, Wait-State Values. R4, R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS5_n – PCS6_n access. **R4, R3, R1, R0 -- Wait States** 0, 0, 0, 0 -- 1 0, 0, 0, 1 -- 3 0, 0, 1, 0 -- 5 0, 0, 1, 1 -- 7 0, 1, 0, 0 -- 9 0, 1, 0, 1 -- 15 0, 1, 1, 0 -- 25 0, 1, 1, 1 -- 40 1, 0, 0, 0 -- 60 1, 0, 0, 1 -- 80

			1, 0, 1, 0 -- 100 1, 0, 1, 1 -- 125 1, 1, 0, 0 -- 150 1, 1, 0, 1 -- 180 1, 1, 1, 0 -- 210 1, 1, 1, 1 -- 255

Midrange Memory Block Size table:

FFAAh bit11-9					
Total Block Size 000	Total Block Size 001	Total Block Size 010	Total Block Size 011	Total Block Size 100	M[6:0]
8K	16K	32K	64K	128K	0000001b
16K	32K	64K	128K	256K	0000010b
32K	64K	128K	256K	512K	0000100b
64K	128K	256K	512K	1M	0001000b
128K	256K	512K	1M	2M	0010000b
256K	512K	1K	2M	4M	0100000b
512K	1M	2M	4M	8M	1000000b

Register Offset: AAh
Register Name: Chip Size Multiplier Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	W[2:0]			M[2:0]			P[2:0]			U[2:0]			L[2:0]		

Bit	Name	Attribute	Description
15	Rsvd	R	Reserved
14-12	W[2:0]	R/W	Wait-State Value. W[2:0] determine the number of wait states inserted into T1 of PCS6_n, PCS5_n, and the PCS3_n – PCS0_n access. **W2, W1, W0 -- <u>Wait States</u>** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 3 0, 1, 1 -- 7 1, 0, 0 -- 11 1, 0, 1 -- 15 1, 1, 0 -- 20 1, 1, 1 -- 31
11-9	M[2:0]	R/W	MCS chip select size multiplier
8-6	P[2:0]	R/W	PCS chip select size multiplier
5-3	U[2:0]	R/W	UCS chip select size multiplier
2-0	L[2:0]	R/W	LCS chip select size multiplier

Register Offset: ACh

Register Name: MCS_n Extended Register

Reset Value : 00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	R4	0	W2	W1	W0

Bit	Name	Attribute	Description
15-5	Rsvd	R/O	Defaulted as 0.
4	R4	R/W	Deaulted as 0. Please see the description for bit 1-0 in the A6h register.
3	Rsvd	RO	Defaulted as 0
2-0	W[2:0]	R/W	T1 Wait-State Value. Defaulted as 0.

12. Refresh Control UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycle. After a period of time, the RCU generates a memory read request to the bus interface unit.

A user guide to program SDRAM:

(1) Configure Lower Memory Chip Select Register (A2h) to set SDRAM space. The suggestion value is 7F38h.

(2) Set Clock Prescalar Register (E2h) and RCU Register (E4h) to enable SDRAM refresh.

Register Offset: E2h
Register Name: Clock Prescalar Register
Reset Value : 0080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RC[14:0]														

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-0	RC[14:0]	RW	Refresh Counter Reload Value. It contains the value of the desired clock count interval between refresh cycles. The counter value should not be set to less than 12h, otherwise there would never be sufficient bus cycle available for the processor to execute code. For Example: SDRAM specification specifies to refresh 1 time every 15.6 u sec and system clock is 25Mhz. The Refresh Counter Reload Value = 15.6us*25Mhz = 15.6us / 40ns = 390.

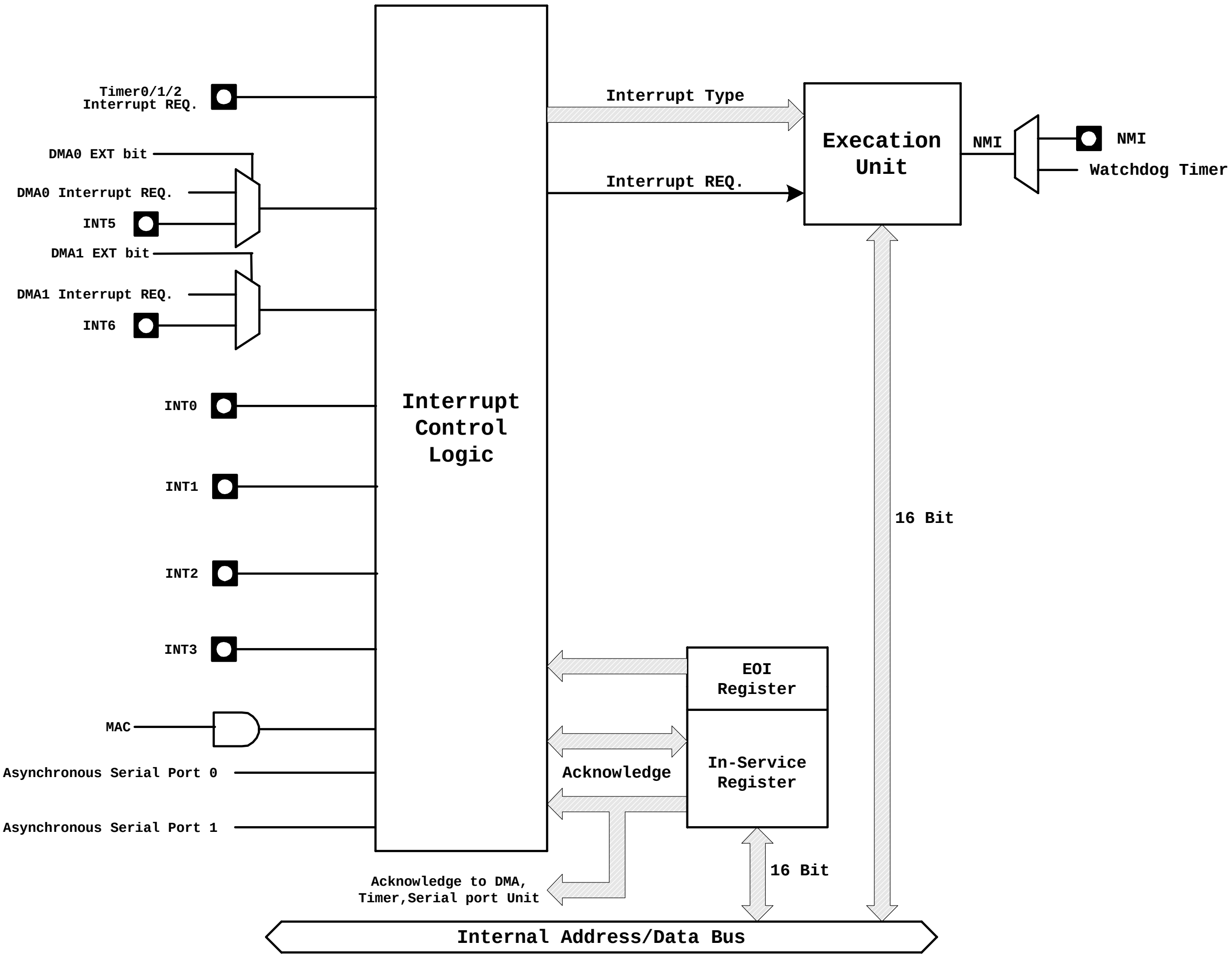
Register Offset: E4h
Register Name: Enable RCU Register
Reset Value : 8000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	T[14:0]														

Bit	Name	Attribute	Description
15	E	RW	Enable RCU Set 1: Enable the refresh counter unit. Set 0: Clear the refresh counter and stop refresh requests, but will not reset the refresh address.
14-0	T[14:0]	RO	Refresh Count. This read-only field contains the present value of the down counter which triggers refresh requests.

13. Interrupt Controller UNIT

There are 17 interrupt request sources connected to the controller: 6 mask able interrupt pins (INT[0:3], INT5, INT6); 2 non-mask able interrupts (NMI, WDT); 9 internal unit request sources (Timer 0, 1, 2; DMA 0, 1; MAC 0,1; Asynchronous Serial Port 0, 1).



Interrupt Control Unit Block Diagram

13.1 Interrupt Vector, Type and Priority

The following table shows the interrupt vector address, type and the priority. The maskable interrupt priority can be changed by programming the priority registers. The vector address for each interrupt was fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Op code Exception	06h	18h		1	
ESC Op code Exception	07h	1Ch		1	
Timer 0	08h	20h	08h	2-1	*
Reserved	09h				
DMA 0/INT5	0Ah	28h	0Ah	3	
DMA 1/INT6	0Bh	2Ch	0Bh	4	
INT0	0Ch	30h	0Ch	5	
INT1	0Dh	34h	0Dh	6	
INT2	0Eh	38h	0Eh	7	
INT3	0Fh	3Ch	0Fh	8	
MAC	10h	40h	10h	9	
Asynchronous Serial port 1	11h	44h	11h	9	
Timer 1	12h	48h	08h	2-2	*
Timer 2	13h	4Ch	08h	2-3	*
Asynchronous Serial port 0	14h	50h	14h	9	
Reserved	15h-1Fh				

Note *: When the interrupt occurs in the same time, the priority is (1-1 > 1-2); (2-1> 2-2 > 2-3)

13.2 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies the interrupt is enabled (the IF flag is enabled and the MSK bit is not set) and that there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-trigger) to request the interrupt controller service, the INT pins must be held till the micro controller entering the interrupt service routine. There is no interrupt-acknowledge output when running in fully nested mode, so it should use PIO pin to simulate the interrupt-acknowledge pin if necessary.

13.3 Programming the Registers

Software is programmed through the registers (44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h) to define the interrupt controller operation.

Register Offset: 44h
Register Name: Serial Port 0 Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 0. Set 0: Enable the serial port 0 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. **The priority selection:** **PR2**, **PR1**, **PR0** -- **Priority** 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

Register Offset: 42h
Register Name: Serial Port 1 Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 1. Set 0: Enable the serial port 1 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. **The priority selection:** **PR2**, **PR1**, **PR0** -- **Priority** 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

Register Offset: 40h

Register Name: MAC Interrupt Control Register

Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enabled. When this bit is set to 1 and bit 4 is cleared to 0, an interrupt is triggered by edge from MAC0 or MAC1, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: the high active level triggers an interrupt. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of MAC. Set 0: Enable the MAC interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as bit 2-0 of the 44h register.

Register Offset: 3Eh
Register Name: INT3 Control Register
Reset Value : 000Fh

15-8	7	6	5	4	3	2	1	0
Reserved	ETM	Rsvd	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enabled. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1 = Falling edge/Low level trigger. Set 0 = Rising edge/High level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by level. Set 0: An interrupt is triggered by edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT3. Set 0: Enable the INT3 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 3Ch
Register Name: INT2 Control Register
Reset Value : 000Fh

15-8	7	6	5	4	3	2	1	0
Reserved	ETM	Rsvd	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enabled. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1 = Falling edge/Low level trigger. Set 0 = Rising edge/High level trigger.
4	LTM	R/W	Level-Triggered Mode.

			Set 1: An Interrupt is triggered by level. Set 0: An interrupt is triggered by edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT2. Set 0: Enable the INT2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 3Ah

Register Name: INT1 Control Register

Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enabled. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1
5	ELS	R/W	Edge/Level Select Set 1: falling edge/Low level trigger Set 0: rising edge/High level trigger
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by level. Set 0: An interrupt is triggered by edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT1. Set 0: Enable the INT1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 38h

Register Name: INT0 Control Register

Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enabled. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by the edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT0
5	ELS	R/W	Edge/Level Select Set 1: Falling edge/Low level trigger. Set 0 : Rising edge/High level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by level. Set 0: An interrupt is triggered by edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT0. Set 0: Enable the INT0 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 36h
Register Name: DMA1/INT6 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	ELS	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1: Falling edge/Low level trigger. Set 0: Rising edge/High level trigger.
4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 34h
Register Name: DMA0/INT5 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	ELS	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1 = Falling edge/Low level trigger. Set 0 = Rising edge/High level trigger.
4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 32h
Register Name: Timer Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the timer controller. Set 0: Enable the timer controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit 2-0 for the 44h register.

Register Offset: 30h
Register Name: Interrupt Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved									MAC1	MAC0	Rsvd	TMR2	TMR1	TMR0

The **reset value** is not defined.

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-mask able interrupts occur. Set 0: When an IRET instruction is executed.
14-6	Rsvd	RO	Reserved
5-4	MAC[1:0]	R/W	Indicate that the corresponding MAC controller has an interrupt request while set to 1.
3	Rsvd	RO	Reserved
2-0	TMR[2:0]	R/W	Indicate that the corresponding timer has an interrupt request pending while set to 1.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5, MAC, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT[3:0] external interrupts, the corresponding bits (I[3:0]) reflect the current values of the external signals.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	RO	Serial Port 0 Interrupt Request. Indicates the interrupt status of the serial port 0.
9	SP1	RO	Serial Port 1 Interrupt Request. Indicates the interrupt status of the serial port 1.
8	MAC	RO	MAC Interrupt Request. Indicates the interrupt status of the MAC1 **or** MAC0.
7-4	I[3:0]	RO	Interrupt Requests. Set 1: The corresponding INT pin has an interrupt pending.
3-2	D1/I6 –	RO	DMA Channel or INT Interrupt Request.

	D0/I5		Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved
0	TMR	RO	Timer Interrupt Request. Set 1: The timer control unit has an interrupt pending.

Register Offset: 2Ch
Register Name: In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

These bits in this Register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	R/W	Serial Port 0 Interrupt In-Service. Set 1: the serial port 0 interrupt is currently being serviced.
9	SP1	R/W	Serial Port 1 Interrupt In-Service. Set 1: the serial port 1 interrupt is currently being serviced.
8	MAC	R/W	MAC In-Service. Indicates the MAC1 **OR** MAC0 interrupt is currently being serviced.
7-4	I[3:0]	R/W	Interrupt In-Service. Set 1: the corresponding INT interrupt is currently being serviced.
3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt In-Service. Set 1: the corresponding DMA channel or INT interrupt is currently being serviced.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt In-Service. Set 1: the timer interrupt is currently being serviced.

Register Offset: 2Ah
Register Name: Priority Mask Register
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

It determines the minimum priority level at which mask able interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved
2-0	PRM[2:0]	R/W	Priority Field Mask, determining the minimum priority that is required in order for a mask able interrupt source to generate an interrupt. **PR[2:0]** **Priority** 000 (High) 0 001 1 010 2 011 3 100 4 101 5 110 6 111 (Low) 7

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10	SP0	R/W	Serial Port 0 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 0 interrupt is masked.
9	SP1	R/W	Serial Port 1 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 1 interrupt is masked.
8	MAC	R/W	MAC Interrupt Mask. When set 1, this bit indicates that the MAC[1:0] interrupts are masked.
7-4	I[3:0]	R/W	External Interrupt Mask. When set 1, I[3:0] bits indicate that the corresponding interrupts are masked.
3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt Masks. When set 1, these bits indicate that the corresponding interrupts are masked.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt Mask. When set 1, this bit indicates that the Timer controller interrupt is masked.

Register Offset: 26h
Register Name: Poll Status Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

The Poll Status (POLLST) register mirrors the current state of the Poll register. The POLLST register can be read without affecting the current interrupt requests.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 24h
Register Name: Poll Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

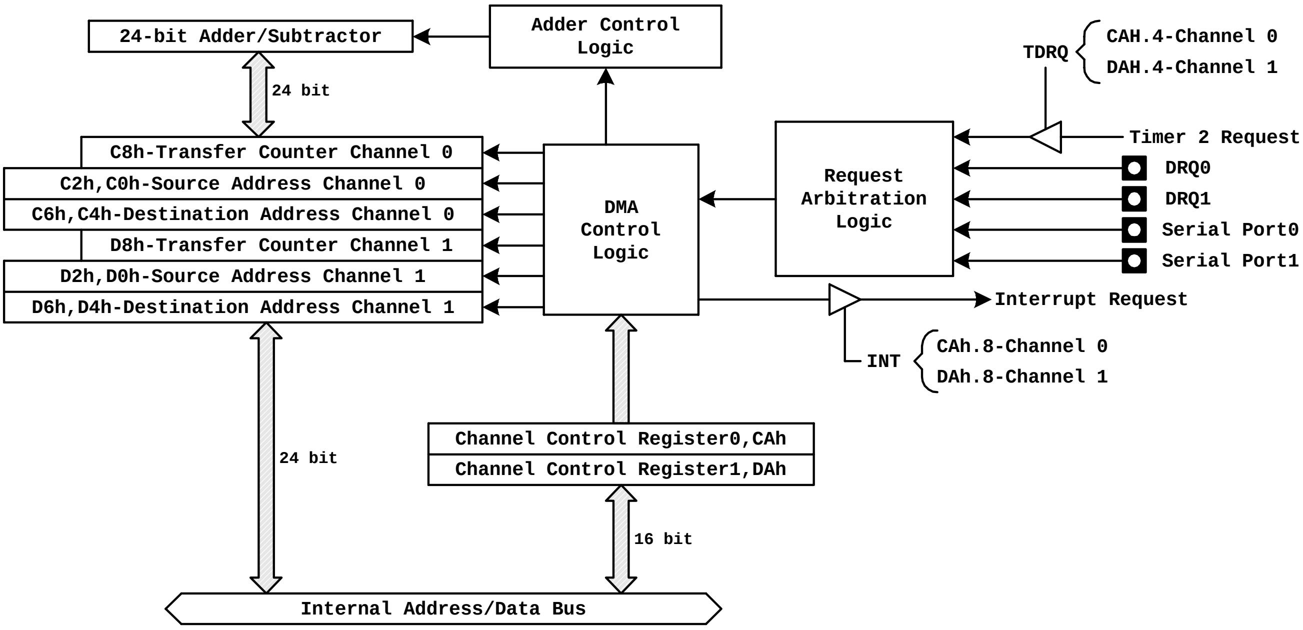
Register Offset: 22h
Register Name: End - Of - Interrupt
Reset Value : Write Only

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSPEC	Reserved										S[4:0]				

Bit	Name	Attribute	Description
15	NSPEC	R/W	Non-Specific EOI. Set 1: indicates non-specific EOI. Set 0: indicates the specific EOI interrupt type in S[4:0].
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	WO	Source EOI Type. It specifies the EOI type of the interrupt that is currently being processed.

14. DMA UNIT

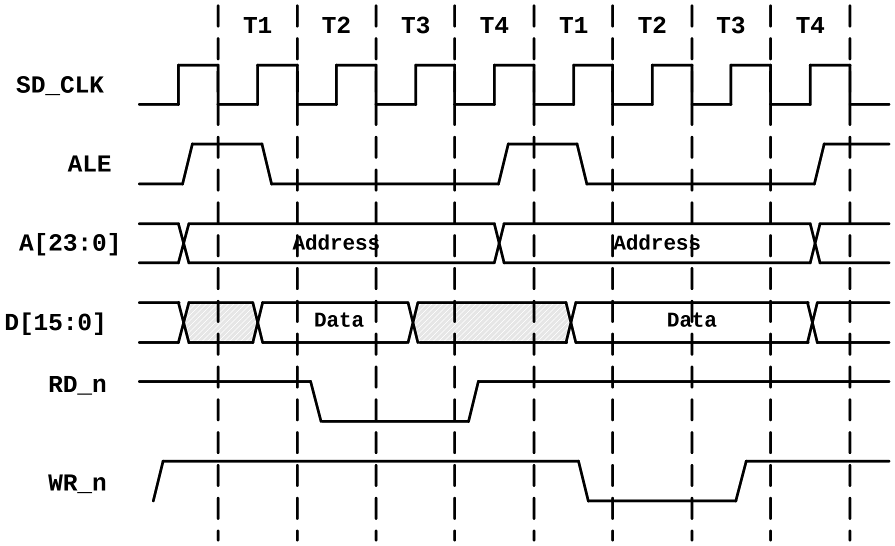
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port 0 or port 1), or Timer 2 overflow. The data transfer from sources to destinations can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (read from sources and write to destinations) for each data transfer.



DMA Unit Block

14.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer) and the two bus cycles cannot be separated by a bus hold request, a refresh request, or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h, and D0h) are used to configure and operate the two DMA channels.



Typical DMA Trarsfer

Register Offset: CAh (DMA0)
Register Name: DMA0 Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

The definitions of Bit [15:0] for DMA0 are the same as those of Bit [15:0] of Register DAh for DMA1.

Register Offset: C8h (DMA0)
Register Name: DMA0 Transfer Count Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 0 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: C6h (DMA0)
Register Name: DMA0 Destination Address High Register
Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="8">DDA[23:16]</td></tr>
</table>

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DDA[23:16]	R/W	High DMA 0 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: C4h (DMA0)
Register Name: DMA0 Destination Address Low Register
Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">DDA[15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: C2h (DMA0)
Register Name: DMA0 Source Address High Register
Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="8">DSA[23:16]</td></tr>
</table>

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DSA[23:16]	R/W	High DMA 0 Source Address. These bits are mapped to A[23:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: C0h (DMA0)
Register Name: DMA0 Source Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 0 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA [23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: DAh (DMA1)
Register Name: DMA1 Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

Bit	Name	Attribute	Description
15	DM/IO_n	R/W	Destination Address Space Select. Set 1: The destination address is in memory space. Set 0: The destination address is in I/O space.
14	DDEC	R/W	Destination Decrement. Set 1: The destination address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decrement value, which is by 1 or 2 when both DDEC and DINC bits are set to 1 or 0. The address remains constant. Set 0: Disable the decrement function.
13	DINC	R/W	Destination Increment. Set 1: The destination address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the increment function.
12	SM/IO_n	R/W	Source Address Space Select. Set 1: The Source address is in memory space. Set 0: The Source address is in I/O space.
11	SDEC	R/W	Source Decrement. Set 1: The Source address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decremented value is by 1 or 2 when both SDEC and SINC bits are set to 1 or 0. The address remains constant. Set 0: Disable the decrement function.

10	SINC	R/W	Source Increment. Set 1: The Source address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the decrement function.
9	TC	R/W	Terminal Count. Set 1: The synchronized DMA transfer is terminated when the DMA Transfer Count Register reaches 0. Set 0: The synchronized DMA transfer is not terminated when the DMA Transfer Count Register reaches 0. Unsynchronized DMA transfer is always terminated when the DMA transfer count register reaches 0, regardless of the setting of this bit.
8	INT	R/W	Interrupt. Set 1: DMA unit generates an interrupt request when the transfer count is completed. The TC bit must be set to 1 to generate an interrupt.
7-6	SYN[1:0]	R/W	Synchronization Type Selection. **SYN1** , **SYN0** -- **Synchronization Type** 0 , 0 -- Unsynchronized 0 , 1 -- Source synchronized 1 , 0 -- Destination synchronized 1 , 1 -- Reserved
5	P	R/W	Priority. Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.
4	TDRQ	R/W	Timer Enable/Disable Request. Set 1: Enable the DMA requests from timer 2. Set 0: Disable the DMA requests from timer 2.
3	EXT	R/W	This bit enables the external interrupt functionality of the corresponding DRQ pin. Set 1: the external pin is an INT pin and requests on the pin are passed to the interrupt controller. Set 0: The pin functions as a DRQ pin.
2	CHG	R/W	Changed Start Bit. This bit must be set to 1 when the ST bit is modified.
1	ST	R/W	Start/Stop DMA channel. Set 1: Start the DMA channel Set 0: Stop the DMA channel
0	B_n/W	R/W	Byte/Word Select. Set 1: The address is incremented or decremented by 2 after each transfer. Set 0:The address is incremented or decremented by 1 after each transfer. Only byte transfer is supported if either source or destination bus width is 8 bit.

Register Offset: D8h (DMA1)
Register Name: DMA1 Transfer Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 1 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: D6h (DMA1)
Register Name: DMA1 Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DDA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DDA[23:16]	R/W	High DMA 1 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: D4h (DMA1)
Register Name: DMA1 Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 1 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: D2h (DMA1)
Register Name: DMA1 Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DSA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DSA[23:16]	R/W	High DMA 1 Source Address. These bits are mapped to A[23:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: D0h (DMA1)
Register Name: DMA1 Source Address Low Register
Reset Value : ——

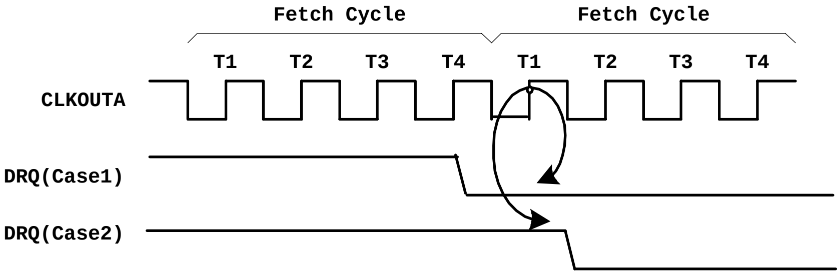
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 1 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA[23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

14.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of SD_CLK. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects (PCSx_n) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

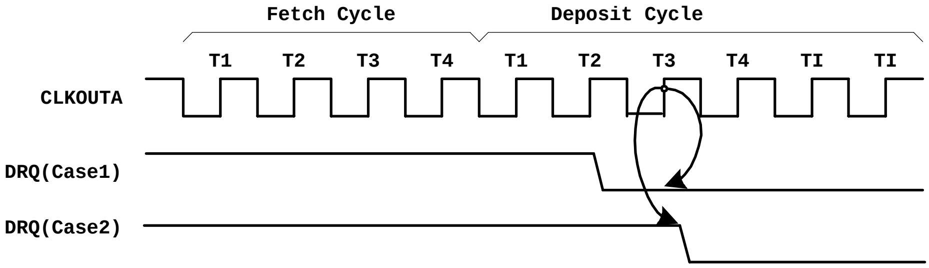
DMA transfer can be either source- or destination-synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer, which provides the source device at least three clock cycles from the time. It is acknowledged to dessert its DRQ line.



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer, which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NOTES:
Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

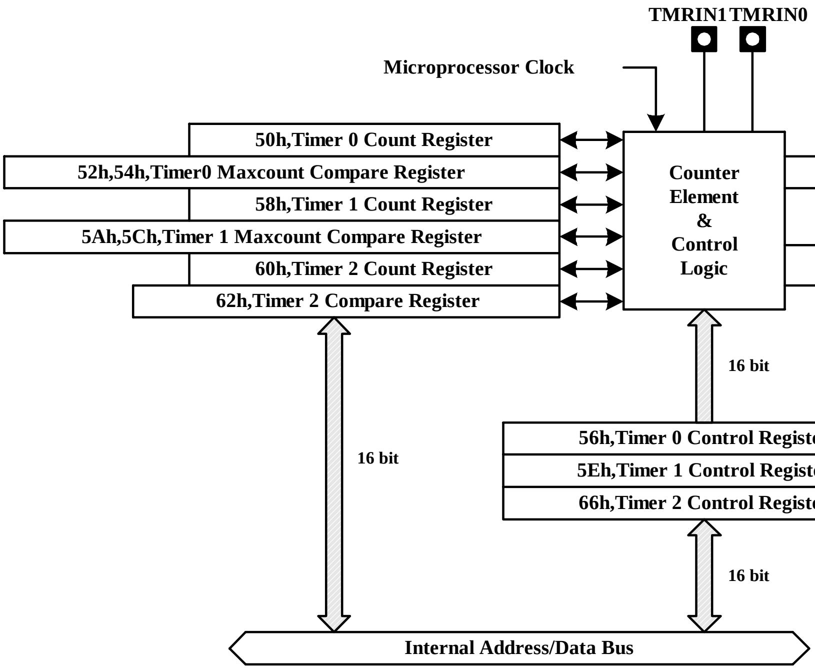
Destination-Synchronized Transfers

14.3 Serial Port/DMA Transfer

The serial port data can be DMA transfer to or from memory or I/O space. And the B_n/W bit of the DMA Control Register must be set to 0 for byte transfer. The map address of the Transmit Data Register is written to the DMA Destination Address Register and the memory or I/O address is written to the DMA Source Address Register, when the data are transmitted. The map address of the Receive Data Register is written to the DMA Source Address Register and the memory or I/O address is written to the DMA Destination Address Register, when the data are received.

The software is programmed through the Serial Port Control Register to perform the serial port/ DMA transfer. When a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated. For DMA to the serial port, the DMA channel should be configured as being destination-synchronized. For DMA from the serial port, the DMA channel should be configured as source-synchronized.

15. Timer Control UNIT



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R2020C. The timer operation is independent of the CPU. These three timers can be programmed as a timer element or as a counter element. Timer 0 and 1 are each connected to two external pins (TMRIN0, TMROUT0, TMRIN1, TMROUT1), which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected any external pins. It can be used as a prescalar to Timer 0 and Timer 1 or as a DMA request source.

Register Offset: 56h
Register Name: Timer 0 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

The definitions for Timer 0 are the same as those of Register 5Eh for Timer 1.

Register Offset: 50h
Register Name: Timer 0 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Count Value. This register contains the current count of Timer 0. The count is incremented by one every **8** internal processor clocks, or prescaled by Timer 2, or incremented by one every 8 external clock which is configured the external clock select bit to refer to the TMRIN1 signal.

Register Offset: 52h
Register Name: Timer 0 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare A Value.

Register Offset: 54h
Register Name: Timer 0 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare B Value.

Register Offset: 5Eh
Register Name: Timer 1 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: The timer 1 is enabled. Set 0: The timer 1 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n bit and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n bit and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time the count reaches Max-Count A or Max-Count B. Set 0: Timer 1 will not issue interrupt request.
12	RIU	R/W	Register in Use Bit. Set 1: The Maxcount Compare B Register of timer 1 is being used. Set 0: The Maxcount Compare A Register of timer 1 is being used.
11-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set as each time either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the EN bit (offset 5Eh [15]).
4	RTG	R/W	Re-trigger Bit. This bit defines the control function by the input signal of TMRIN1 pin. When EXT=1 (5Eh.2), this bit is ignored. Set 1: Timer1 Count Register (58h) counts internal events; Reset the counting on every TMRIN1 input signal going from low to high (rising edge trigger). Set 0: Low input holds the timer 1 Count Register (58h) value; High input enables the counting which counts the internal events. **The definition of setting the (EXT, RTG)** (0, 0) – Timer1 counts the internal events. if the TMRIN1 pin remains high. (0, 1) – Timer1 counts the internal events; count register resets on every rising transition on the TMRIN1 pin. (1, x) – TMRIN1 pin input acts as a clock source and timer1 count register is incremented by one every 8 external clocks.
3	P	R/W	Prescalar Bit. This bit and EXT bit (5Eh [2]) define the timer 1 clock source. **The definition of setting the (EXT, P)** (0, 0) – Timer1 Count Register is incremented by one every 8 internal processor clocks. (0, 1) – Timer1 Count Register is incremented by one which is prescaled by Timer 2. (1, x) – TMRIN1 pin input acts as a clock source and Timer1 Count Register is incremented by one every 8 external clocks.
2	EXT	R/W	External Clock Bit. Set 1: Timer 1 clock source from external.

			Set 0: Timer 1 clock source from internal.
1	ALT	R/W	Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode. Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A, then resets the count register to 0. The timer counts to Maxcount Compare B, then resets the count register to 0 again, and starts over with Maxcount Compare A. Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and reset to 0, and then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer runs continuously. Set 0: The timer will halt after each counting to the maximum count and EN bit will be cleared.

Register Offset: 58h

Register Name: Timer 1 Count Register

Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">TC[15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every 8 internal processor clocks, prescaled by Timer 2, or incremented by one every 8 external clocks which is configured as the external clock select bit to refer to the TMRIN1 signal.

Register Offset: 5Ah

Register Name: Timer 1 Maxcount Compare A Register

Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">TC[15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare A Value.

Register Offset: 5Ch
Register Name: Timer 1 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare B Value.

Register Offset: 66h
Register Name: Timer 2 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: Timer 2 is enabled. Set 0: Timer 2 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. Set 0: Timer 2 will not issue interrupt request.
12-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the EN bit (66h.15).
4-1	Rsvd	RO	Reserved
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer is continuously running when it reaches the maximum count. Set 0: The EN bit (66h [15]) is cleared and the timer is held after each timer count reaches the maximum count.

Register Offset: 60h
Register Name: Timer 2 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Count Value. This register contains the current count of Timer 2. The count is incremented by one every 8 internal processor clocks.

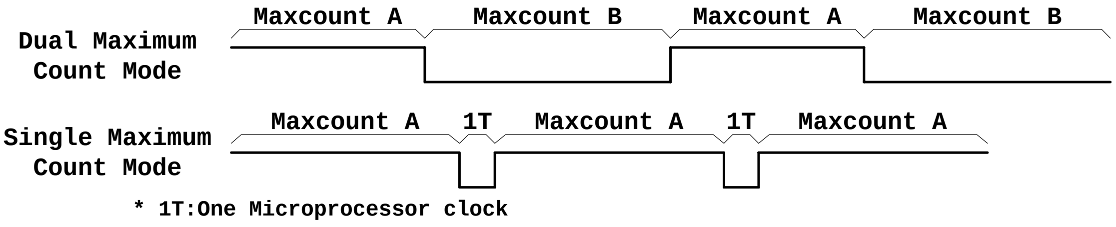
Register Offset: 62h
Register Name: Timer 2 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Compare A Value.

15.1 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and Timer1 can be configured to be a single or dual maximum count mode. The TMROUT0 or TMROUT1 signals can be used to generate waveforms of various duty cycles.



Timer/Counter Unit Output Modes

15.2 Watchdog Timer

The R2020C has one independent watchdog timer, which is programmable. **The watchdog timer is active after reset** and the timeout count with a maximum count value. The keyed sequence (3333h, CCCCh) must be written to the register (E6h) first, then the new configuration to the Watchdog Timer Control Register. It is a single write, so every writing to the Watchdog Timer Control Register will follow this rule.

When the watchdog timer activates, an internal counter is counting. If this internal count is over the watchdog timer duration, the watchdog timeout happens. The keyed sequence (AAAAh, 5555h) must be written to the register (E6h) to reset the internal count and prevent the watchdog timeout. The internal count should be reset before the Watchdog Timer timeout period is modified to ensure that an immediate timeout will not occur.

Register Offset: E6h
Register Name: Watchdog Timer Control Register
Reset Value : C080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	WRST	RSTFLAG	NMIFLAG	Rsvd				COUNT							

Bit	Name	Attribute	Description
15	ENA	R/W	Enable Watchdog Timer. Set 1: Enable Watchdog Timer. Set 0: Disable Watchdog Timer.
14	WRST	R/W	Watchdog Reset. Set 1: WDT generates a system reset when WDT timeout count is reached. Set 0: WDT generates an NMI interrupt when WDT timeout count is reached if the NMIFLAG bit is 0. If the NMIFLAG bit is 1, the WDT will generate a system reset when timeout.
13	RSTFLAG	R/W	Reset Flag. When watchdog timer reset event has occurred, hardware will set this bit to 1. This bit will be cleared by any keyed sequence write to this register or external reset. This bit is 0 after an external reset or 1 after a watchdog timer reset.
12	NMIFLAG	R/W	NMI Flag. After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence written to this register.
11-8	Rsvd	RO	Reserved

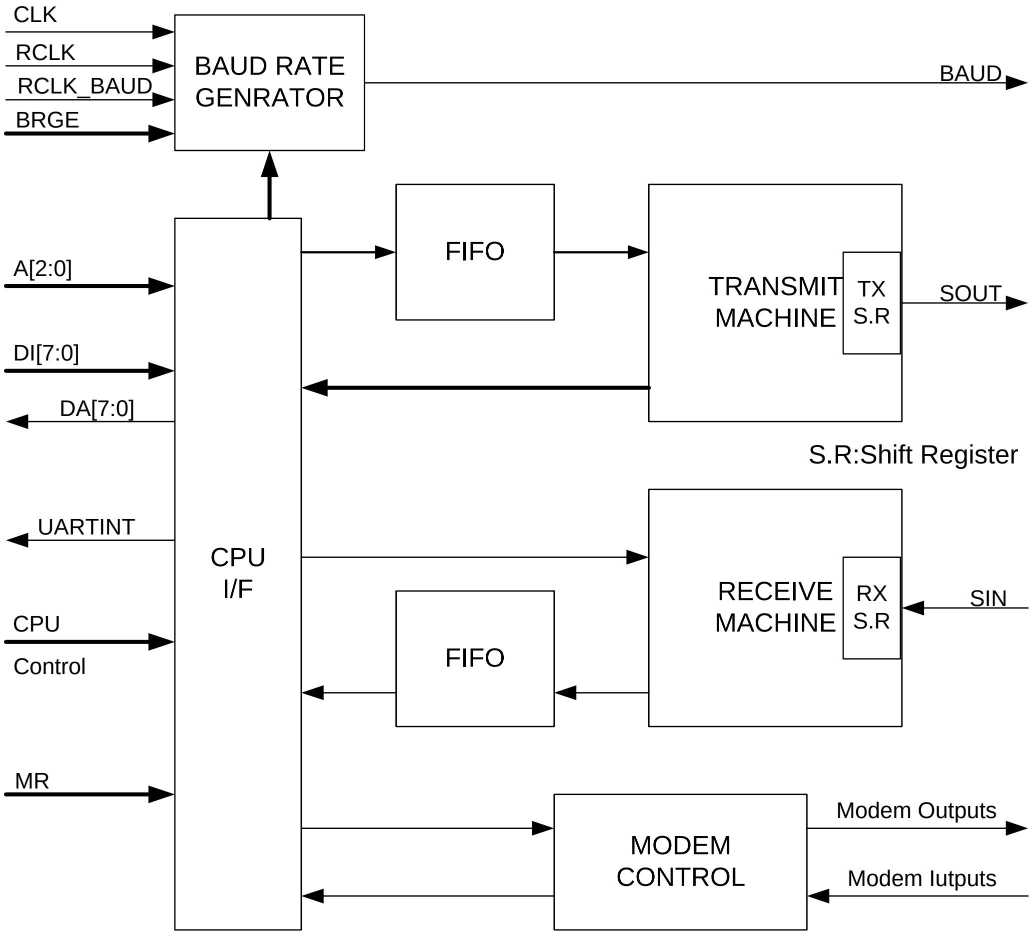
<table>
<tr><td rowspan="4">7-0</td><td rowspan="4">COUNT</td><td rowspan="4">R/W</td><td colspan="9">Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.
a. The duration equation: **Duration =(2^{Exponent}) / (Frequency/2)**
b. The Exponent of the COUNT setting:
(Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent)
(0 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (N/A)
(x , x , x , x, x , x , x , 1) = (10)
(x , x , x , x, x , x , 1 , 0) = (20)
(x , x , x , x, x , 1 , 0 , 0) = (21)
(x , x , x , x, 1 , 0 , 0 , 0) = (22)
(x , x , x , 1, 0 , 0 , 0 , 0) = (23)
(x , x , 1 , 0, 0 , 0 , 0 , 0) = (24)
(x , 1 , 0 , 0, 0 , 0 , 0 , 0) = (25)
(1 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (26)
c. Watchdog timer Duration reference table:
For example: System clock =100Mhz and frequency exponent=10, then
Duration = 2^{10} **/** (100Mhz / 2) = 2048 / 100Mhz = 20.48 us</td></tr>
<tr><td>**Frequency\ Exponent**</td><td>**10**</td><td>**20**</td><td>**21**</td><td>**22**</td><td>**23**</td><td>**24**</td><td>**25**</td><td>**26**</td></tr>
<tr><td>**75 MHz**</td><td>27.3 us</td><td>28 ms</td><td>55.9 ms</td><td>111.8 ms</td><td>223.7 ms</td><td>447.4 ms</td><td>894.8 ms</td><td>1.79 s</td></tr>
<tr><td>**100 MHz**</td><td>20.5 us</td><td>21 ms</td><td>41.9 ms</td><td>83.9 ms</td><td>167.8 ms</td><td>335.5 ms</td><td>671 ms</td><td>1.34 s</td></tr>
</table>

16. 16550 UART Serial Port

The system programmer may access any of the UART registers summarized in the following Table via the CPU. These registers control the UART operation in which the transmission and reception of data and status are included, and each register bit in the Table has its own name.

Register Address	**Register Name**	**Mnem.**	**Bit No.**									**Note.**
			15-8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
80h/10h	Receiver Buffer Register	**RBR**	0	RBR[7]	RBR[6]	RBR[5]	RBR[4]	RBR[3]	RBR[2]	RBR[1]	RBR[0]	DLAB=0 & read only
	Transmitter Holding Register	**THR**	0	THR[7]	THR[6]	THR[5]	THR[4]	THR[3]	THR[2]	THR[1]	THR[0]	DLAB=0 & write only
	Divisor Latch(LS)	**DLL**	0	DL[7]	DL[6]	DL[4]	DL[4]	DL[3]	DL[2]	DL[1]	DL[0]	DLAB=1
82h/12h	Interrupt Enable Register	**IER**	0	0	0	0	0	EMSI	ERLSI	ETHREI	ERDAI	DLAB=0
	Divisor Latch(MS)	**DLM**	0	DL[15]	DL[14]	DL[13]	DL[12]	DL[11]	DL[10]	DL[9]	DL[8]	DLAB=1
84h/14h	Interrupt Identified Register	**IIR**	0	FIFO Enabled (Note)	FIFO Enabled (Note)	0	0	IID[2]	IID[1]	IID[0]	IP	Read Only
	FIFO Control Register	**FCR**	DMAC TL2-0	RCVR Trigger Level (MSB)	RCVR Trigger Level (LSB)	Reserved	Reserved	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled	Write Only
86h/16h	Line Control Register	**LCR**	0	DLAB	SB	SP	EPS	PEN	STB	WLS[1]	WLS[0]	
88h/18h	MODEM Control Register	**MCR**	0	0	0	ACE	Loop	LDCD	LRI	RTS	DTR	
8Ah/1Ah	Line Status Register	**LSR**	0	Error in RCVR FIFO (Note)	TEMT	THRE	BI	FE	PE	OE	DR	
8Ch/1Ch	MODEM Status Register	**MSR**	0	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS	
8Eh/1Eh	Scratch Register	**SCR**	0	SCR[7]	SCR[6]	SCR[5]	SCR[4]	SCR[3]	SCR[2]	SCR[1]	SCR[0]	

Note: These bits are always 0 in the 16450 mode.



UART Block Diagram

16.1 Receiver Buffer Register and Transmitter Holding Register

Register Offset: 80h
Register Name: UART0 Receiver Buffer Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								RBR [7:0]							

This register is Receiver Buffer Register when DLAB=0 and the read function is operated.

Register Offset: 80h
Register Name: UART0 Transmitter Holding Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								THR [7:0]							

This register is Transmitter Holding Register when DLAB=0 and the write function is operated.

16.2 Divisor Latch LS and MS Register

The divisor value, DLL[15:0], is the host clock / 16 / Baud Rate.

For example:

Host Clock=75Mhz, and Baud Rate=57600, then

Divisor=75Mhz/16/57600=81.3 → 81

Register Offset: 80h
Register Name: UART0 Divisor Latch (LS) Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [7:0]							

This register is Divisor Latch (LS) Register when DLAB=1.

Register Offset: 82h
Register Name: UART0 Divisor Latch (MS) Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [15:8]							

This register is Divisor Latch (MS) Register when DLAB=1.

16.3 Interrupt Enable Register

This Interrupt Enable Register (IER) enables the four types of UART interrupts. Each interrupt can individually activate the interrupt output signal (UARTINT). It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, setting the relative bit of the IER register to 1 will enable the selected interrupt(s). Disabling an interrupt prevents it from being indicated as being active in the IIR and from activating the UARTINT output signal. All other system functions operate in their normal manners, including the setting of the Line Status and MODEM Status Registers. The details of each bit of the IER are described as below:

Register Offset: 82h
Register Name: UART0 Interrupt Enable Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	BMSI	ERLSI	ETHREI	ERDAI

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved and always 0.
3	EMSI	R/W	The MODEM Status Interrupt bit. Set to 1 to enable the MODEM Status Interrupt.
2	ERLSI	R/W	The Enable Receiver Line Status Interrupt bit. Set to 1 to enable the Receiver Line Status Interrupt.
1	ETHREI	R/W	The Enable Transmitter Holding Register Empty Interrupt bit. Set to 1 to enable the Transmitter Holding Register Empty Interrupt.
0	ERDAI	R/W	The Enable Received Data Interrupt bit. Set to 1 to enable the Received Data Available Interrupt (and timeout interrupts in the FIFO mode).

16.4 Interrupt Identification Register

This is a read only register. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register (IIR). The four levels of interrupt conditions in priority order are Receiver Line Status, Received Data Ready, Transmitter Holding Register Empty, and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. The details of each bit of Interrupt Identification Register are described as below.

Register Offset: 84h
Register Name: UART0 Interrupt Identified. Register (Read Only)
Reset Value : XX01h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								FIFOs Enabled	FIFOs Enabled	0	0	IID2	IID1	IID0	IP

Bit	Name	Attribute	Description
7-6	FIFOs Enabled	R/W	These two bits are set when FCR [0]=1.
5-4	Rsvd	RO	Reserved and always 0.
3	IID2	R/W	The Interrupt ID indicator. In the NS16450 Mode, this bit is 0. In the FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2-1	IID[1:0]	R/W	The Interrupt ID indicator. These two bits are used to identify the highest priority interrupt pending as indicated in the following table:
0	IP	R/W	The Interrupt Pending indicator. This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending or not. Set 1: Indicate that no interrupt is pending. Set 0: Indicate that an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

Interrupt Control Function:

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Rest Control**
0	0	0	1	—	None	none	—
0	1	1	0	Highest	Receiver Line Status	overrun error, parity error, framing error, or break interrupt	reading the line status register
0	1	0	0	Second	Received Data Available	received data available or trigger level reached	reading the receiver buffer register or the FIFO dropping below the trigger level
1	1	0	0	Second	Character Timeout Indication	no character has been removed from or input to the RCVR FIFO during the last 4 characters times and there is at least 1 character in it during this time	reading the receiver buffer register
0	0	1	0	Third	Transmitter Holding Register Empty	transmitter holding register empty	reading the IIR register (if the source of interrupt is available) or writing into the transmitter holding register
0	0	0	0	Fourth	MODEM Status	clear to send, data set ready, ring indicator, or data carrier detect	reading the modem status register

16.5 FIFO Control Register

The FIFO Control Register (write only) is at the same location as the Interrupt Identification Register (read only). This register is used to enable the FIFO, clear the FIFO, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Register Offset: 84h
Register Name: UART0 FIFO Control Register (Write Only)
Reset Value : X000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					DMACTL[2:0]			RCVR Trigger (MSB)	RCVR Trigger (LSB)	Rsvd		DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled

Bit	Name	Attribute	Description
10-8	DMACTL [2:0]	R/W	With the DMA transfers listed as follows, users can configure these bits for the UART Port. **DMACTL [2:0]** **Receive** **Transmit** 000 No DMA No DMA 001 DMA0 DMA1 010 DMA1 DMA0 011 Reserved Reserved 100 DMA0 No DMA 101 DMA1 No DMA 110 No DMA DMA0 111 No DMA DMA1
7-6	RCVRTL [1:0]	R/W	RCVR Trigger. These two bits are used to set the trigger level for the RCVR FIFO interrupt. **RCVRTL[1:0] – RCVR FIFO Trigger Level (Bytes)** 0 0 -- 01 Bytes 0 1 -- 04 Bytes 1 0 -- 08 Bytes 1 1 -- 14 Bytes
5-4	Rsvd	RO	Reserved
3	DMA Mode Select	R/W	DMA Mode Select. Setting FCR0[3]=1 will cause the UART to change from mode 0 to mode 1 if FCR0[0]=0.
2	XMIT FIFO Reset	R/W	XMIT FIFO Reset. Writing a 1 to FCR0[2] clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
1	RCVR FIFO Reset	R/W	RCVR FIFO Reset. Writing a 1 to FCR0[1] clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is

			self-clearing.
0	FIFO Enabled	R/W	FIFO Enable. Writing a 1 to FCR0 enables both the XMIT and RCVR FIFO. Resetting FCR0[0] will clear all bytes in both FIFO. When changing from FIFO Mode to NS16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when written to other FCR bits or they will not be programmed.

16.6 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The detailed contents of each bit of LCR register is as follows:

Register Offset: 86h
Register Name: UART0 Line Control Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLAB	Set Break	Stick Parity	EPS	PEN	STB	WSL1	WSL0

Bit	Name	Attribute	Description
7	DLAB	RW	Divisor Latch Access bit. Set 1: To access the Divisor Latches of the Baud Generator during a Read or Write operation. Set 0: To access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register
6	SB	R/W	Break Control bit. It causes a break condition to be transmitted to the receiving UART. Set 1: the serial output (SOUT) is forced to the Spacing (logic 0) state. Set 0: the Break is disabled. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. ***Note:*** *This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.* *1.Load an all Os, pad character, in response to THRE.* *2.Set break after the next THRE.* *3.Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.* *During the break, the Transmitter can be used as a character timer to accurately establish the break duration.*
5	SP	R/W	Stick Parity bit. Set Bit 5=1, Bit 4=1, & Bit 3=1, the Parity bit is transmitted and checked as logic 0.

			Set Bit 5=1, Bit 4=0, & Bit 3=1, the Parity bit is transmitted and checked as logic 1. Set Bit 5=0, Stick Parity is disabled.
4	EPS	R/W	Even Parity Select bit. Set Bit 4=0 & Bit 3=1, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. Set Bit 4=1 & Bit 3=1, an even number of logic 1s is transmitted or checked.
3	PEN	R/W	Parity Enable bit. Set 1: A Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)
2	STB	R/W	Stop bit. This bit specifies the number of Stop bits transmitted and received in each serial character. Set 0: One Stop bit is generated in the transmitted data. Set 1: One and a half stop bits are generated for a 5-bit word length characters. Two stop bits are generated for 6-, 7-, or 8-bit word length characters. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1-0	WLS[1:0]	R/W	These two specify the number of bits in each transmitted or received serial character. **WLS[1:0] -- Character Length** 0 0 -- 5-bit character 0 1 -- 6-bit character 1 0 -- 7-bit character 1 1 -- 8-bit character

---

16.7 Modem Control Register

This Modem Control Register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The details are described as below:

Register Offset: 88h
Register Name: UART0 MODEM Control Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	ACE	Loop	LDCD	LRI	RTS	DTR

Bit	Name	Attribute	Description
7-6	Rsvd	RO	Reserved and always 0.
5	ACE	R/W	Autoflow Control is Enabled when set. ACE can be configured by MCR bits 1and 5 as shown in the following table. MCR bit5(AFE) MCR bit1(RTS)

<table>
<tr><td rowspan="3"></td><td rowspan="3"></td><td rowspan="3"></td><td>1</td><td>1</td><td>Auto-RTS and auto-CTS enabled</td></tr>
<tr><td>1</td><td>0</td><td>Auto-CTS enabled</td></tr>
<tr><td>0</td><td>X</td><td>AFE disabled</td></tr>
<tr><td>4</td><td>Loop</td><td>R/W</td><td colspan="3">This bit provides a local loop back feature for diagnostic testing of the UART.
Set to 1, the following occur:
The transmitter Serial Output (SOUT) is set to the Marking (logic 1) state. The receiver Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input. The four MODEM Control inputs (CTS_n, DSR_n, RI_n, and DCD_n) are disconnected, and the 2 MODEM Control outputs (DTR_n and RTS_n) are internally connected to the two MODEM Control inputs (DSR_n, CTS_n), and the MODEM Control output pins are forced to their inactive state (high).
In the diagnostic mode, data transmitted are immediately received. This feature allows the processor to verify the transmitted and received data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the sources of the interrupts are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.</td></tr>
<tr><td>3, 2</td><td>LDCD,
LRI</td><td>R/W</td><td colspan="3">Bit3: The bit controls DCD_n signal internal if loop back mode is enabled.
Bit2: The bit controls RI_n signal internal if loop back mode is enabled.</td></tr>
<tr><td>1</td><td>RTS</td><td>R/W</td><td colspan="3">The Request To Send bit. This bit controls the Request To Send (RTS_n) output.
Set 1: the RTS_n output is forced to logic 0.
Set 0: the RTS_n output is forced to logic 1.</td></tr>
<tr><td>0</td><td>DTR</td><td>R/W</td><td colspan="3">The Data Terminal Ready indicator. This bit controls the Data Terminal Ready (DTR_n) output.
Set 1: the DTR_n output is forced to logic 0.
Set 0: the DTR_n output is forced to logic 1.
Note: <i>The DTR_n output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.</i></td></tr>
</table>

16.8 Line Status Register

This register provides status information to the part of the CPU processing data transfer. The contents of each Bit of the Line Status Register are described as below.

Register Offset: 8Ah
Register Name: UART0 Line Status Register
Reset Value : XX60h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Error in RCVR (Note 2)	TEMT	THRE	BI	FE	PE	OE	DR

Bit	Name	Attribute	Description
7	Error in RCVR	R/W	Error in Receive FIFO. In the NS16450 Mode, this is a 0. In the FIFO mode, LSR [7] is set to 1 when there is

	(Note 2)		at least one parity error, framing error or break indication in the FIFO. LSR [7] is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO. ***Note:*** *The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.*
6	TEMT	R/W	The Transmitter Empty indicator. Set 1: This bit is set to 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. Set 0: This bit is reset to 0 whenever either the Transmitter Holding Register or the Transmitter Shift Register contains a data character. In the FIFO mode, this bit is set to one whenever the transmitter FIFO and shift register are both empty.
5	THRE	R/W	The Transmitter Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high. Set 1: This bit will be set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. Set 0: This bit is reset to 0 upon the CPU loading character to the Transmitter Holding Register. In the FIFO mode, this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.
4	BI	R/W	Break Interrupt indicator. Set 1: This bit will be set to 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + Data Bits + Parity Bit + Stop Bit). Set 0: This bit will be reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit. ***Note:*** *Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.*
3	FE	R/W	Framing Error indicator. This bit indicates that the received characters don’t have a valid Stop Bit. Set 1: This bit will be set to 1 whenever the Stop Bit follows the last data bit or Parity bit is detected as a logic 0 bit (Spacing level). Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error occurs. To do this, it assumes that the framing error was due to the next start bit, so it samples this “start” bit twice and then takes in the “data”.
2	PE	R/W	Parity Error indicator. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. Set 1: This bit will be set upon detection of a parity error. Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it

			applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.
1	OE	R/W	Overrun Error indicator. This bit indicates that the data in the Receiver Buffer Register were not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. Set 1: Indicate OE indicator is set to logic 1 upon detection of an overrun condition. Set 0: Automatic reset to 0 whenever the CPU reads the contents of the Line Status Register. If the data in the FIFO mode continue to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
0	DR	R/W	Data Ready indicator. Set 1: Indicate whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Set 0: Automatic set to 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

16.9 Modem Status Register

This Modem Status Register (MSR) provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to logic 1 whenever a control input from the MODEM changes its state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. The contents of the MSR register are described as below.

Register Offset: 8C
Register Name: UART0 MODEM Status Register
Reset Value : XXX0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit	Name	Attribute	Description
7	DCD	R/W	Data Carrier Detect. This bit is the complement of the Data Carrier Detect (DCD_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT2 in the MCR.
6	RI	R/W	Ring Indicator. This bit is the complement of the Ring Indicator (RI_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	DSR	R/W	Data Set Ready. This bit is the complement of the Data Set Ready (DSR_n) input.

			If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	CTS	R/W	Clear To Send. This bit is the complement of the Clear to Send (CTS_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	DDCD	R/W	Delta Data Carrier Detect. This bit indicates that the DCD_n input has changed the state. ***Note:** Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.*
2	TERI	R/W	Trailing Edge Ring Indicator. This bit indicates that the RI_n input has changed from a low to a high state.
1	DDSR	R/W	Delta Data Set Ready. This bit indicates that the DSR_n input has changed the state since the last time it was read by the CPU.
0	DCTS	R/W	Delta Clear To Send. This bit indicates that the CTS_n input has changed the state since the last time it was read by the CPU.

16.10 Scratchpad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Register Offset: 8E
Register Name: UART0 Scratch Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SCR[7:0]							

16.11 Programmable Baud Generator

The UART contains a programmable Baud Generator that is divided by any divisor from 2 to 2^{16}-1.. The output frequency of the Baud Generator is 16 times the Baud [divisor # = (CPU frequency)/(baud rate*16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Baud Rates	CPUCLK=75MHz				CPUCLK=100MHz			
	DLM	DLL	Baud	Dev.(%)	DLM	DLL	Baud	Dev.(%)
1200	0Fh	42h	1200	0	14h	58h	1200	0
2400	07h	A1h	2400	0	0Ah	2Ch	2400	0
4800	03h	D1h	4798	0.04	05h	16h	4800	0
9600	01h	E8h	9606	0.06	02h	8Bh	9601	0
19200	0h	F4h	19211	0.06	01h	46h	19171	0.15
38400	0h	7Ah	38422	0.06	0h	A3h	38344	0.15
57600	0h	51h	57870	0.5	0h	6Dh	57339	0.45
115200	0h	29h	114329	0.76	0h	36h	115741	0.47
230400	0h	14h	234375	1.73	0h	1Bh	231481	0.47
460860	0h	0Ah	468750	1.71	0h	0Eh	446428	3.13

16.12 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR [0]=1, IER [0]=1), RCVR interrupt will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.

D. The data ready bit (LSR [0]) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

—at least one character is in the FIFO.

—the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).

—the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 BAUD with a 12-bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred: It is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred: The timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR [0]=1, IER [1]=1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

16.13 FIFO Polled Mode Operation

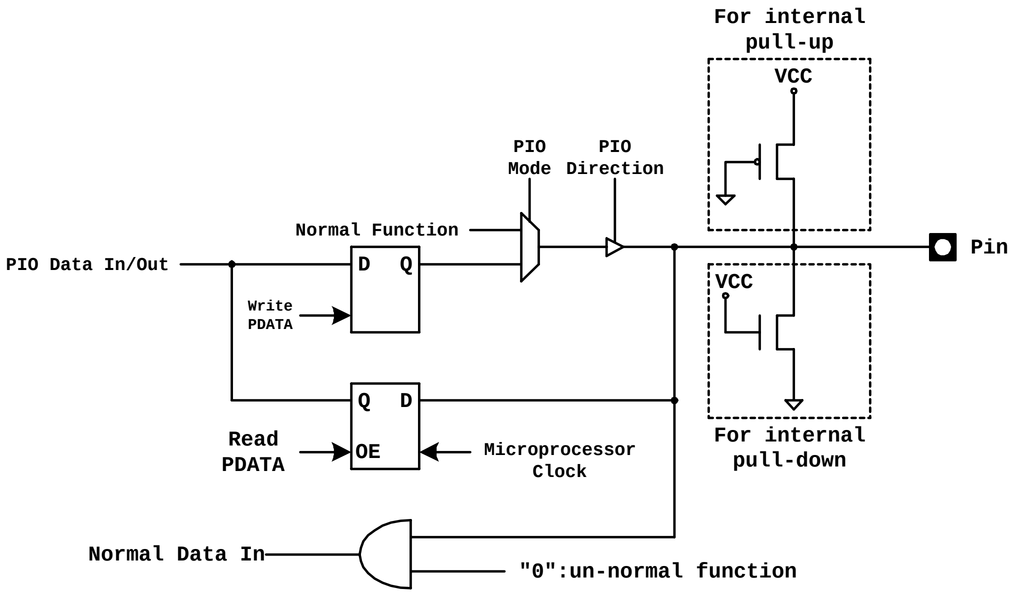
With FCR [0]=1, resetting IER [0], IER [1], IER [2], IER [3] or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR [0] will be set as long as there is one byte in the RCVR FIFO.
LSR [1] to LSR [4] will specify which error(s) has occurred.
Character error status is handled the same way as in the interrupt mode, the IIR is not affected since IER2=0.
LSR [5] will indicate when the XMIT FIFO is empty.
LSR [6] will indicate that both the XMIT FIFO and Shift Register are empty.
LSR [7] will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

17. PIO UNIT

The R2020C provides 32 programmable I/O signals, which are multi-functional pins with other signals of normal functions. Software must be used to configure these multi-functional pins as PIO or normal functions by means of programming through these registers (7Ah, 78h, 76h, 74h, 72h, and 70h).



PIO pin Operation Diagram

17.1 PIO Multi-Function Pin List Table

PIO No.	Pin No.(PQFP)	Multi Function	Reset status/PIO internal resister
0	10	TMRIN1/SA10	PIO/ Input with 75K pull-up
1	12	TMROUT1/SA8	PIO/ Input with 75K pull-down
2	156	PCS6_n	PIO/ Input with 75K pull-up
3	155	PCS5_n	PIO/ Input with 75K pull-up
4	153	DT/R_n	Normal operation/ Input with 75K pull-up
5	154	DEN_n	Normal operation/ Input with 75K pull-up
6	113	RXD0_1	PIO/ Input with 75K pull-up
7	51	A17/SAD6	Normal operation/ Input with 75K pull-up
8	49	A18/SAD7	Normal operation/ Input with 75K pull-up
9	48	A19/ALE	Normal operation/ Input with 75K pull-up
10	13	TMROUT0/SA7	PIO/ Input with 75K pull-down
11	11	TMRIN0/SA9	PIO/ Input with 75K pull-up
12	15	DRQ0/INT5/SA5	PIO/ Input with 75K pull-up
13	14	DRQ1/INT6/SA6	PIO/ Input with 75K pull-up
14	158	PCS0_n	PIO/ Input with 75K pull-up
15	157	PCS1_n	PIO/ Input with 75K pull-up
16	122	TXD0_3	PIO/ Input with 75K pull-up
17	121	TXD0_2	PIO/ Input with 75K pull-up
18	120	TXD0_1	PIO/ Input with 75K pull-up
19	119	TXD0_0	PIO/ Input with 75K pull-up

20	123	TXEN0	PIO/ Input with 75K pull-up
21	118	TXC0	Normal operation/ Input with 75K pull-up
22	117	RXC0	Normal operation/ Input with 75K pull-up
23	116	RXD0_3	PIO/ Input with 75K pull-up
24	115	RXD0_2	PIO/ Input with 75K pull-up
25	36	PCS2_n/IOR_n	PIO/ Input with 75K pull-up
26	37	PCS3_n/IOW_n	PIO/ Input with 75K pull-up
27	43	A23	PIO/ Input with 75K pull-up
28	45	A22	PIO/ Input with 75K pull-up
29	46	UARTX0	PIO/ Input with 75K pull-down
30	47	UARTX1	PIO/ Input with 75K pull-down
31	6	INT2	PIO/ Input with 75K pull-up

PIO Mode	PIO Direction	Pin Function
0	0	Normal Operation
0	1	PIO input with pull-up/pull-down
1	0	PIO output
1	1	PIO input without pull-up/pull-down

Register Offset: 7Ah
Register Name: PIO Data 1 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA[31:16]															

Bit	Name	Attribute	Description
15-0	PDATA [31:16]	R/W	PIO Data Bits. These bits PDATA[31:16] are mapped to the PIO[31:16] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 78h
Register Name: PIO Direction 1 Register
Reset Value : FF9Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR[31:16]															

Bit	Name	Attribute	Description
15-0	PDIR [31:16]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 76h
Register Name: PIO Mode 1 Register
Reset Value : 0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">PMODE[31:16]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	PMODE [31:16]	R/W	PIO Mode Bits. The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually. The definitions (PIO Mode, PIO Direction) for the functions of PIO pins: (0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down (1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

Register Offset: 74h
Register Name: PIO Data 0 Register
Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">PDATA[15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	PDATA [15:0]	R/W	PIO Data Bits. These bits PDATA[15:0] are mapped to the PIO[15:0] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 72h
Register Name: PIO Direction 0 Register
Reset Value : FC4Fh

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">PDIR[15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	PDIR [15:0]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 70h
Register Name: PIO Mode 0 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE[15:0]															

Bit	Name	Attribute	Description
15-0	PMODE [15:0]	R/W	PIO Mode Bits.

18. CACHE Controller

18.1 Cache Control Register

Register Offset: FEC0h
Register Name: Cache Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICE	DCE	Reserved		NCR3	NCR2	NCR1	NCR0	WIR	Reserved						

Bit	Name	Attribute	Description
15	ICE	R/W	Instruction Cache enable when set
14	DCE	R/W	Data Cache enable when set
13-12	Rsvd	RO	Reserved
11	NCR3	R/W	Non-Cache region3 enable when set
10	NCR2	R/W	Non-Cache region2 enable when set
9	NCR1	R/W	Non-Cache region1 enable when set
8	NCR0	R/W	Non-Cache region0 enable when set
7	WIR	R/W	Write Invalid region enable when set
6-0	Rsvd	RO	Reserved

18.2 Non-Cache Region Register

Register Offset: FEC2h
Register Name: Non-Cache Region0 Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FEC4h
Register Name: Non-Cache Region0 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FEC6h
Register Name: Non-Cache Region0 End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FEC8h
Register Name: Non-Cache Region0 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

Register Offset: FECAh
Register Name: Non-Cache Region1 Start Address Low Register
Reset Value : ----

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="13">NCRS[15:3]</td><td colspan="3">Reserved</td></tr>
</table>

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FECCh
Register Name: Non-Cache Region1 Start Address High Register
Reset Value : -----

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="8">NCRS[23:16]</td></tr>
</table>

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FECEh
Register Name: Non-Cache Region1 End Address Low Register
Reset Value : ----

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="13">NCRE[15:3]</td><td colspan="3">Reserved</td></tr>
</table>

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FED0h
Register Name: Non-Cache Region1 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

Register Offset: FED2h
Register Name: Non-Cache Region2 Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FED4h
Register Name: Non-Cache Region2 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FED6h
Register Name: Non-Cache Region2 End Address Low Register
Reset Value : ----

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="13">NCRE[15:3]</td><td colspan="3">Reserved</td></tr>
</table>

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FED8h
Register Name: Non-Cache Region2 End Address High Register
Reset Value : -----

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="8">NCRE[23:16]</td></tr>
</table>

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

Register Offset: FEDAh
Register Name: Non-Cache Region3 Start Address Low Register
Reset Value : ----

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="13">NCRS[15:3]</td><td colspan="3">Reserved</td></tr>
</table>

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FEDCh
Register Name: Non-Cache Region3 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FEDEh
Register Name: Non-Cache Region3 End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FEE0h
Register Name: Non-Cache Region3 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

18.3 Write Invalid Region Register

Register Offset: FEE2h
Register Name: Write Invalid Region Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	WIRS	R/W	Write Invalid Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Write Invalid Region start address [2:0]

Register Offset: FEE4h
Register Name: Write Invalid Region Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WIRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	WIRS	R/W	Write Invalid Region start address [23:16]

Register Offset: FEE6h
Register Name: Write Invalid Region End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	WIRE	R/W	Write Invalid Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Write Invalid Region start address [2:0]

Register Offset: FEC8h
Register Name: Write Invalid Region End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WIRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	WIRE	R/W	Write Invalid Region end address [23:16]

19. SDRAM Controller

19.1 SDRAM Mode Set Register

Register Offset: F2h
Register Name: SDRAM Mode Set Register
Reset Value : 0020h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								0	LAT[2:0]			0	BL[2:0]		

Bit	Name	Attribute	Description
15-7	Rsvd	RO	Reserved
6-4	LAT[2:0]	R/W	CAS_n Latency Select. Refer to the following list: **LAT [2:0]** **CAS_n Latency** 0 0 0 Reserved 0 0 1 Reserved 0 1 0 2 (Default) 0 1 1 3 1 0 0 Reserved 1 0 1 Reserved 1 1 0 Reserved
3	Rsvd	RO	1'b0.
2-0	BL[2:0]	RO	Burst Length.

19.2 SDRAM Control Register

Register Offset: F4h
Register Name: SDRAM Control Register
Reset Value : 0001h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											SSSEL1	SSSEL0	SREF	Rsvd	SDRAM EN

Bit	Name	Attribute	Description
15-5	Rsvd	RO	Reserved
4-3	SSSEL[1:0]	R/W	The SDRAM Size Select bit. (Default is 2'b0) **SSEL1-0 -------- SDRAM Size Select** 0 0 -------- 1Mx16 bits

			0 1 -------- 4Mx16 bits 1 0 -------- Reserved 1 1 -------- Reserved
2	SREF	R/W	Self-Refresh Enable. Set 1: Enable Self-Refreshed when SDRAM is in power mode. Set 0: Disable Self-Refreshed. (Default)
1	Rsvd	RO	Reserved
0	SDRAMEN	R/W	SDRAM Enable. Set 1: Enable SDRAM. (Default) Set 0: Disable SDRAM.

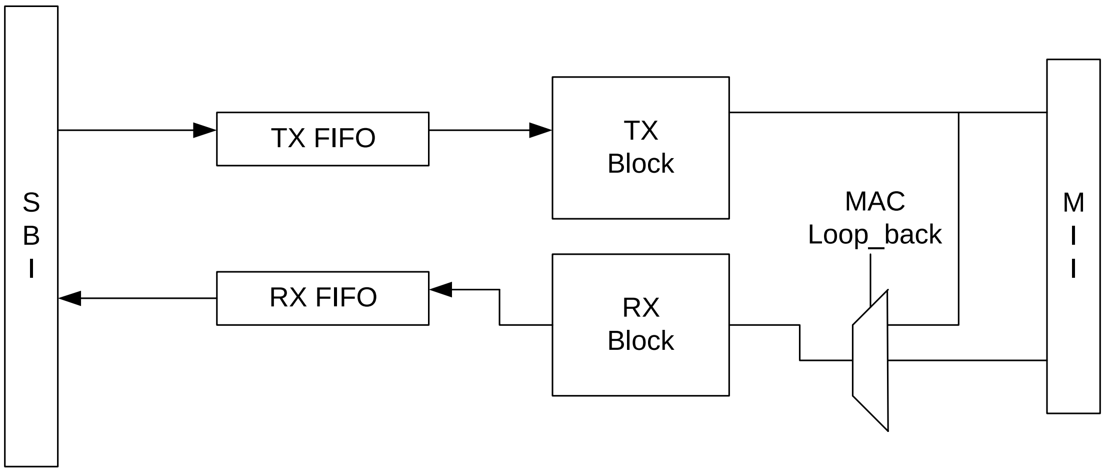
19.3 SDRAM Timing Parameter Register

Register Offset: F6h
Register Name: SDRAM Timing Parameter Register
Reset Value : F933h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SREXT[2:0]			TWR	MRC[3:0]				MPR[3:0]				RCD[3:0]			

Bit	Name	Attribute	Description
15-13	SREXT[2:0]	R/W	Self-Refresh Exit Time (t_{SREX}). The Self-Refresh Exit Time can be programmed from 0 to 15 Clocks.
12	TWR	R/W	Write Recovery Time. 1: 2 Clocks cycle. 0: 1 Clock cycle.
11-8	MRC[3:0]	R/W	Min Row Cycle Time (t_{RC},). It can be programmed from 0 to 15 Clocks.
7-4	MPR[3:0]	R/W	Min Pre-charge Time (t_{RP},). It can be programmed from 0 to 15 Clocks.
3-0	RCD[3:0]	R/W	Row to Column Delay time (t_{RCD}). It can be programmed from 0 to 15 Clocks.

20. Fast Ethernet Controller



SBI : System Bus Interface

MAC Block Diagram

20.1 RX Descriptor Format

15	3 2 1 0
DRST	
DRLEN	
DRBP	0 0
	DRBP [23:16]
DRNX	0 0
	DRNX [23:16]
	HIDX[5:0]
Reserve2	
Reserve3	

1. DRST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	RXOK	Reserved		PHY ERR	DRI BBLE	OBL	LONG	RUNT	CRC ERR	BROAD CAST	MULTI CAST	MCH	MIDH	MID	

The RX circuit will stop receiving packet if Owner Bit=0.

DRST [14:0]: RX Status. The MAC will update the RX status field after frame receiving is complete.

Bit	Name	Description
15	O	Owner Bit. Set1: MAC. Set0: CPU.

14	RXOK	RX successful. This bit indicates that the packet was received successfully without error. It includes: (1) RX_ER = 0 (MII interface). (2) Ignore DRIBBLE status. (3) No over buffer length. (4) Without CRC error. (5) Not a LONG packet. (6) Not a RUNT packet. (7) No FIFO Full.
13-12	Rsvd	Reserved.
11	PHYERR	PHY RX Error packet. Read 1 means that an error occurred in receiving packets on MII interface.
10	DRIBBLE	Dribble packet. Read 1 means the received packet is a dribble packet.
9	OBL	Over Buffer Length. Read 1 means the received packet length > buffer maximum length.
8	LONG	Long packet. Read 1 means the received packet length > maximum packet length.
7	RUNT	Runt packet. Read 1 means the received packet length < 64 Bytes.
6	CRCERR	CRC Error packet. Read 1 means receiving a packet with CRC errors.
5	BROADCAST	It indicates that the received packet is a broadcast packet.
4	MULTICAST	It indicates that the received packet is a multicast packet.
3	MCH	Multicast Hit. It indicates that the received packet hits one of the hash-table bits.
2	MIDH	MID table is hit.
1-0	MID	Index of matched MIDx. These two bits indicate that the received packet hits one of the MID groups.

2. DRLEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DRLEN										

Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DRLEN	The size of the received frame.

3. DRBP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DRBP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRBP	RX Data Buffer Pointer. This is a 24-bit address pointer and DRBP [1:0] is always 2'b00.

4. DRNX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DRNX																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRNX	RX Next Frame Descriptor Pointer. This is a 24-bit descriptor address pointer and DRNX [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

5. HIDX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										HIDX					

Bit	Name	Description
15-6	Rsvd	Reserved.
5-0	HIDX	HIDX[5:0] is a hash index. If MCR1[14] is set to 1, the hash index number will be written into RX description.

6. Reserve2

7. Reserve3

Note:

1. RX Descriptor start address and Data Buffer start address must be Double-Word alignment.
2. The RX packet will be filtered out if its length is less than 6. (Not complete DA information.)

20.2 TX Descriptor Format

15	3	2	1	0
DTST				
DTLEN				
DTBP			0	0
	DTBP [23:16]			
DTNP			0	0
	DTNP [23:16]			

1. DTST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	TXOK	DIS CRC	Reserved						TXFUR	LATEC	EXCEE DC	COLCNT			

The TX circuit will stop transmitting packet if the Owner Bit=0

DTST [14:0]: TX Status and packet control. The MAC will update the TX status field after frame transmission is completed. The control bit is for each packet usage.

Bit	Name	Description
15	O	Owner Bit. Set1: MAC. Set0: CPU.
14	TXOK	TX packet successful. This bit indicates that the packet was transmitted successfully without error. It includes: (1) No late collision. (2) No excessive collision. (3) No TX FIFO under-run. (4) No lost carrier.
13	DISCRC	Disable append CRC field. This is a control bit. =1: disable CRC append. =0: enable CRC append on TX packet. When the status is updated, this bit will keep in previous setting.
12-7	Rsvd	Reserved
6	TXFUR	FIFO Under-Run.
5	LATEC	Late Collision.
4	EXCEEDC	Exceed Collision.
3-0	COLCNT	Collision Counts.

2. DTLEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DTLEN										

Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DTLEN	The length of the transmitted packet.

3. DTBP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DTBP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTBP	TX Buffer Pointer. This is a 24-bit address pointer.

4. DTNP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DTNP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTNP	TX Next Descriptor Pointer. This is a 24-bit descriptor address pointer and DTNP [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

Note:

1. TX Descriptor start address must be Double-Word alignment.
2. TX Data Buffer start address can be any byte alignment address.
3. Driver needs to take care that the transmitted data are less than 60 bytes.

20.3 MCR0: MAC Control Register 0 (00h)

Register Offset: 00h
Register Name: MCR0: MAC Control Register 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULLD	TXEIE	Rsvd	XMTEN	Reserved		FCEN	AMCP	RXEIE	FBCP	PROM	ADRB	ALONG	ARUNT	ACRCER	RCVEN

Bit	Name	Attribute	Description
15	FULLD	R/W	Full Duplex. Set 1: Full duplex. Set 0: Half duplex. (Default)
14	TXEIE	R/W	TX Early Interrupts Enable. Set 1: MAC will generate one TX early interrupt when the data are transmitted over early interrupt threshold (see MCR1 [7:6]). Set 0: TX early interrupt will be disabled.
13	Rsvd	RO	Reserved
12	XMTEN	R/W	Transmission Enable
11-10	Rsvd	RO	Reserved
9	FCEN	R/W	Flow Control Function Enable. Set 1: will enable flow control. Set 0: will disable flow control.
8	AMCP	R/W	Accept Multicast Packet. Set 1: will enable hash table function. Set 0: will disable hash table function.
7	RXEIE	R/W	RX Early Interrupts Enable. Set to 1, MAC will generate one RX early interrupt when the data are received over early interrupt threshold (see MCR1 [7:6]). Set 0: RX early interrupt will be disabled.
6	FBCP	R/W	Filter Broadcast Packet. Set 1: to filter broadcast packet. Set 0: to accept broadcast packet.
5	PROM	R/W	Promiscuous Mode. Set 1: MAC will receive all packets without checking the MAC address. Set 0: MAC will only receive the packet that hits the MAC address.
4	ADRB	R/W	Accept DRIBBLE packet. Set 1: Enable to accept dribble packets. Set 0: Disable.
3	ALONG	R/W	Accept Long packet. Set 1: Enable to accept long packets. Set 0: Disable.
2	ARUNT	R/W	Accept RUNT packet. Set 1: Enable to accept runt packets. The packets which length > 6 and < 64 will be accepted, but the packets which length >0 and < 6 will be rejected. Set 0: Disable to accept runt packets.
1	ACRCER	R/W	Accept CRC Error packet. Set 1: Enable. Set 0: Disable.
0	RCVEN	R/W	Receive Enable. Set 1: Enable to receive packets. Set 0: Disable packet receive.

20.4 MCR1: MAC Control Register 1 (04h)

Register Offset: 04h
Register Name: MCR1: MAC Control Register 1
Reset Value : 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUCP	WIDX	Reserved				TPF	ECR	EITH [1:0]		MAXLEN [1:0]		0	0	LBM	MRST

Bit	Name	Attribute	Description
15	AUCP	R/W	Filter uni-cast packet by hash-table. Set 1: Enable. Set 0: Disable.
14	WIDX	R/W	Write the hash index number that was hit by hash-table. Set 1: Enable to write the HIDX [5:0] into Rx descriptor. Set 0: Disable this function.
13-10	Rsvd	RO	Reserved
9	TPF	RO	Trigger Pause Frame to be transmitted. If flow control (FCEN bit in MCR0 [9]) is enabled, this bit will be set automatically when received descriptor unavailable happens. TPF refers to XMTEN bit (MCR0 [12]). When XMTEN bit is set, the pause frame can be sent.
8	ECR	R/W	Excessive Collision Retransmit times. 0: 16 times. (Default) 1: 32 times.
7-6	EITH [1:0]	R/W	Early Interrupt Threshold. 00: 1129 bytes. (Default) 01: 1257 bytes. 10: 1385 bytes. 11: 1513 bytes.
5-4	MAXLEN [1:0]	R/W	Maximum Packet Length Selector. Define the length of long packets. 01: 1518 bytes. (Default) 10: 1522 bytes. 11: 1534 bytes. 00: 1537 bytes.
3-2	Rsvd	R/O	Reserved
1	LBM	R/W	Loop-Back mode. 0: Normal Mode. (Default) 1: MAC Loop-Back.
0	MRST	R/W	MAC Reset. Set 1 to reset MAC. After reset, this bit will be cleared to 0.

20.5 MBCR: MAC Bus Control Register (08h)

Register Offset: 08h
Register Name: MBCR: MAC Bus Control Register
Reset Value : 1F1Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RHPT [4:0]					Reserved		RXFTH [1:0]		TXFTH [1:0]		FIFOTL [1:0]	

PS. Update this register only when RCVEN=0

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12-8	RHPT [4:0]	R/W	SDRAM Bus Request High Priority Timer. When MAC issues a bus request to SDRAM arbiter, this timer will start to count down. After this timer is timeout, if SDRAM arbiter is still not granted to MAC, the SDRAM bus request will become high priority. Wait time = 0 ~15 host clocks. (Default=15 host clocks)
7-6	Rsvd	RO	Reserved
5-4	RXFTH [1:0]	R/W	RX FIFO Data Threshold. MAC receive machine starts to move the received data into host memory when receiving data over the RX FIFO threshold. 00: 8 bytes. 01: 16 bytes. (Default) 10: 32 bytes. 11: 64 bytes.
3-2	TXFTH [1:0]	R/W	TX FIFO Data Threshold. MAC transmit machine starts to send out packets to PHY when transmitting data into TX FIFO over the threshold. 00: 16 bytes. 01: 32 bytes. 10: 64 bytes. (Default) 11: 96 bytes.
1-0	FIFOTL [1:0]	R/W	FIFO Transfer Length. The every transfer data length between MAC FIFO and SDRAM. 00: 4 bytes. 01: 8 bytes. 10: 16 bytes. (Default) 11: 32 bytes.

20.6 MTICR: TX Interrupt Control Register (0Ch)

Register Offset: 0Ch
Register Name: MTICR: TX Interrupt Control Register
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">Reserved</td><td colspan="4">TXINTC [3:0]</td><td colspan="2">Reserved</td><td colspan="6">TXTIMER [5:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	TXINTC [3:0]	R/W	TX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after sending N packets (1~15 packets).
7-6	Rsvd	RO	Reserved
5-0	TXTIMER [5:0]	R/W	Wait TX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: (63 + TXTIMER * 64) TX clock

20.7 MRICR: RX Interrupt Control Register (10h)

Register Offset: 10h
Register Name: MRICR: RX Interrupt Control Register
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">Reserved</td><td colspan="4">RXINTC [3:0]</td><td colspan="2">Reserved</td><td colspan="6">RXTIMER [5:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	RXINTC [3:0]	R/W	RX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after N packets (1~15 packets) are received.
7-6	Rsvd	RO	Reserved
5-0	RXTIMER [5:0]	R/W	Wait RX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: (63 + RXTIMER * 64) RX clock

20.8 MTPR: TX Poll Command Register (14h)

Register Offset: 14h
Register Name: MTPR: TX Poll Command Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TM2TX

Bit	Name	Attribute	Description
15-1	Rsvd	RO	Reserved
0	TM2TX	R/W	Trigger MAC to Transmit. When Write: Trigger MAC to check TX description owner bit. If owner bit=0, MAC will standby until the owner bit=1 to start transmission. When Read: TM2TX is current transmission status. When TM2TX= 1, it means MAC is in transmitting. When TM2TX= 0, it means transmission was completed.

20.9 MRBSR: RX Buffer Size Register (18h)

Register Offset: 18h
Register Name: MRBSR: RX Buffer Size Register
Reset Value : 0600h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RBSZ [10:0]									RBSZ[1:0]	

PS. Update this register only when RCVEN=0

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10-2	RBSZ [10:2]	R/W	RX Buffer Size Bit10~Bit2 for all RX frame data buffer of Descriptors.
1-0	RBSZ [1:0]	R/W	RX Buffer Size Bit1:0 must be 00.

20.10 MRDCR: RX Descriptor Control Register (1Ah)

Register Offset: 1Ah
Register Name: MRDCR: RX Descriptor Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXPT [7:0]								RXDESPAN [7:0]							

Bit	Name	Attribute	Description
15-8	RXPT [7:0]	R/W	RX Descriptor Threshold value. MAC controller will send TX Pause Frame when available RX Descriptor reaches this threshold value.
7-0	RXDESPAN [7:0]	R/W	RX Descriptor Available Number for flow-control. When MAC finishes one descriptor data transfer into RX buffer, the RX descriptor available number will decrease 1 automatically. Use "IN" instruction to read this register and "OUT" instruction to increase the register value. When RCVEN=0, use "OUT" instruction to setup RX descriptor available number. When RCVEN=1, use "OUT" instruction to increase RX descriptor available number. This register must be initialized before RCVEN = 1.

20.11 MLSR: MAC Last Status Register(1Ch)

Register Offset: 1Ch
Register Name: MLSR: MAC Last Status Register
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFOR	LATEC	EXCEEDC	Rsvd	PHYSTS	RXDESPUA	TXFUR	Rsvd	PHYEER	DRIBBLE	OBL	LONG	RUNT	CRCERR	BROADCAST	MULTICAST

PS. The MAC last time status. It is updated by next packet coming.

Bit	Name	Attribute	Description
15	RXFOR	RO	RX FIFO Over-Run
14	LATEC	RO	Transmit Late Collision.
13	EXCEEDC	RO	Transmit Exceed Collision.
12	Rsvd	RO	Reserved
11	PHYSTS	RO	The value is the status of input pin PHY_CHG.

10	RXDESPUA	RO	RX Descriptor Unavailable.
9	TXFUR	RO	TX FIFO Under-Run.
8	Rsvd	RO	Reserved
7	PHYERR	RO	PHY RX Error.
6	DRIBBLE	RO	Dribble Packet.
5	OBL	RO	Received Packet Length Over Buffer Length.
4	LONG	RO	Received Packets Too Long.
3	RUNT	RO	Received Packets Too Short.
2	CRCERR	RO	Received Packets CRC Error.
1	BROADCAST	RO	Received Broadcast Packets.
0	MULTICAST	RO	Received Multicast Packets.

20.12 MMDIO: MDIO Control Register (20h)

Register Offset: 20h
Register Name: MMDIO: MDIO Control Register
Reset Value : ——

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Rsvd</td><td>MIIWR</td><td>MIIRD</td><td colspan="5">PHYAD [4:0]</td><td colspan="3">Reserved</td><td colspan="5">REGAD [4:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14	MIIWR	R/W	MDIO Write. Set 1 to write MIIWDATA [15:0] to MDIO. It will be cleared after the operation is completed.
13	MIIRD	R/W	MDIO Read. Set 1 to read data from MDIO into MIIRDATA [15:0]. It will be cleared after the operation is completed.
12-8	PHYAD [4:0]	R/W	PHY address.
7-5	Rsvd	RO	Reserved
4-0	REGAD [4:0]	R/W	REG address.

20.13 MMRD: MDIO Read Data Register (24h)

Register Offset:	24h
Register Name:	MMRD: MDIO Read Data Register
Reset Value :	0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">MIIRDATA [15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	MIIRDATA [15:0]	RO	MII Read Data. The data, read from MDIO, are put in this register.

20.14 MMWD: MDIO Write Data Register (28h)

Register Offset:	28h
Register Name:	MMRD: MDIO Write Data Register
Reset Value :	0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">MIIWDATA [15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	MIIWDATA [15:0]	R/W	MII Write Data. The data, intended for being written to MDIO, are put in this register.

20.15 MTDSA0: TX Descriptor Start Address 0 (2Ch)

Register Offset: 2Ch
Register Name: MTDSA0: TX Descriptor Start Address 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDSA [15:1]															0

PS. Initial this register only when XMTEN=0

Bit	Name	Attribute	Description
15-1	TDSA [15:1]	R/W	TX Descriptor Start Address Bit 15 - Bit 1 that are currently being sent.
0	0	RO	This bit must be 0.

Note: The first TX descriptor start address TDSA [23:0] = {MTDSA1 [7:0], MTDSA0 [15:0]} must be Double-Word alignment. MAC will update the TX descriptor start address when the previous TX has been finished.

20.16 MTDSA1: TX Descriptor Start Address 1 (30h)

Register Offset: 30h
Register Name: MTDSA1: TX Descriptor Start Address 1
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TDSA [23:16]							

PS. **Initial this register only when XMTEN=0**

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	TDSA [23:16]	RW	TX Descriptor Start Address Bit 23-16 that are currently being sent.

20.17 MRDSA0: RX Descriptor Start Address 0 (34h)

Register Offset: 34h
Register Name: MRDSA0: RX Descriptor Start Address 0
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDSA [15:1]															0

PS. **Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-1	RDSA [15:1]	R/W	RX Descriptor Start Address Bit 15-1.
0	0	RO	This bit must be 0.

Note: The first RX descriptor start address RDSA [23:0] = {MRDSA1 [7:0], MRDSA0 [15:0]} must be Double-Word alignment. MAC will update the RX descriptor start address after the previous RX has been finished.

20.18 MRDSA1: RX Descriptor Start Address 1 (38h)

Register Offset: 38h
Register Name: MRDSA1: RX Descriptor Start Address 1
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RDSA [23:16]							

PS. **Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	RDSA [23:16]	RW	The first RX Descriptor Start Address Bit 23-16.

20.19 MISR: INT Status Register (3Ch)

Register Offset: 3Ch
Register Name: MISR: INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PCHG	ECNTO	TXEI	Reserved		TXEND	RXEI	RXFF	RXDUA	RXEND

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	PCHG	RC	PHY Media Changed Interrupt status.
8	ECNTO	RC	Event Counter Overflow Interrupt status.
7	TXEI	RC	TX Early Interrupt status.
6-5	Rsvd	RO	Reserved.
4	TXEND	RC	This bit indicates Transmit Packet Finish Interrupt status.
3	RXEI	RC	RX Early Interrupt status.
2	RXFF	RC	RX FIFO Full Interrupt status.
1	RXDUA	RC	This bit indicates RX Descriptor Unavailable Interrupt status.
0	RXEND	RC	This bit indicates Receive Packet Finish Interrupt status.

Note: RC = Read Clear

20.20 MIER: INT Enable Register (40h)

Register Offset: 40h
Register Name: MIER: INT Enable Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCHGE	ECNTOE	TXEIEN	Reserved		TXENDE	RXEIE	RXFFE	RXDNAE	RXENDE

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	MCHGE	RW	PHY Link Changed Interrupt Enable Set 1: Enable MAC to generate interrupts to CPU.
8	ECNTOE	R/W	Event Counter Overflow Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
7	TXEIEN	R/W	TX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

6-5	Rsvd	RO	Reserved.
4	TXENDE	R/W	Transmit Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
3	RXEIE	R/W	RX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
2	RXFFE	R/W	RX FIFO Full Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
1	RXDNAE	R/W	RX Descriptor Unavailable Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
0	RXENDE	R/W	Receive Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

20.21 MECISR: Event Counter INT Status Register(44h)

Register Offset: 44h
Register Name: MECISR: Event Counter INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCI	LCCI	STPCI	RFFCI	RDUCI	Rsvd	LONGCI	RUNTCI	CRCECI	BCCI	MCCI	SRPCI

The correspond bit in Event Counter INT status register will be set when the MSB bit in related Event Counter register is set to 1. Reading the Event Counter register will clear the corresponding bits. Those event counters will keep increasing until reaching 255 or 65535.

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCI	RO	TX FIFO under-run Dropped Packet Counter Interrupt status.
10	LCCI	RO	TX Late Collision Counter Interrupt status.
9	STPCI	RO	TX Successfully package counter Interrupt status.
8	RFFCI	RO	RX FIFO Full Counter Interrupt status.
7	RDUCI	RO	RX Descriptor Unavailable Dropped Packet Counter Interrupt status.
6	Rsvd	RO	Reserved.
5	LONGCI	RO	RX Long Packet Counter Interrupt status.
4	RUNTCI	RO	RX Runt Packet Counter Interrupt status.
3	CRCECI	RO	RX CRC Error Packet Counter Interrupt status.
2	BCCI	RO	RX Broadcast Packet Counter Interrupt status.
1	MCCI	RO	RX Multicast Packet Counter Interrupt status.
0	SRPCI	RO	RX Successfully Packet Counter Interrupt status.

20.22 MECIER: Event Counter INT Enable Register (48h)

Register Offset: 48h
Register Name: MECIER: Event Counter INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCIE	LCCIE	STPCIE	RFFCIE	RDUCIE	Rsvd	LONGCIE	RUNTCIE	CRCECIE	BCCIE	MCCIE	SRPCIE

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCIE	RW	TX FIFO under-run Dropped Packet Counter Interrupt Enable
10	LCCIE	R/W	TX Late Collision Counter Interrupt Enable.
9	STPCIE	R/W	TX Successfully Packet Counter Interrupt Enable.
8	RFFCIE	R/W	RX FIFO Full Counter Interrupt Enable.
7	RDUCIE	R/W	RX Descriptor Unavailable Dropped Packet Counter Interrupt Enable.
6	Rsvd	RO	Reserved.
5	LONGCIE	R/W	RX Long Packet Counter Interrupt Enable.
4	RUNTCIE	R/W	RX Runt Packet Counter Interrupt Enable.
3	CRCECIE	R/W	RX CRC Error Packet Counter Interrupt Enable.
2	BCCIE	R/W	RX Broadcast Packet Counter Interrupt Enable.
1	MCCIE	R/W	RX Multicast Packet Counter Interrupt Enable.
0	SRPCIE	R/W	RX Successfully Packet Counter Interrupt Enable.

Note: Reading any one of all the following event counter registers will clear its value to 0.

20.23 MRCNT: Successfully Received Packet Counter (50h)

Register Offset: 50h
Register Name: MRCNT: Successfully Received Packet Counter
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRPCNT [15:0]															

Bit	Name	Attribute	Description
15-0	SRPCNT [15:0]	RC	Successfully Received Packet Counter

Note: RC = Read Clear

20.24 MECNT0: Event Counter 0 (52H)

Register Offset: 52h
Register Name: MECNT0: Event Counter 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCCNT [7:0]								MCCNT [7:0]							

Bit	Name	Attribute	Description
15-8	BCCNT [7:0]	RC	Receive Broadcast Packet Counter.
7-0	MCCNT [7:0]	RC	Receive Multicast Packet Counter.

Note: RC = Read Clear

20.25 MECNT1: Event Counter 1 (54h)

Register Offset: 54h
Register Name: MECNT1: Event Counter 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUNCNT [7:0]								CRCECNT [7:0]							

Bit	Name	Attribute	Description
15-8	RUNCNT [7:0]	RC	Receive Run Packet Counter.
7-0	CRCECNT [7:0]	RC	Receive CRC Error Packet Counter.

Note: RC = Read Clear

20.26 MECNT2: Event Counter 2 (56h)

Register Offset: 56h
Register Name: MECNT2: Event Counter 2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								LONGCNT [7:0]							

Bit	Name	Attribute	Description
15-8	Rsvd	RC	Reserved
7-0	LONGCNT [7:0]	RC	Receive Long Packet Counter.

Note: RC = Read Clear

20.27 MCENT3: Event Counter 3 (58h)

Register Offset: 58h
Register Name: MECNT3: Event Counter 3
Reset Value : 0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RFFCNT [7:0]</td><td colspan="8">RDUVCNT [7:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-8	RFFCNT [7:0]	RC	RX FIFO Full Packet Counter.
7-0	RDUVCNT [7:0]	RC	RX Descriptor Unavailable Packet lost Counter.

Note: RC = Read Clear

20.28 MTCNT: Successfully Transmit Packet Counter (5Ah)

Register Offset: 5Ah
Register Name: MTCNT: Successfully Transmit Packet Counter
Reset Value : 0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">STPCNT [15:0]</td></tr>
</table>

Bit	Name	Attribute	Description
15-0	STPCNT [15:0]	RC	Successfully Transmitted Packet Counter.

Note: RC = Read Clear

20.29 MCENT4: Event Counter 4 (5Ch)

Register Offset: 5Ch
Register Name: MECNT4: Event Counter 4
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDPCNT [7:0]								LCCNT [7:0]							

Bit	Name	Attribute	Description
15-8	TDPCNT [7:0]	RC	TX Dropped Packet Counter by TX FIFO under-run.
7-0	LCCNT [7:0]	RC	TX Late Collision Packet Counter.

Note: RC = Read Clear

20.30 MPCNT: Pause Frame Counter (5Eh)

Register Offset: 5Eh
Register Name: MPCNT: Pause Frame Counter
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXPFCNT [7:0]								RXPFCNT [7:0]							

Bit	Name	Attribute	Description
15-8	TXPFCNT [7:0]	RC	Transmitted Pause Frame Counter.
7-0	RXPFCNT [7:0]	RC	Received Pause Frame Counter.

Note: RC = Read Only

20.31 MAR0 ~3: Hash Table Word 0 ~3 (60h, 62h, 64h, 66h)

Register Offset: 60h
Register Name: MAR0: Hash Table Word 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR0 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR0 [15:0]	R/W	Hash Table Word 0.

Register Offset: 62h
Register Name: MAR1: Hash Table Word 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR1 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR1 [15:0]	R/W	Hash Table Word 1.

Register Offset: 64h
Register Name: MAR2: Hash Table Word 2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR2 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR2 [15:0]	R/W	Hash Table Word 2.

Register Offset: 66h
Register Name: MAR3: Hash Table Word 3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR3 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR3 [15:0]	R/W	Hash Table Word 3.

20.32 MID0 (68h, 6Ah, 6Ch)

Register Offset: 68h
Register Name: MID0
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID0L [15:0]</td></tr>
</table>

Register Offset: 6Ah
Register Name: MID0
Reset Value : ——

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID0M [15:0]</td></tr>
</table>

Register Offset: 6Ch
Register Name: MID0
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID0H [15:0]</td></tr>
</table>

The MAC/Multicast address MID0 [47:0] = {MID0H [15:0], MID0M [15:0], MID0L [15:0]};

For example: MAC address is 01:02:03:04:05:06, the contents for MID are:

MID0L [15:0] = 0201h

MID0M [15:0] = 0403h

MID0H [15:0] = 0605h

Bit 15-0: MID0L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID0M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID0H [15:0], the two bytes in the last line of the MAC/Multicast address.

20.33 MID1 (70h, 72h, 74h)

Register Offset: 70h
Register Name: MID1
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID1L [15:0]</td></tr>
</table>

Register Offset: 72h
Register Name: MID1
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID1M [15:0]</td></tr>
</table>

Register Offset: 74h
Register Name: MID1
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID1H [15:0]</td></tr>
</table>

The MAC/Multicast address MID1 [47:0] = {MID1H [15:0], MID1M [15:0], MID1L [15:0]};

Bit 15-0: MID1L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID1M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID1H [15:0], the two bytes in the last line of the MAC/Multicast address.

20.34 MID2 (78h, 7Ah, 7Ch)

Register Offset: 78h
Register Name: MID2
Reset Value : 0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">MID2L [15:0]</td></tr>
</table>

Register Offset: 7Ah
Register Name: MID2
Reset Value : 0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">MID2M [15:0]</td></tr>
</table>

Register Offset: 7Ch
Register Name: MID2
Reset Value : 0000h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">MID2H [15:0]</td></tr>
</table>

The MAC/Multicast address MID2 [47:0] = {MID2H [15:0], MID2M [15:0], MID2L [15:0]};

Bit 15-0: MID2L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID2M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID2H [15:0], the two bytes in the last line of the MAC/Multicast address.

20.35 MID3 (80h, 82h, 84h)

Register Offset: 80h
Register Name: MID3
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID3L [15:0]</td></tr>
</table>

Register Offset: 82h
Register Name: MID3
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID3M [15:0]</td></tr>
</table>

Register Offset: 84h
Register Name: MID3
Reset Value : 0000h

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">MID3H [15:0]</td></tr>
</table>

The MAC/Multicast address MID3 [47:0] = {MID3H [15:0], MID3M [15:0], MID3L [15:0]};

Bit 15-0: MID3L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID3M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID3H [15:0], the two bytes in the last line of the MAC/Multicast address.

21. DC Electrical Characteristics

21.1 Absolute Maximum Ratings (25℃)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VDDC	Core Supply Voltage	2.25	2.75	V	
VDDP1/VDDP2	PLL/DLL Supply Voltage	2.25	2.75	V	
VDDIO	I/O Supply Voltage	3.0	3.6	V	
Vil	Input Low Voltage	---	0.8	V	
Vih	Input High Voltage	2.0	---	V	
Vol	Output Low Voltage	---	0.4	V	
Voh	Output High Voltage	2.4	---	V	
Iin	Input leakage current	-10	10	uA	Vi = VDDO or 0
Ioz	Tri-State output leakage current	-10	10	uA	

Note: * Eq. C = (256/VCC) x Vout x (VCC - Vout)

** Eq. D = (98.0/VCC) x (Vout - VCC) x (Vout + 0.4VCC)

21.2 Operating Temperature

Symbol	Parameter	Typ.	Unit	Conditions
Tc	Case Temperature	55~65	℃	1. Ambient Temperature = 25℃ 2. Open case testing.

22. AC Electrical Characteristics

22.1 Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description	Parameter Symbol	No.	Description
tAVCH	14	SAD Address Valid to Clock High	tCLRH	27	RD_n Inactive Delay
tAVLL	12	SAD Address Valid to ALE Low	tCLRL	25	RD_n Active Delay
tAVRL	66	SAD Address Valid to RD_n Low	tCVCTX	20	Control Active Delay 1
tAVWL	65	SAD Address Valid to WR_n Low	tCVDEX	31	Control Inactive Delay
tAZRL	24	SAD Address Float to RD_n Active	tCXCSX	21	DEN_n Inactive Delay
tCHCSV	67	SD_CLK High to LCS_n/UCS_n Valid	tDVCL	17	MCS_n/PCS_n Hold from Command Inactive
tCHCSX	18	MCS_n/PCS_n Inactive Delay	tDXDL	1	Data in Setup
tCHCTV	22	Control Active Delay 2	tLHLL	10	ALE Width
tCHLH	9	ALE Active Delay	tLLAX	13	SAD Address Hold from ALE Inactive
tCHLL	11	ALE Inactive Delay	tRESIN	57	RST_n Setup Time
tCLAX	6	Address Hold	tRHAV	29	RD_n Inactive to SAD Address Active
tCLAZ	15	SAD Address Float Delay	tRHDX	59	RD_n High to Data Hold on SAD Bus
tCLCSV	16	MCS/PCS Active Delay	tRHLH	28	RD_n Inactive to ALE High
tCLDV	7	Data Valid Delay	tRLRH	26	RD_n Pulse Width
tCLDX	2	Data in Hold	tWLWH	32	WR_n Pulse Width

22.2 Numerical Key to Switching Parameter Symbols

No.	Parameter Symbol	Description	No.	Parameter Symbol	Description
1	tDVCL	Data in Setup	21	tCVDEX	DEN_n Inactive Delay
2	tCLDX	Data in Hold	22	tCHCTV	Control Active Delay 2
6	tCLAX	Address Hold	24	tAZRL	SAD Address Float to RD_n Active
7	tCLDV	Data Valid Delay	25	tCLRL	RD_n Active Delay
9	tCHLH	ALE Active Delay	26	tRLRH	RD_n Pulse Width
10	tLHLL	ALE Width	27	tCLRH	RD_n Inactive Delay
11	tCHLL	ALE Inactive Delay	28	tRHLH	RD_n Inactive to ALE High
12	tAVLL	SAD Address Valid to ALE Low	29	tRHAV	RD_n Inactive to SAD Address Active
13	tLLAX	SAD Address Hold from ALE Inactive	31	tCVCTX	Control Inactive Delay
14	tAVCH	SAD Address Valid to Clock High	32	tWLWH	WR_n Pulse Width
15	tCLAZ	SAD Address Float Delay	57	tRESIN	RST_n Setup Time
16	tCLCSV	MCS/PCS Active Delay	59	tRHDX	RD_n High to Data Hold on SAD Bus
17	tCXCSX	MCS_n/PCS_n Hold from Command Inactive	65	tAVWL	SAD Address Valid to WR_n Low
18	tCHCSX	MCS_n/PCS_n Inactive Delay	66	tAVRL	SAD Address Valid to RD_n Low
20	tCVCTV	Control Active Delay 1	67	tCHCSV	SD_CLK High to LCS_n/UCS_n Valid

22.3 CPU Bus

- **Read Cycle (100 MHz)**

Parameter			Preliminary 100 MHz		Unit
No.	**Symbol**	**Description**	**Min.**	**Max.**	
General Timing Requirements					
1	tDVCL	Data in Setup	**2**	**---**	ns
2	tCLDX	Data in Hold(c)	**0.4**	**---**	ns
General Timing Responses					
6	tCLAX	Address Hold	**3**	**---**	ns
9	tCHLH	ALE Active Delay	**3**	**---**	ns
10	tLHLL	ALE Width	**1T**	**1.5T**	ns
11	tCHLL	ALE Inactive Delay	**---**	**2.7**	ns
12	tAVLL	SAD Address Valid to ALE Low(a)	**4.4 (T1+no wait)**	**9.2 (T1+wait)**	ns
13	tLLAX	SAD Address Hold from ALE Inactive(a)	**0.8**	**0.8+T1 wait**	ns
14	tAVCH	SAD Address Valid to Clock High	**---**	**1.2**	ns
15	tCLAZ	SAD Address Float Delay	**---**	**3.5**	ns
16	tCLCSV	MCS_n/PCS_n Active Delay	**8**	**---**	ns
17	tCXCSX	MCS_n/PCS_n Hold from Command Inactive(a)	**7**	**---**	ns
18	tCHCSX	MCS_n/PCS_n Inactive Delay	**5**	**---**	ns
20	tCVCTV	Control Active Delay 1(b)	**---**	**8.5**	ns
21	tCVDEX	DEN_n inactive Delay	**8.0**	**---**	ns
22	tCHCTV	Control Active Delay 2(b)	**---**	**3**	ns
Read Cycle Timing Responses					
24	tAZRL	SAD Address Float to RD_n Active	**---**	**0**	ns
25	tCLRL	RD_n Active Delay	**3**	**---**	ns
26	tRLRH	RD_n Pulse Width	**2T (0 wait)**	**2T+T3 wait**	ns
27	tCLRH	RD_n Inactive Delay	**2.8**	**---**	ns
28	tRHLH	RD_n Inactive to ALE High(a)	**4.5**	**---**	ns
29	tRHAV	RD_n Inactive to SAD Address Active(a)	**6**	**---**	ns
59	tRHDX	RD_n High to Data Hold on SAD Bus(c)	**0**	**---**	ns
66	tAVRL	SAD Address Valid to RD_n Low(a)	**---**	**14**	ns
67	tCHCSV	SD_CLK High to UCS_n Valid	**---**	**6**	ns

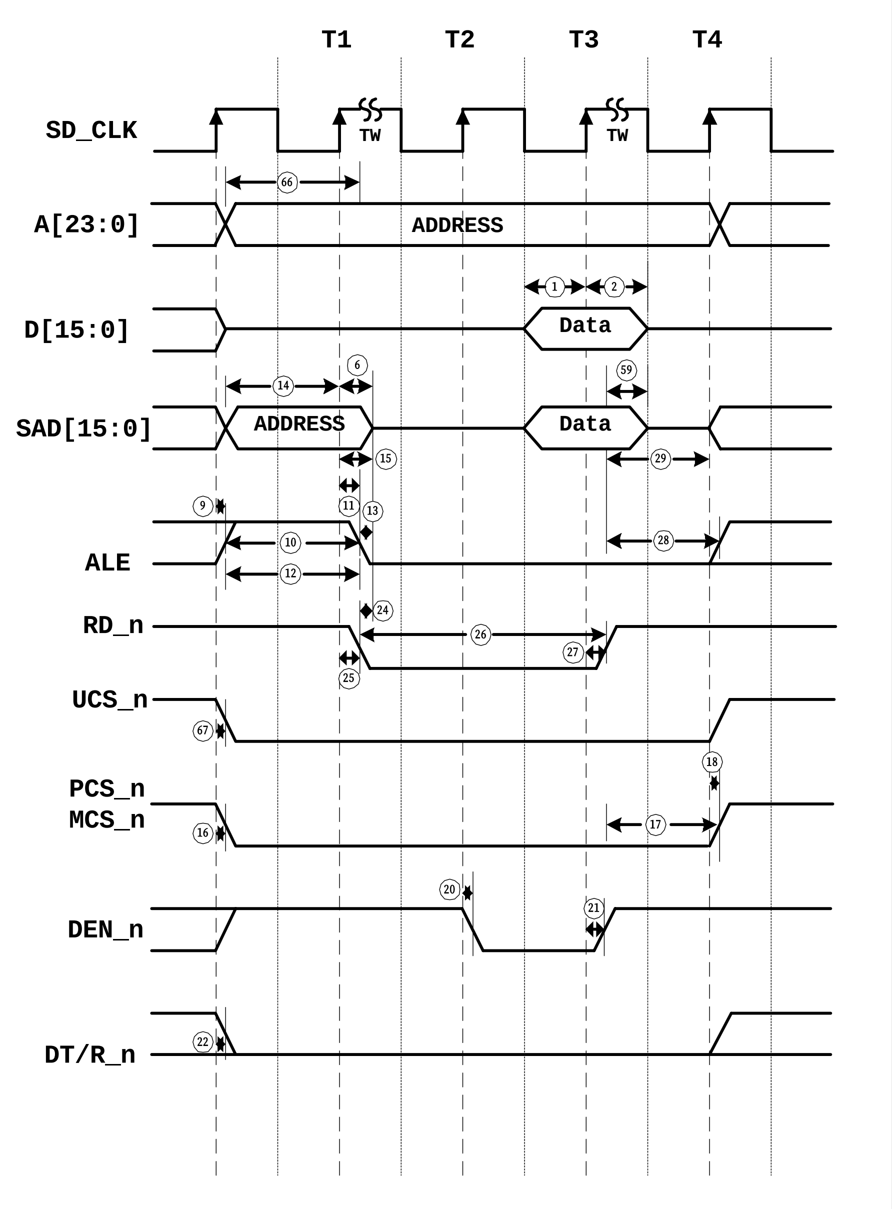
Notes: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a. Equal loading on referenced pins. T1 wait states should be inserted to increase hold time.

b. This parameter applies to the DEN_n, WR_n, WHB_n, and WLB_n signals.

c. If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

- **Read Cycle Waveforms**



READ CYCLE

Write Cycle (100 MHz)

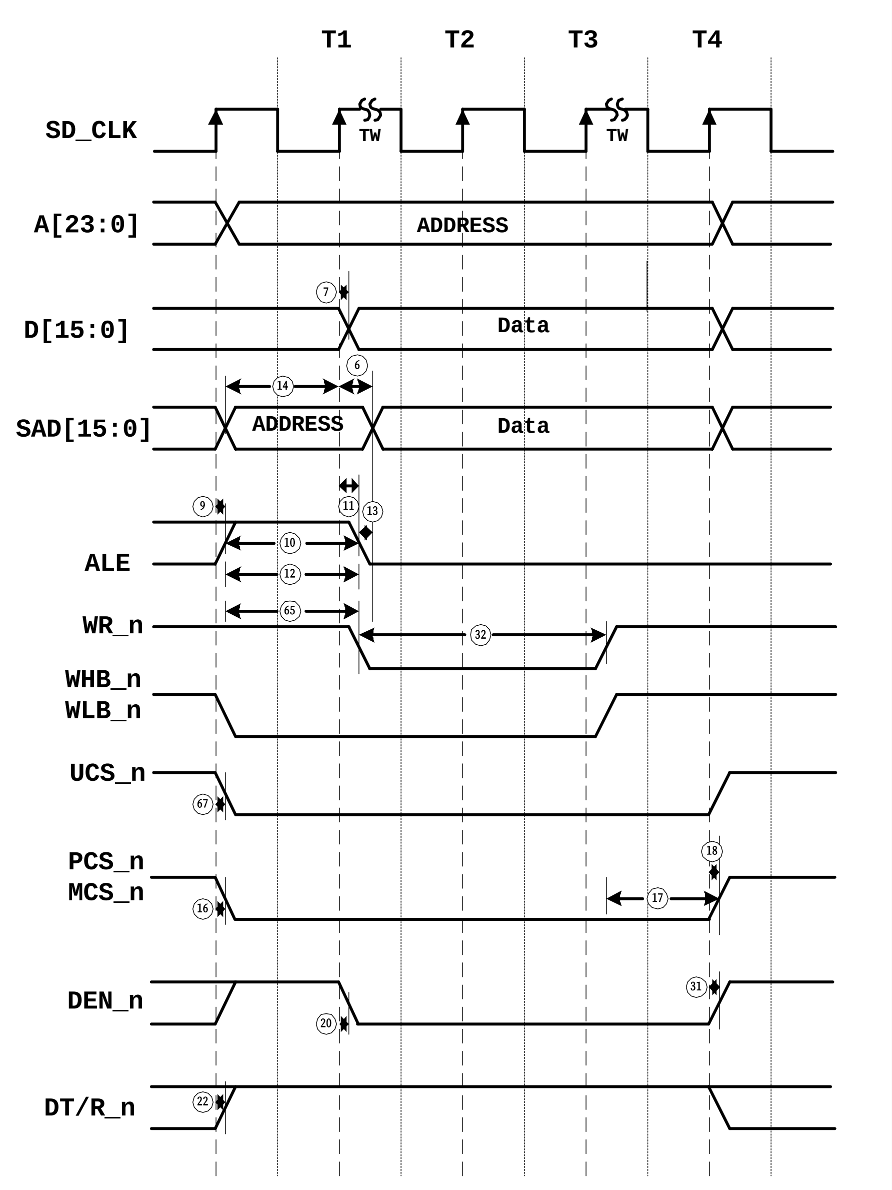
Parameter			Preliminary		Unit
			100 MHz		
No.	**Symbol**	**Description**	**Min.**	**Max.**	
General Timing Responses					
6	t_{CLAX}	Address Hold	**3**	**---**	ns
7	t_{CLDV}	Data Valid Delay	**2.5**	**---**	ns
9	t_{CHLH}	ALE Active Delay	**3**	**---**	ns
10	t_{LHLL}	ALE Width	**1T**	**1.5T**	ns
11	t_{CHLL}	ALE Inactive Delay	**---**	**2.7**	ns
12	t_{AVLL}	SAD Address Valid to ALE Low(a)	**4.4 (T1 no wait)**	**9.2 (T1 wait)**	ns
13	t_{LLAX}	SAD Address Hold from ALE Inactive(a)	**0.8 (T1 no wait)**	**5.6 (T1 wait)**	ns
14	t_{AVCH}	SAD Address Valid to Clock High	**---**	**1.2**	ns
16	t_{CLCSV}	MCS_n/PCS_n Active Delay	**8**	**---**	ns
17	t_{CXCSX}	MCS_n/PCS_n Hold from Command Inactive(a)	**7**	**---**	ns
18	t_{CHCSX}	MCS_n/PCS_n Inactive Delay	**5**	**---**	ns
20	t_{CVCTV}	Control Active Delay 1(b)	**---**	**8.5**	ns
22	t_{CHCTV}	Control Active Delay 2(b)	**---**	**3**	ns
Write Cycle Timing Responses					
31	t_{CVCTX}	Control Inactive Delay(b)	**0.3**	**---**	ns
32	t_{WLWH}	WR_n Pulse Width	**2T**	**2T+wait**	ns
65	t_{AVWL}	SAD Address Valid to WR_n Low	**---**	**---**	ns
67	t_{CHCSV}	SD_CLK High to UCS_n Valid	**---**	**6**	ns

Notes: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a. Equal loading on referenced pins. T1 wait states should be inserted to increase hold time.

b. This parameter applies to the DEN_n, WR_n, WHB_n, and WLB_n signals.

- **Write Cycle Waveforms**



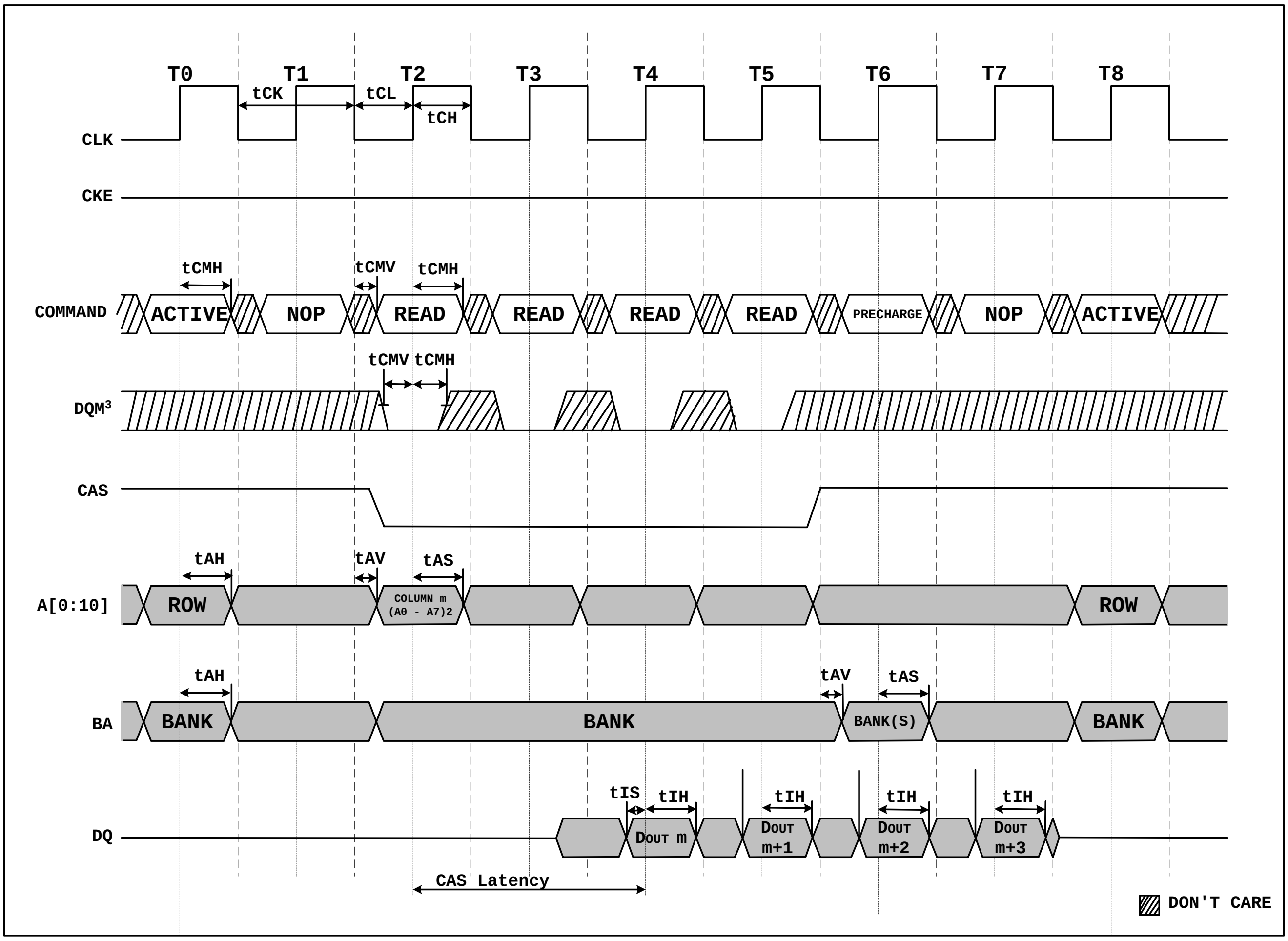
WRITE CYCLE

22.4 SDRAM Bus

- **SDRAM Read Cycle (100 MHz)**

Symbol	Description	Min.	Type	Max.
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
tCMV	Command Valid Delay time	---	---	6
tcmh	Command Hold time	4	---	---
tAv	Address Valid Delay time	---	---	5
tAH	Address Setup Hold time	4	---	---
tIS	Data Input Setup time	2	---	---
tIH	Data Input Hold time	1	---	---

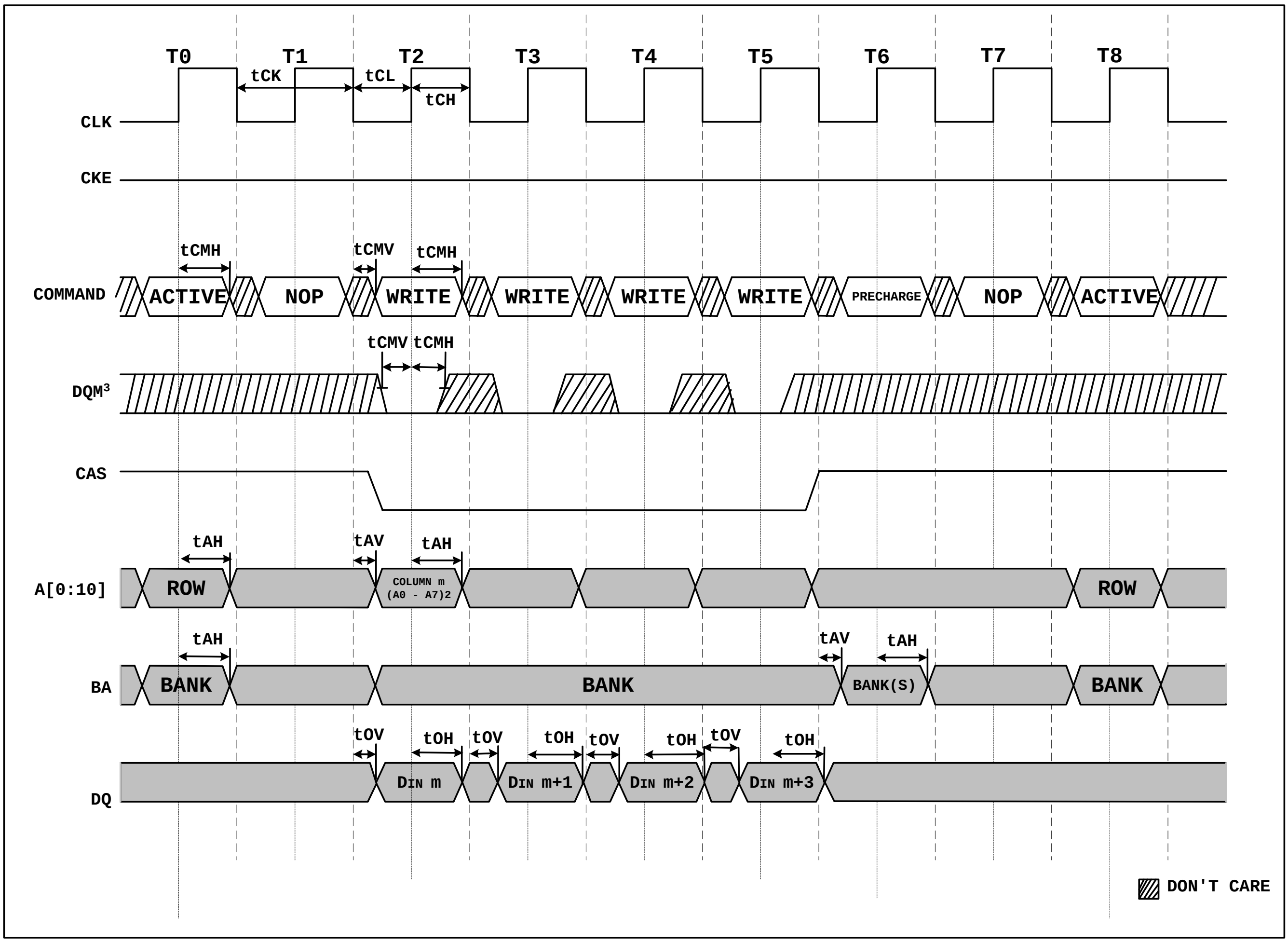
- **SDRAM Read Cycle Waveforms**



SDRAM Write Cycle (100 MHz)

Symbol	Description	Min.	Type	Max.
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
tCMV	Command Valid Delay time	---	---	6
tCMH	Command Hold time	4	---	---
tAV	Address Valid Delay time	---	---	5
tAH	Address Setup Hold time	---	---	5
tOV	Data Output Valid Delay time	---	---	8
tOH	Data Output Hold time	0	---	---

SDRAM Write Cycle Waveforms



22.5 CPU Reset

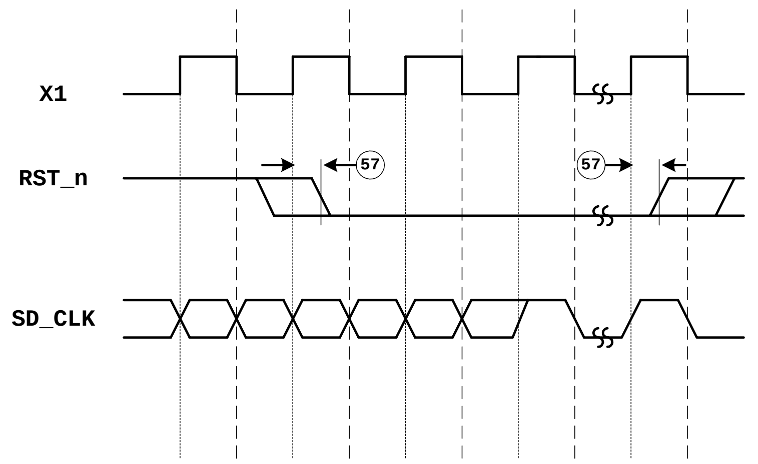
- **Reset and Bus Hold (100 MHz)**

Parameter			Preliminary		Unit
			100 MHz		
No.	**Symbol**	**Description**	**Min.**	**Max.**	
Reset and Bus Hold Timing Requirements					
15	t_{CLAZ}	SAD Address Float Delay	**---**	**3.5**	ns
57	t_{RESIN}	RST_n Setup Time	**2**	**---**	ns
58	t_{HVCL}	HOLD Setup(a)	**2.5**	**---**	ns

Note: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a. This timing must be met to guarantee recognition at the next clock.

- **Reset Waveforms**

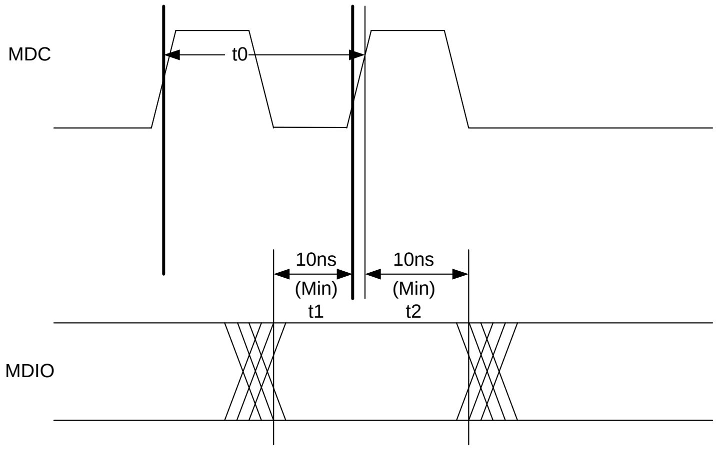


Reset Waveforms

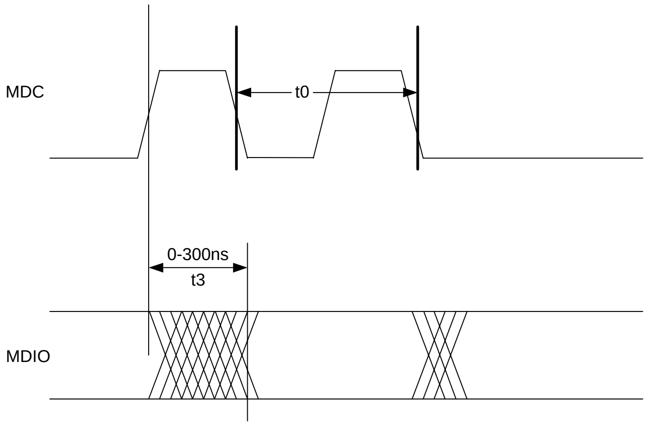
22.6 MDC/MDIO Timing

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
t0	MDC Cycle Time		TXC/10			
t1	MDIO Setup before MDC		MDC/2-10			
t2	MDIO Hold after MDC		MDC/2+10			
t3	MDC to MDIO Output Delay		10			

MDIO Timing When OUTPUT by R2020C



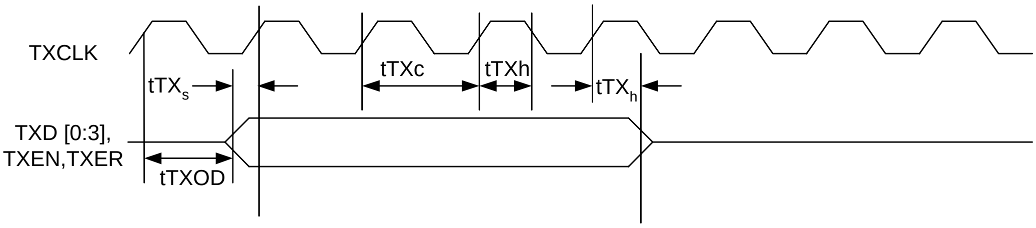
MIDO Timing When OUTPUT by PHY



22.7 TX Transmit Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tTXh, tTXl	TXCLK High/Low Time					
tTXs	TXD{0:3}, TXEN, and TXER Setup to TXCLK High	1T-6				
tTXh	TXD{0:3}, TXEN, and TXER Hold from TXCLK High			4		
tTXOD	TXCLK to Output Delay			6		
Typical Values are at 25℃ and for design aid only; not guaranteed and not subject to production testing.						

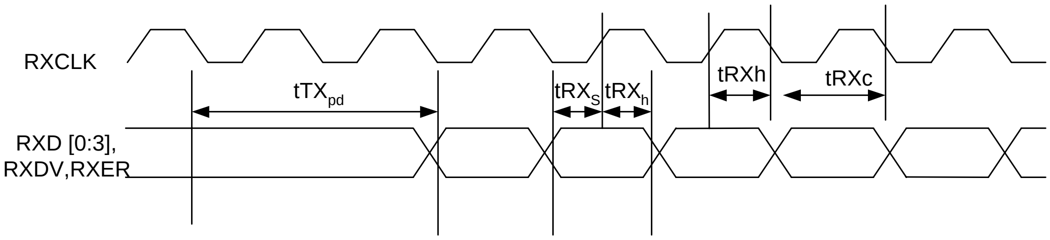
22.8 TX Transmit Timing Diagram



22.9 RX Receive Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tRXs	RXD{0:3}, RXDN, and RXER Setup to RXCLK High	0.8				
tRXh	RXD{0:3}, RXDN, and RXER Hold from RXCLK High	1				
Typical Values are at 25℃ and for design aid only; not guaranteed and not subject to production testing.						

22.10 RX Receive Timing Diagram



23. Instruction Set OP-Code and Clock Cycles

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	

immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	

Function	**Format**				**Clocks**	**Notes**
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	

AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	
CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	

JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp		1/9	
JNBE/JA = not below or equal/above	01110111	disp		1/9	
JNP/JPO = not parity/parity odd	01111011	disp		1/9	
JNO = not overflow	01110001	disp		1/9	
JNS = not sign	01111001	disp		1/9	

Function	Format			Clocks	Notes
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = Retum from procedure					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = Unconditional jump					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	

ES	00100110		2	

24. R2020C Execution Timing

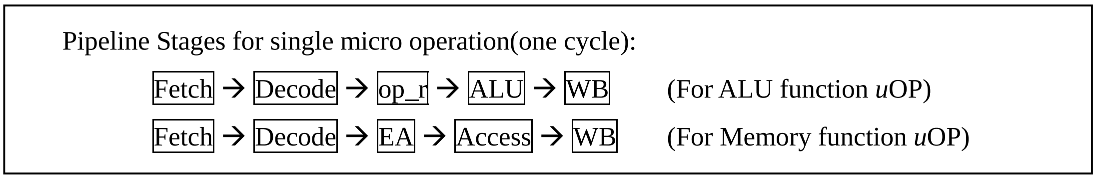
The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.

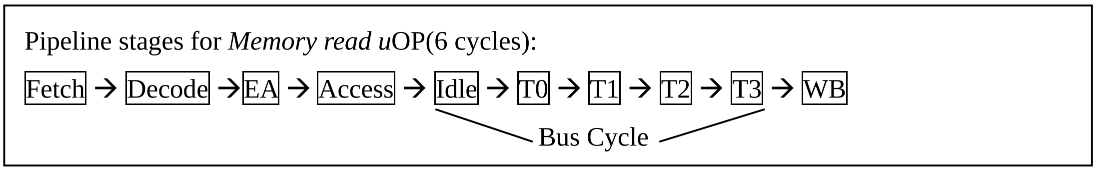
2. No wait states or bus HOLDs occur.

3. All word -data are located on even-address boundaries.

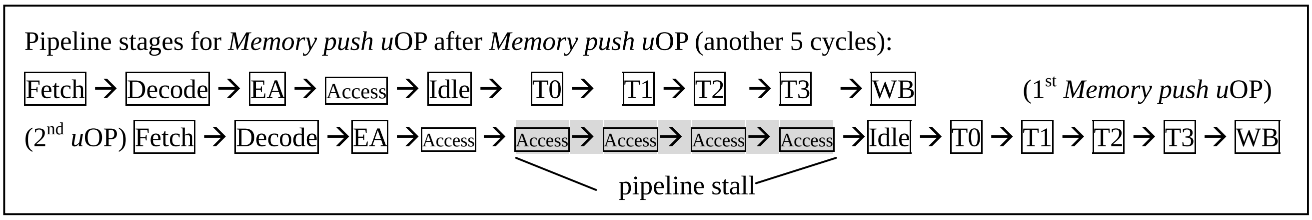
4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:



4.1 *Memory read u*OP need 6 cycles for bus.

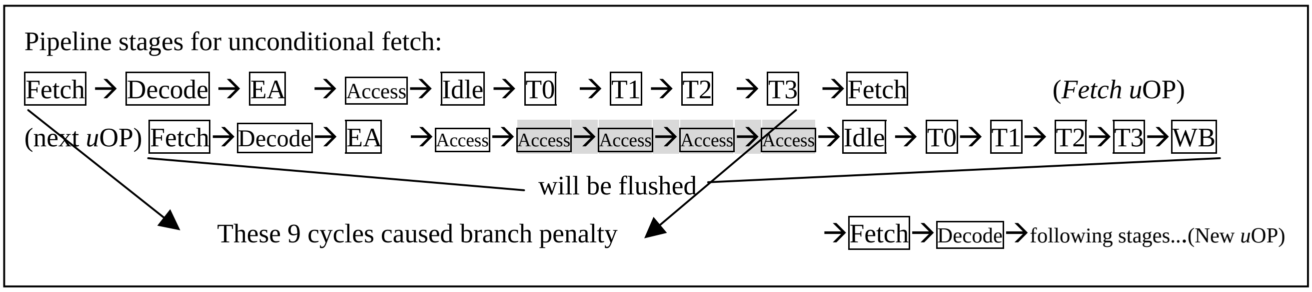


4.2 *Memory push u*OP need 1 cycle if it has no previous *Memory push u*OP, and 5 cycles if it has previous *Memory push* or *Memory Write u*OP.



4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8 bits operation need both 8 cycles, for 16 bits operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*Unconditional Fetch u*OP) will need 9 cycles.

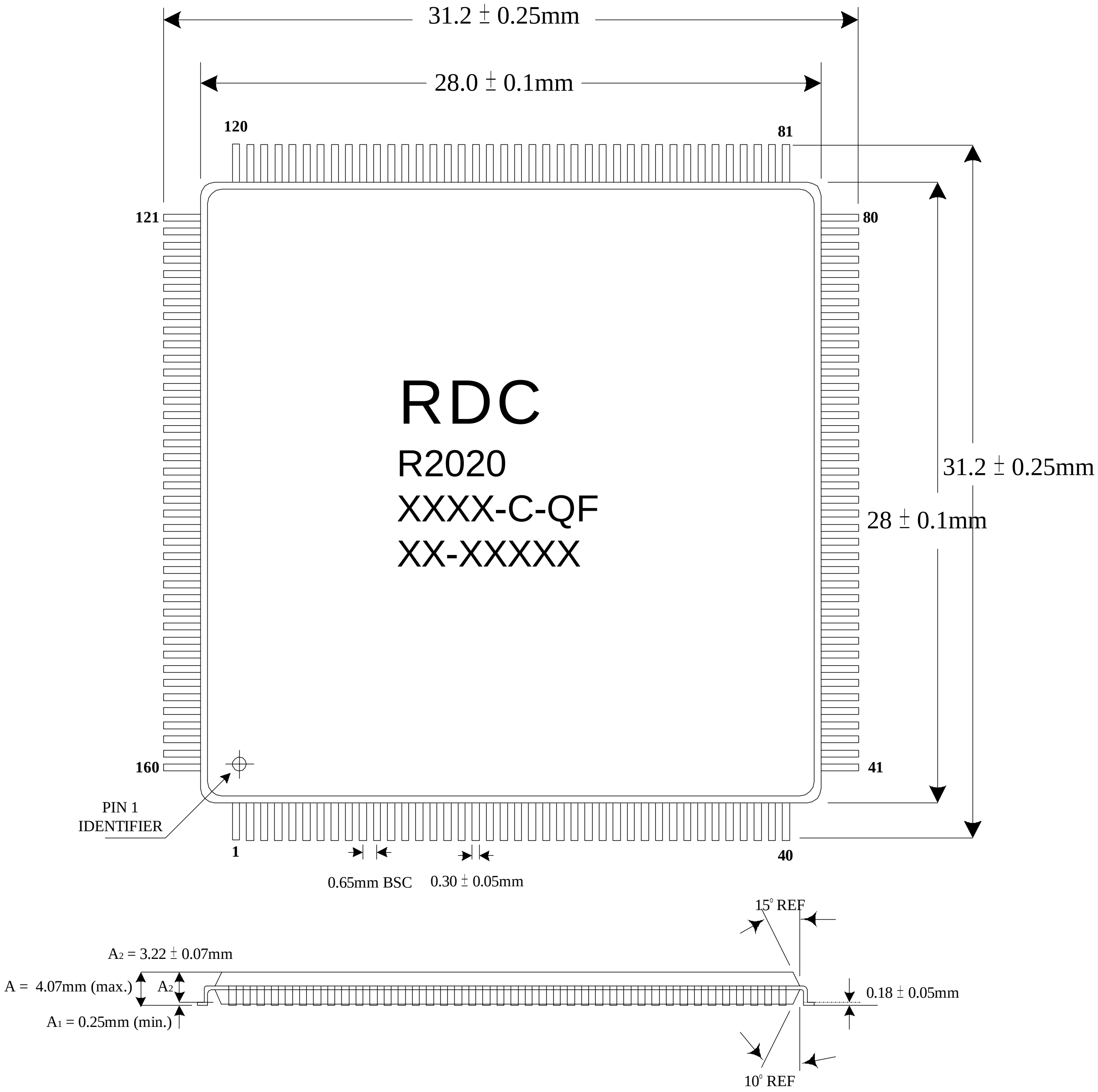


Note: op_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage,

Access: Access data from cache memory stage.

25. Package Information

25.1 PQFP 160 pins



26. Revision History

Rev.	Date	History
D01	09/03/2002	Draft Version 0.1
D02	10/23/2002	Draft Version 0.2
D03	11/13/2002	Draft Version 0.3
D04	12/31/2002	Draft Version 0.4
P01	01/23/2003	Preliminary Version 0.1
P02	02/10/2003	Preliminary Version 0.2
F10	02/17/2003	Final Version 1.0
F11	03/18/2003	Final Version 1.1 1. page 13 (Pin 14 & 15): the third line from bottom The INT6/5 are edge-triggered only and must be held until the interrupt is acknowledged.＝＞The INT6/5 are **level-triggered** only. 2. page 43: Insert one paragraph of descriptions for A6h register. 3. page 104: Bit 6 & 5 for F4h register are modified to be **Reserved.**
F12	04/02/2003	Final Version 1.2 1. page 52~55: Register 3E, 3C, 3A, 38, 36, and 34 bit 5: ES－＞ELS; Edge Select－＞Edge/Level Select. 2. page 52~54: Register 3E, 3C, 3A, and 38 bit 4: Description modifications.
F13	05/27/2003	Final Version 1.3 1. page 11 & 32: Delete all the related ONCE information due to lack of the ONCE pins. 2. page 65: Description for Bit 13 in Register DAh: Set 0: Disable the **increment** function. 3. page 132: Change the contents for Absolute Maximum Ratings table.
F14	07/08/2003	Final Version 1.4 1. page 44: Register A6h, bit 1-0, line3, MCS3_n~MCS0_n－＞MCS_n. 2. page 50: Table for Chapter 13.1, add “h” to all the figures of EOI Type. 3. page 51: descriptions for Chapter 13.3, delete the related information about slave mode. 4. page 64 & 65: Register C2h & C0h, Destination－＞Source. 5. page 71: Figure for Timer / Counter Unit Block, 58h: Compare－＞Count; 62h: Count－＞Compare. 6. page 95 & 96: Register 74h & 70h, PIO Data Bus－＞PIO Data Bits. 7. page 106: Register F6h, bit 12, Set 1: 1 clock cycle; Set 0: 2 clocks cycle.－＞ Set1: 2 clocks cycle; Set 0: 1 clock cycle.
F15	10/27/2003	Page 23 (PLL Configuration Table): Change the first line of Output Clock from “**25MHz**” into “**Reserved**”.