

Overview

The LC89970 and LC89970M are CCD delay lines for PAL television systems. It incorporates a comb filter for chrominance signal and a 1 H delay line for luminance signal.

Structure

- NMOS + CCD

Functions

- Two CCD shift registers (for chrominance and luminance signals)
- CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- Sample-and-hold circuit
- PLL 3 × frequency multiplier
- fsc clock output circuit
- RD voltage generator

Features

- 5 V single-voltage power supply
- Built-in PLL 3 × frequency multiplier circuit allows 3 fsc operation from an fsc (4.43 MHz) input.
- Control pin switchable to handle PAL/GBI and 4.43 MHz NTSC systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

Specifications

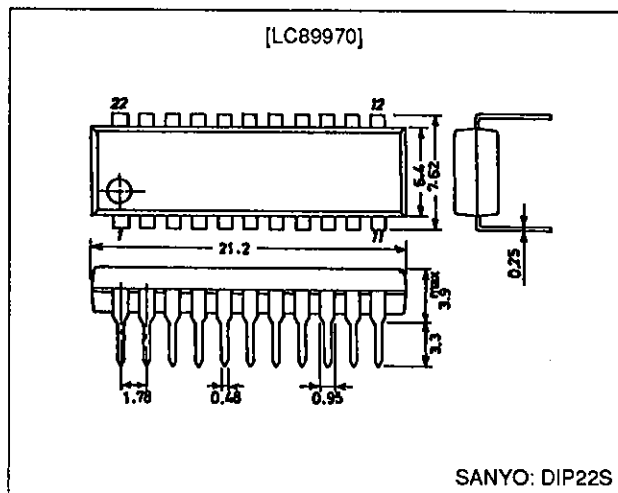
Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|------------|--------------|------|
| Maximum supply voltage | V _{DD} max | | -0.3 to +6.0 | V |
| Allowable power dissipation | Pd max | LC89970 | 1200 | mW |
| | | LC89970M | 600 | mW |
| Operating temperature | T _{opr} | | -10 to +70 | °C |
| Storage temperature | T _{stg} | | -55 to +150 | °C |

Package Dimensions

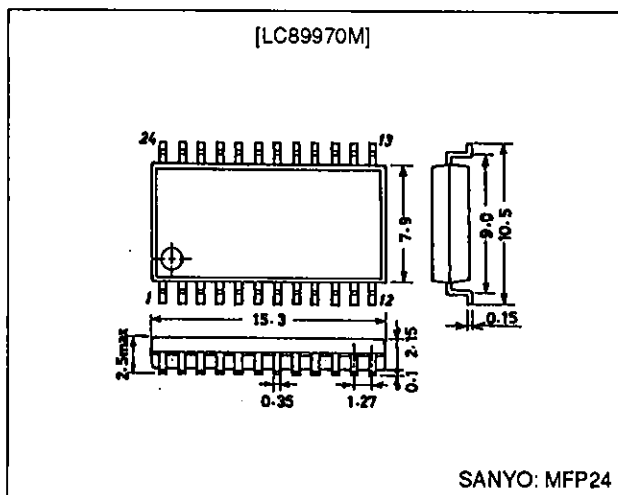
unit: mm

3059-DIP22S



unit: mm

3045B-MFP24



Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|----------------------------------|-------------------|------------|------|------------|------|-------|
| Supply voltage | V _{DD} | | 4.75 | 5.00 | 5.25 | V |
| Clock input amplitude | V _{CLK} | | 300 | 500 | 1000 | mVp-p |
| Clock frequency | F _{CLK} | Sine wave | — | 4.43361875 | — | MHz |
| Clock signal input amplitude | V _{IN-C} | | — | 350 | 500 | mVp-p |
| Luminance signal input amplitude | V _{IN-Y} | | — | 400 | 572 | mVp-p |

Electrical Characteristics at V_{DD} = 5.0 V, Ta = 25°C, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

| Parameter | Symbol | Switch states | | | Conditions | min | typ | max | Unit |
|---|---------------------|---------------|-----|------|------------|------|-----|------|-------|
| | | SW1 | SW2 | SW3 | | | | | |
| Supply current | I _{DD-1} | a | a | b | 1 | 40 | 50 | 60 | mA |
| | I _{DD-2} | b | a | b | | | | | |
| Chrominance System Characteristics (with no Y-IN input) | | | | | | | | | |
| Pin voltage (input) | V _{INC-1} | a | a | b | 2 | 2.0 | 2.4 | 2.8 | V |
| | V _{INC-2} | b | a | b | | | | | |
| Pin voltage (output) | V _{OUYC-1} | a | a | b | 2 | 1.2 | 1.6 | 2.0 | V |
| | V _{OUTC-2} | b | a | b | | | | | |
| Voltage gain | G _{VC-1} | a | a | b | 3 | -2 | 0 | +2 | dB |
| | G _{VC-2} | b | a | b | | | | | |
| Comb depth | C _{D-1} | a | a | b | 4 | — | -40 | -35 | dB |
| | C _{D-2} | b | a | b | | | | | |
| Linearity | L _{NC-1} | a | a | b | 5 | -0.3 | 0.0 | +0.3 | dB |
| | L _{NC-2} | b | a | b | | | | | |
| Clock leakage (3 fsc) | L _{CK3C-1} | a | a | b | 6 | — | 10 | 50 | mVrms |
| | L _{CK3C-2} | b | a | b | | | | | |
| Clock leakage (fsc) | L _{CK1C-1} | a | a | b | 6 | — | 0.8 | 1.5 | mVrms |
| | L _{CK1C-2} | b | a | b | | | | | |
| Noise | N _{C-1} | a | a | b | 7 | — | 0.5 | 2.0 | mVrms |
| | N _{C-2} | b | a | b | | | | | |
| Output impedance | Z _{OC-1} | a | a | a, b | 8 | 200 | 350 | 500 | Ω |
| | Z _{OC-2} | b | a | a, b | | | | | |
| OH delay time | T _{DC-1} | a | a | b | 9 | — | 245 | — | ns |
| | T _{DC-2} | b | a | b | | | | | |

Continued from preceding page.

| Parameter | Symbol | Switch states | | | Conditions | min | typ | max | Unit |
|---|---------------------|---------------|-----|------|------------|-----|-------|-----|-------|
| | | SW1 | SW2 | SW3 | | | | | |
| Luminance System Characteristics (with no C-IN1 or C-IN2 input) | | | | | | | | | |
| Pin voltage (input) | V _{INY-1} | a | a | b | 10 | 1.7 | 2.1 | 2.5 | V |
| | V _{INY-2} | b | a | b | | | | | |
| Pin voltage (output) | V _{OUTY-1} | a | a | b | 10 | 0.8 | 1.2 | 1.6 | V |
| | V _{OUTY-2} | b | a | b | | | | | |
| Voltage gain | G _{VY-1} | a | a | b | 11 | -2 | 0 | +2 | dB |
| | G _{VY-2} | b | a | b | | | | | |
| Frequency response | G _{FY-1} | a | b | b | 12 | -2 | 0 | +2 | dB |
| | G _{FY-2} | b | b | b | | | | | |
| Differential gain | D _{GY-1} | a | a | b | 13 | 0 | 5 | 7 | % |
| | D _{GY-2} | b | a | b | | | | | |
| Differential phase | D _{PY-1} | a | a | b | 13 | 0 | 5 | 7 | deg |
| | D _{PY-2} | b | a | b | | | | | |
| Linearity | L _{SY-1} | a | a | b | 14 | 37 | 40 | 43 | % |
| | L _{SY-2} | b | a | b | | | | | |
| Clock leakage (3 tsc) | L _{CK3Y-1} | a | a | b | 15 | — | 10 | 50 | mVrms |
| | L _{CK3Y-2} | b | a | b | | | | | |
| Clock leakage (tsc) | L _{CK1Y-1} | a | a | b | 15 | — | 0.8 | 1.5 | mVrms |
| | L _{CK1Y-2} | b | a | b | | | | | |
| Noise | N _{y-1} | a | a | b | 16 | — | 0.5 | 2.0 | mVrms |
| | N _{y-2} | b | a | b | | | | | |
| Output impedance | Z _{OY-1} | a | a | c, b | 17 | 250 | 400 | 550 | Ω |
| | Z _{OY-2} | b | a | c, b | | | | | |
| Delay time | T _{DY-1} | a | a | b | 18 | — | 63.92 | — | μs |
| | T _{DY-2} | b | a | b | | | | | |

Test Conditions

1. Supply current with no signal input.
2. C-OUT voltage (center bias voltage) with no signal input.
3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$GVC = 20 \log \frac{\text{C-OUT output [mVp-p]}}{350 \text{ [mVp-p]}} \text{ [dB]}$$

Test frequencies

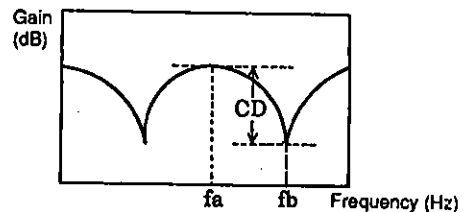
- GVC-1 4.429662 MHz (PAL/GBI)
- GVC-2 4.425694 MHz (4.43 NTSC)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

$$CD = 20 \log \frac{\text{C-OUT output with fb input [mVp-p]}}{\text{C-OUT output with fa input [mVp-p]}} \text{ [dB]}$$

Test frequencies

- | | fa | fb |
|------|--------------|--------------------------|
| CD-1 | 4.429662 MHz | 4.425756 MHz (PAL/GBI) |
| CD-2 | 4.425694 MHz | 4.417819 MHz (4.43 NTSC) |



5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

$$\text{LNC} = 20 \log \left(\frac{\text{Output for a 500 mVp-p input [mVp-p]}}{500 \text{ [mVp-p]}} / \frac{\text{Output for a 200 mVp-p input [mVp-p]}}{200 \text{ [mVp-p]}} \right) \text{ [dB]}$$

Test frequencies

- LNC-1 4.429662 MHz (PAL/GBI)
LNC-2 4.425694 MHz (4.43 NTSC)

6. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input.
7. Measure the noise in the C-OUT output with no input.
Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.
8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$\text{ZOC} = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [\Omega]}$$

Test frequencies

- ZOC-1 4.429662 MHz (PAL/GBI)
ZOC-2 4.425694 MHz (4.43 NTSC)

9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)
10. Y-OUT voltage (clamp voltage) with no signal input.
11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

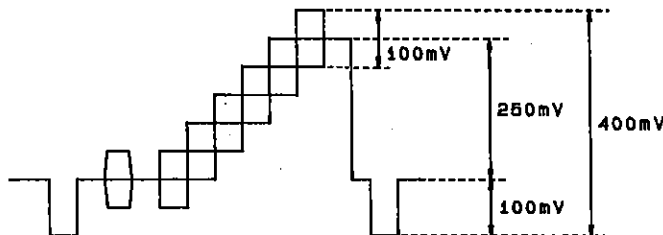
$$\text{GVY} = 20 \log \frac{\text{Y-OUT output [mVp-p]}}{400 \text{ [mVp-p]}} \text{ [dB]}$$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

$$\text{GFY} = 20 \log \frac{\text{Y-OUT output with a 3.3 MHz input [mVp-p]}}{\text{Y-OUT output with a 200 kHz input [mVp-p]}} \text{ [dB]}$$

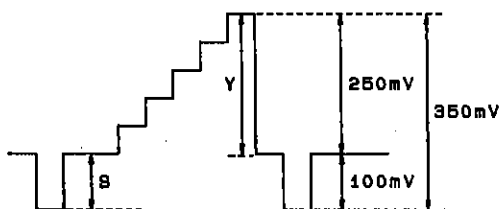
Note that V_{bias} should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



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14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



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$$LS = \frac{S \text{ [mV]}}{Y \text{ [mV]}} \times 100 \text{ [%]}$$

15. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input.

16. Measure the noise in the Y-OUT output with no input.

Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 5 MHz low-pass filter, and a 4.43 MHz trap filter.

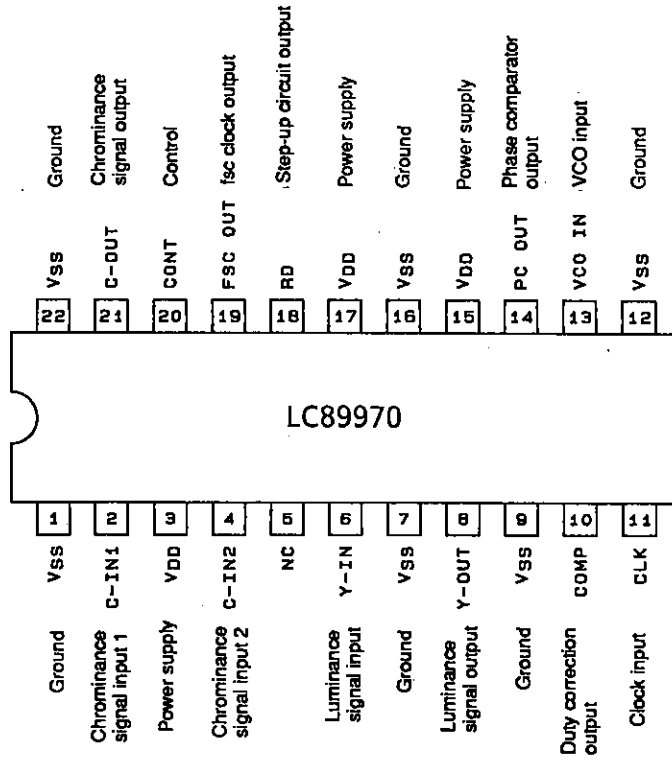
17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW3 set to c, and let V2 be the C-OUT output with SW3 set to b.

$$ZOY = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [\Omega]}$$

18. The Y-OUT delay time with respect to Y-IN

LC89970, 89970M

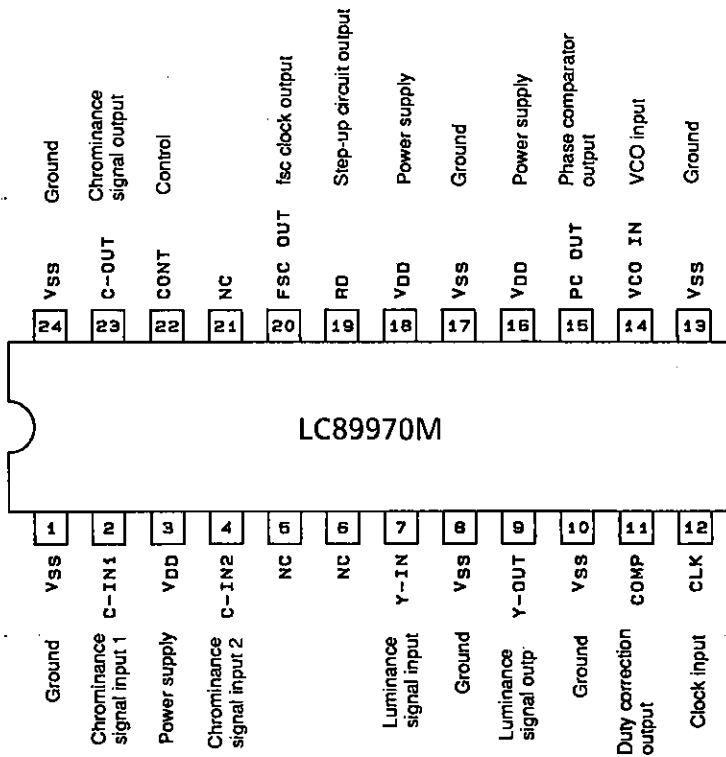
Pin Assignment [LC89970]



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Top view

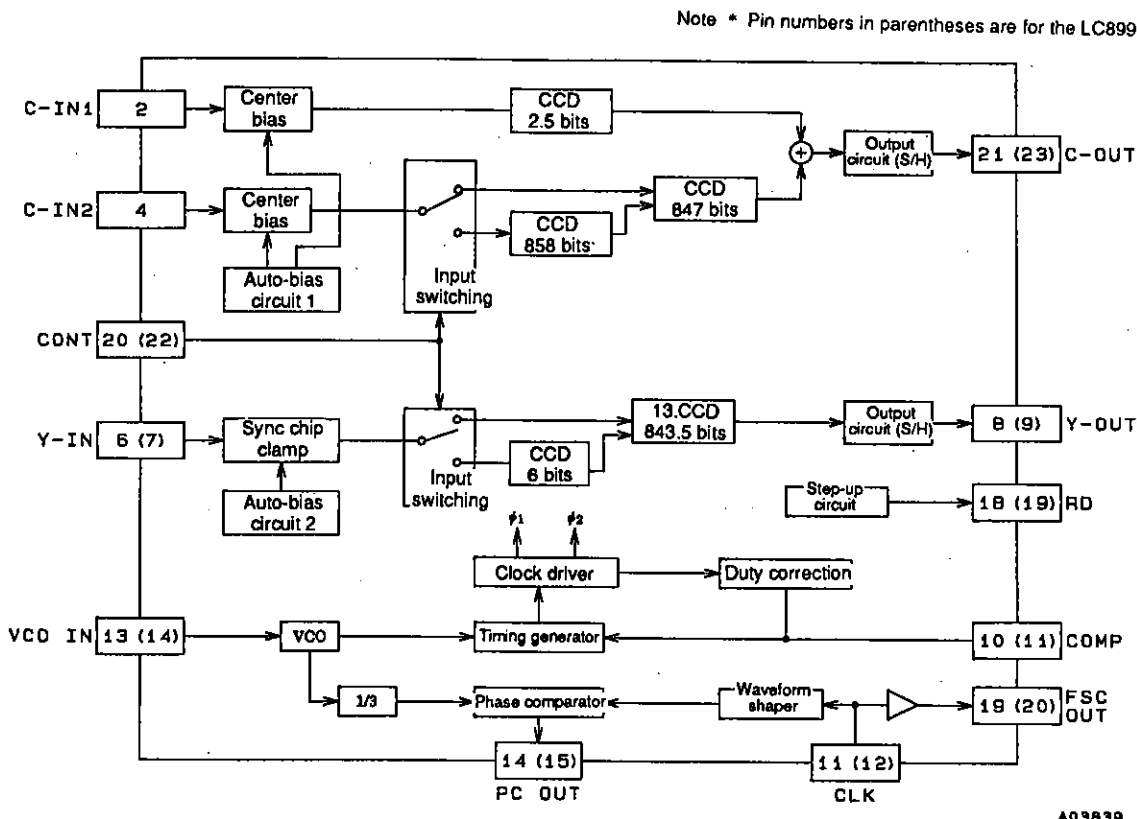
Pin Assignment [LC89970M]



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Top view

Block Diagram



Control Pin Function

| CONT | Mode (representative example) | Chrominance signal delay (CCD bits) | Luminance signal delay (CCD bits) |
|------|-------------------------------|-------------------------------------|-----------------------------------|
| Low | PAL/GBI | 2 H (1705) + 0 H (2.5) | 1 H (849.5) |
| High | 4.43 NTSC | 1 H (847) + 0 H (2.5) | 1 H (843.5) |

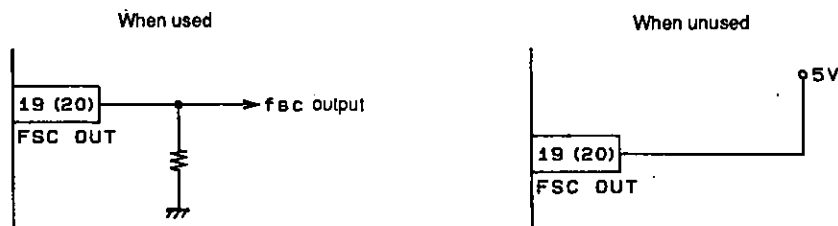
Switching Voltage Levels

| Low/high | Symbol | min. | typ | max | Unit |
|----------|----------------|------|-----|-----|------|
| Low | V _L | -0.3 | 0.0 | 0.5 | V |
| High | V _H | 2.0 | 5.0 | 6.0 | V |

Note: Since the control pin has a built-in pull-down resistor, the pin will be set to the low state if left open.

FSC OUT Pin Function

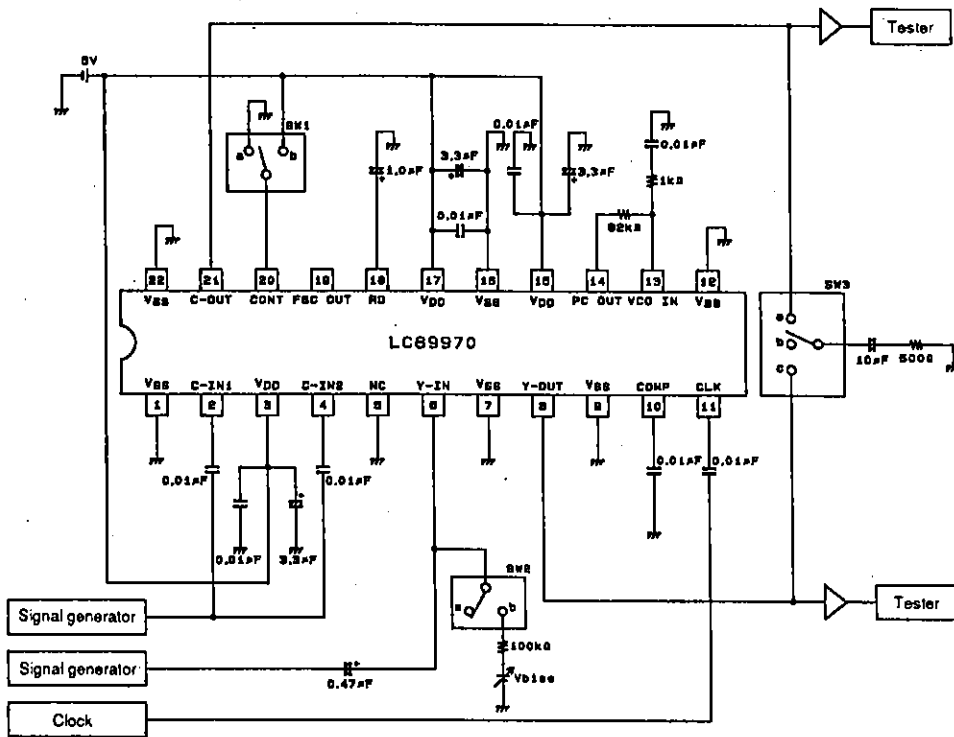
This pin provides a buffer output for the clock signal input to the CLK pin.



Note: Since this pin has a built-in pull-up resistor, the pin voltage will go to the supply voltage and output will cease if left open.

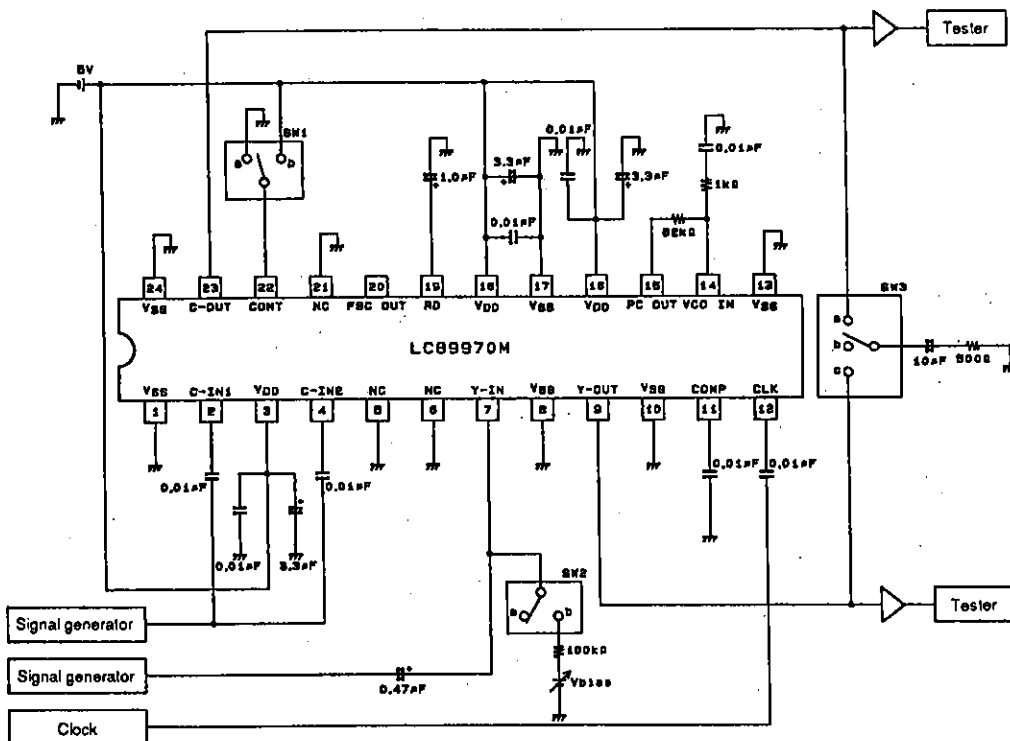
LC89970, 89970M

Test Circuit [LC89970]



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Test Circuit [LC89970M]



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