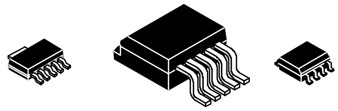


TPS72501
TPS72515, TPS72516
TPS72518, TPS72525

SLVS341B – MAY 2002 – REVISED SEPTEMBER 2002

LOW INPUT VOLTAGE, 1-A LOW-DROPOUT LINEAR REGULATORS WITH SUPERVISOR

FEATURES

- **1-A Output Current**
- **Available in 1.5-V, 1.6-V, 1.8-V, 2.5-V Fixed-Output and Adjustable Versions (1.2-V to 5.5-V)**
- **Input Voltage Down to 1.8 V**
- **Low 170-mV Dropout Voltage at 1 A (TPS72525)**
- **Stable With Any Type/Value Output Capacitor**
- **Integrated Supervisor (SVS) With 50-ms $\overline{\text{RESET}}$ Delay Time**
- **Low 210-µA Ground Current at Full Load (TPS72525)**
- **Less than 1-µA Standby Current**
- **±2% Output Voltage Tolerance Over Line, Load, and Temperature (–40°C to 125°C)**
- **Integrated UVLO**
- **Thermal and Overcurrent Protection**
- **5-Lead SOT223–5 or DDPAK and 8–Pin SOP (TPS72501 only) Surface Mount Package**

APPLICATIONS

- **PCI Cards**
- **Modem Banks**
- **Telecom Boards**
- **DSP, FPGA, and Microprocessor Power Supplies**
- **Portable, Battery Powered Applications**

DESCRIPTION

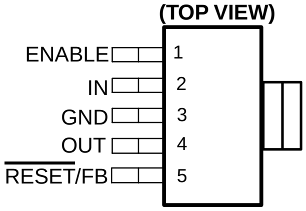
The TPS725xx family of 1-A low-dropout (LDO) linear regulators has fixed voltage options available that are commonly used to power the latest DSPs, FPGAs, and microcontrollers. An adjustable option ranging from 1.22 V to 5.5 V is also available. The integrated supervisory circuitry provides an active low $\overline{\text{RESET}}$ signal when the output falls out of regulation. The no capacitor/any capacitor feature allows the customer to tailor output transient performance as needed. Therefore, compared to other regulators capable of providing the same output current, this family of regulators can provide a stand alone power supply solution or a post regulator for a switch mode power supply.

These regulators are ideal for higher current applications. The family operates over a wide range of input voltages (1.8 V to 6 V) and has very low dropout (170 mV at 1-A).

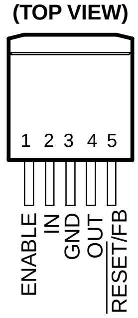
Ground current is typically 210 µA at full load and drops to less than 80 µA at no load. Standby current is less than 1 µA.

Each regulator option is available in either a SOT223–5, D (TPS72501 only), or DDPAK package. With a low input voltage and properly heatsinked package, the regulator dissipates more power and achieves higher efficiencies than similar regulators requiring 2.5 V or more minimum input voltage and higher quiescent currents. These features make it a viable power supply solution for portable, battery powered equipment.

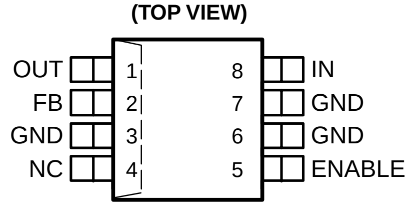
DCQ PACKAGE
SOT223-5
(TOP VIEW)



KTT PACKAGE
DDPAK
(TOP VIEW)



D PACKAGE
(TOP VIEW)



NC – No internal connection

Note: TPS72501 replaces $\overline{\text{RESET}}$ with FB, Tab is GND for the DCQ and KTT packages

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-µF output capacitor.

Unlike some regulators that have a minimum current requirement, the TPS725 family is stable with no output load current. The low noise capability of this family, coupled with its high current operation and ease of power dissipation, make it ideal for telecom boards, modem banks, and other noise sensitive applications.

ORDERING INFORMATION

T_J	VOLTAGE(1)	SOT223–5(2)	SYMBOL	DDPAK(3)	D(4)	SYMBOL
–40°C to 125°C	Adjustable (1.2 V to 5 V)	TPS72501DCQ	PS72501	TPS72501KTT	TPS72501D	TPS72501
	1.5 V	TPS72515DCQ	PS72515	TPS72515KTT	—	TPS72515
	1.6 V	TPS72516DCQ	PS72516	TPS72516KTT	—	TPS72516
	1.8 V	TPS72518DCQ	PS72518	TPS72518KTT	—	TPS72518
	2.5 V	TPS72525DCQ	PS72525	TPS72525KTT	—	TPS72525

(1) Other voltage options are available upon request from the manufacturer.
(2) To order a taped and reeled part, add the suffix R to the part number (e.g., TPS72501DCQR).
(3) To order a taped and reeled part, add the suffix T to the part number (e.g., TPS72501KTTT).
(4) To order a taped and reeled part, add the suffix R or T (2500 or 500) to the part number (e.g. TPS72501DR)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Input voltage, V_I (see Note 2)	–0.3 to 7	V
Voltage range at EN, FB	–0.3 to V_I + 0.3	V
Voltage on OUT, $\overline{\text{RESET}}$	6	V
ESD rating, HBM	2	kV
Continuous total power dissipation	See Dissipation Rating Table	
Operating junction temperature range, T_J	–50 to 150	°C
MAximum junction temperature range, T_J	150	°C
Storage temperature, T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I (see Note 1)	1.8		6	V
Continuous output current, I_O	0		1	A
Operating junction temperature, T_J	–40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_I(\text{min}) = V_O(\text{max}) + V_{DO}(\text{max\^{}load})$$

PACKAGE DISSIPATION RATINGS

PACKAGE	BOARD	$R_{\theta JC}$	$R_{\theta JA}$
DDPAK	High K(1)	2 °C/W	23 °C/W
SOT223	Low K(2)	15 °C/W	53 °C/W
D-8	High K(1)	39.4 °C/W	55 °C/W

(1) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7.5-cm x 7.5-cm), multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.
(2) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch (7.5-cm x 7.5-cm), two-layer board with 2 ounce copper traces on top of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, $C_o = 1$ µF, $C_i = 1$ µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Bandgap voltage reference				1.177	1.220	1.263	V
V_O	Output voltage	TPS72501 Adjustable	0 µA< I_O < 1 A, (1)	1.22 V ≤ V_O ≤ 5.5 V	0.965 V_O		1.035 V_O	V
		TPS72515	T_J = 25°C			1.5		
			0 µA< I_O < 1 A	1.8 V ≤ V_I ≤ 5.5 V	1.47		1.53	
		TPS72516	T_J = 25°C			1.6		
			0 µA< I_O < 1 A	2.6 V ≤ V_I ≤ 5.5 V	1.568		1.632	
		TPS72518	T_J = 25°C			1.8		
			0 µA< I_O < 1 A	2.8 V ≤ V_I ≤ 5.5 V	1.764		1.836	
		TPS72525	T_J = 25°C			2.5		
			0 µA< I_O < 1 A	3.5 V ≤ V_I ≤ 5.5 V	2.45		2.55	
I	Ground current		I_O = 0 µA			75	120	µA
			I_O = 1 A			210	300	
	Standby current		EN < 0.4 V	T_J = 25°C		0.2		µA
			EN < 0.4 V				1	
V_n	Output noise voltage		BW = 200 Hz to 100 kHz, T_J = 25°C,	C_O = 10 µF, I_O = 1 mA		150		µV
PSRR	Ripple rejection		f = 1 kHz, C_O = 10 µF,	T_J = 25°C		60		dB
	Current limit(2)				1.1	1.6	2.3	A
	Output voltage line regulation ($\Delta V_O/V_O$)(3)		V_O + 1 V < V_I ≤ 5.5 V		–0.15	0.02	0.15	%/V
	Output voltage load regulation		0 µA< I_O < 1 A		–0.25	0.05	0.25	%/A
V_{IH}	EN high level input(2)				1.3			V
V_{IL}	EN low level input(2)				–0.2		0.4	
I_I	EN input current		EN = 0 V or V_I			0.01	100	nA
$I_{(FB)}$	Feedback current		TPS72501	$V_{(FB)}$ = 1.22	–100		100	nA
	UVLO threshold		V_{CC} rising		1.45	1.57	1.70	V
	UVLO hysteresis		T_J = 25°C, V_{CC} rising			50		mV
	UVLO deglitch		T_J = 25°C, V_{CC} rising			10		µs
	UVLO delay		T_J = 25°C, V_{CC} rising			100		µs

(1) Minimum IN operating voltage used for testing is $V_{O(typ)}$ + 1 V.
(2) Test condition includes, output voltage $V_O = V_O$ – 15% and pulse duration = 10 ms.
(3) $V_{Imin} = (V_O + 1)$ or 1.8 V whichever is greater.

$$\text{Line regulation (mV)} = (\%/\text{V}) \times \frac{V_O\left(5.5\text{ V} - V_{Imin}\right)}{100} \times 1000$$

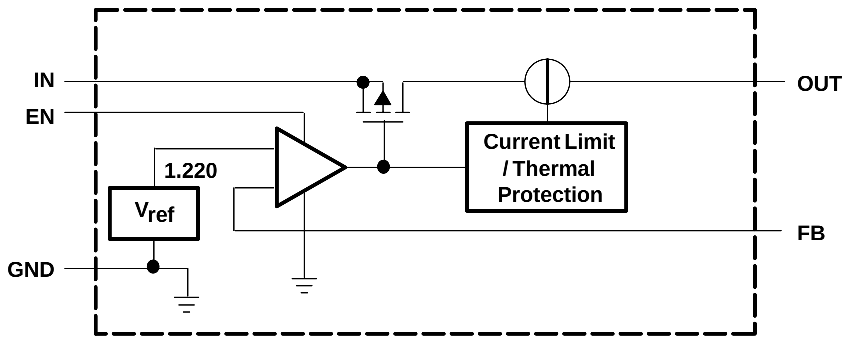
ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, I_O= 1 mA, EN = IN, $C_o = 1\ \mu F$, $C_i = 1\ \mu F$(unless otherwise noted)

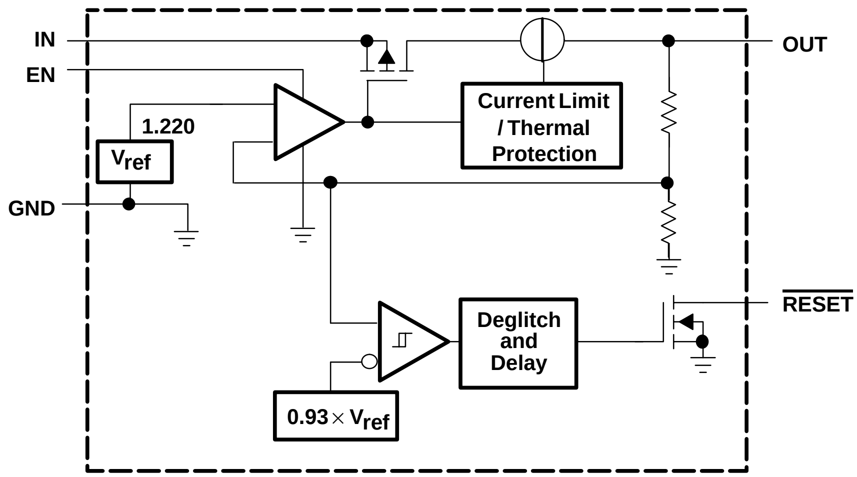
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	TPS72525(1)	I_O = 1 A	T_J = 25°C		170		mV
			I_O = 1 A				280	
		TPS72518(1)	I_O = 1 A	T_J = 25°C		210		
			I_O = 1 A				320	
$\overline{\text{RESET}}$	Minimum input voltage for valid $\overline{\text{RESET}}$				1.3			V
	Trip threshold voltage				90	93	96	$\%V_O$
	Hysteresis voltage					10		mV
	$t_{(RESET)}$ delay time				25	50	75	ms
	Rising edge deglitch					10		µs
	Output low voltage (at 700 µA)				–0.3		0.4	V
	Leakage current						100	nA

(1) Dropout voltage is defined as the differential voltage between V_O and V_I when V_O drops 100 mV below the value measured with $V_I = V_O + 1$ V.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



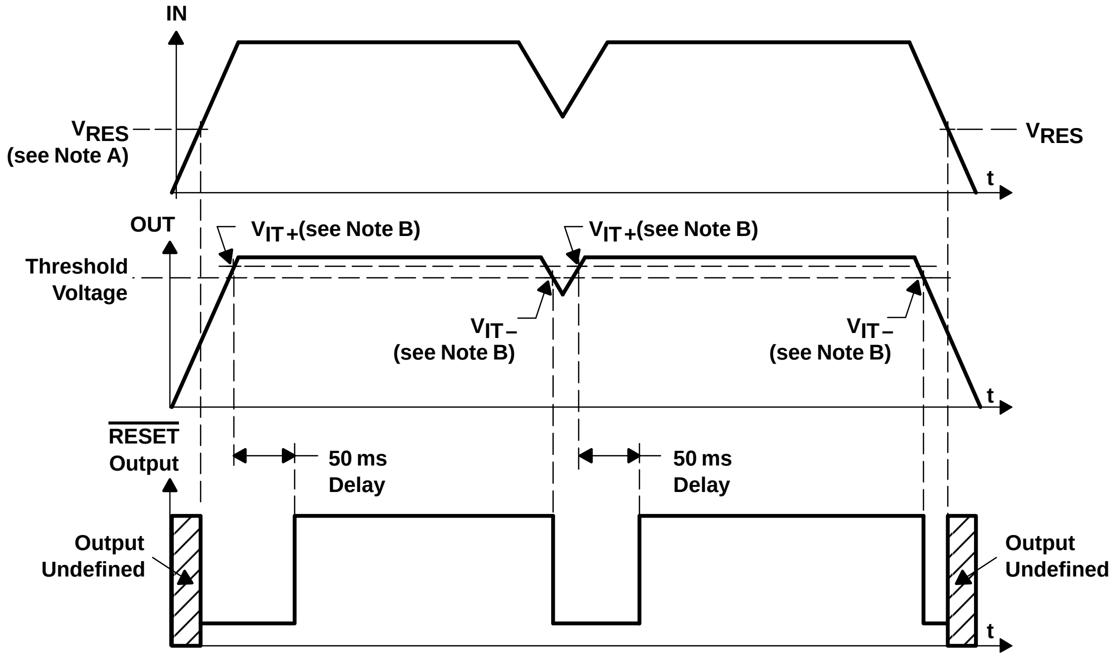
FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D	NO. DCQ & KTT		
ENABLE	5	1	I	Enable input
FB	2			Feedback
GND	3, 6, 7	3		Ground
IN	8	2	I	Input supply voltage
$\overline{\text{RESET}}$/FB	—	5	O/I	This terminal is the feedback point for the adjustable option TPS72501. For all other options, this terminal is the $\overline{\text{RESET}}$ output terminal. When used with a pullup resistor, this open-drain output provides the active low $\overline{\text{RESET}}$ signal when the regulator output voltage drops more than 5% below its nominal output voltage. The $\overline{\text{RESET}}$ delay time is typically 50 ms.
NC	4	—		No connection
OUT	1	4	O	Regulated output voltage

$\overline{\text{RESET}}$ TIMING DIAGRAM



NOTES: A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} –Trip voltage is typically 7% lower than the output voltage (93%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

TPS72518
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

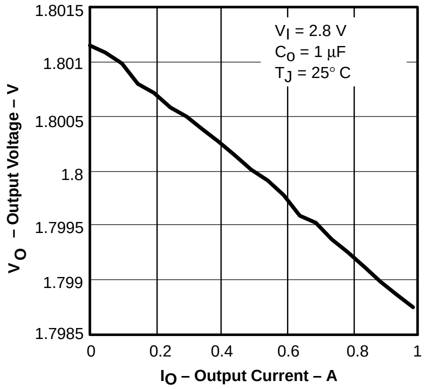


Figure 1

TPS72518
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

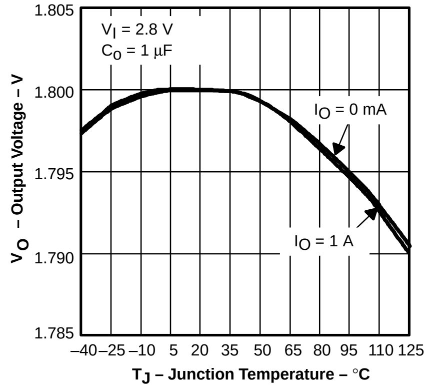


Figure 2

TPS72518
GROUND CURRENT
vs
JUNCTION TEMPERATURE

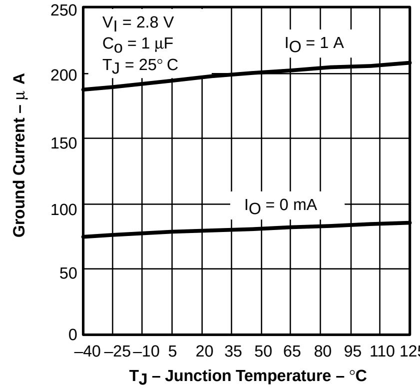


Figure 3

TPS72518
GROUND CURRENT
vs
OUTPUT CURRENT

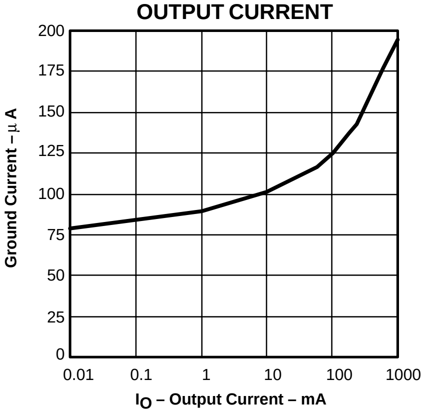


Figure 4

TPS72525
DC DROPOUT VOLTAGE
vs
OUTPUT CURRENT

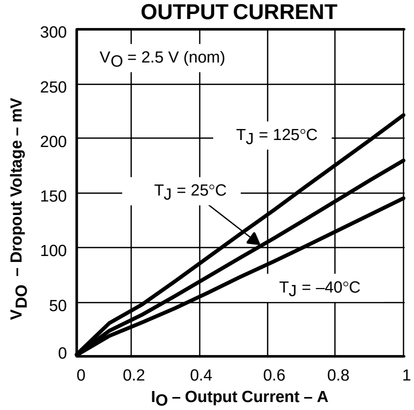


Figure 5

TPS72518
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

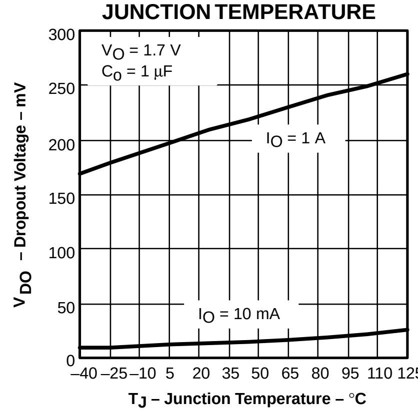


Figure 6

MINIMUM REQUIRED INPUT VOLTAGE
vs
OUTPUT VOLTAGE

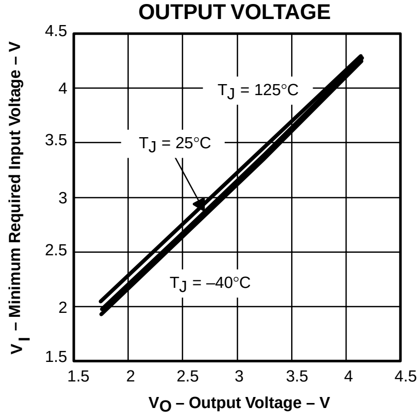


Figure 7

TPS72518
LINE TRANSIENT RESPONSE

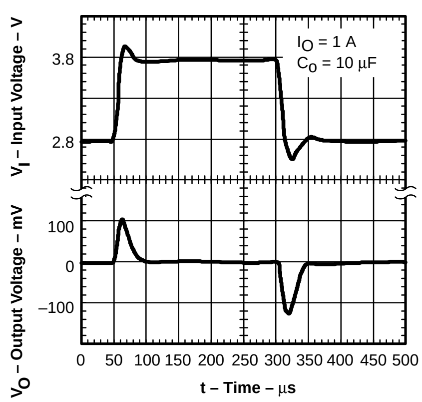


Figure 8

TPS72518
LOAD TRANSIENT RESPONSE

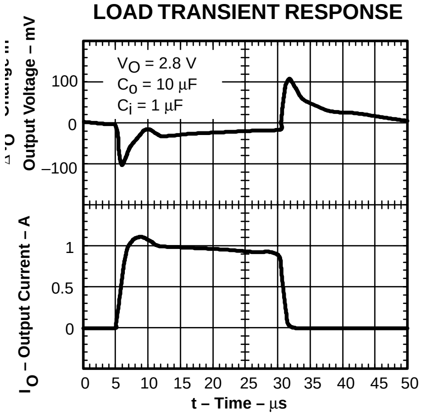


Figure 9

TEXAS INSTRUMENTS
www.ti.com

TPS72518
LOAD TRANSIENT RESPONSE

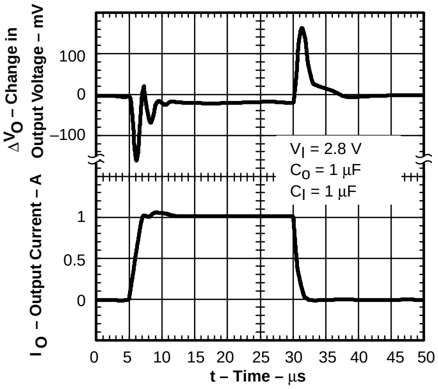


Figure 10

TPS72518
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

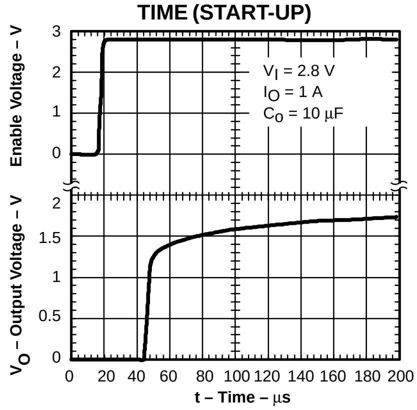


Figure 11

TPS72518
POWER UP/POWER DOWN

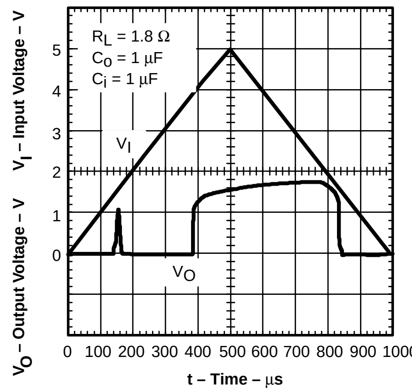


Figure 12

TPS72518
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

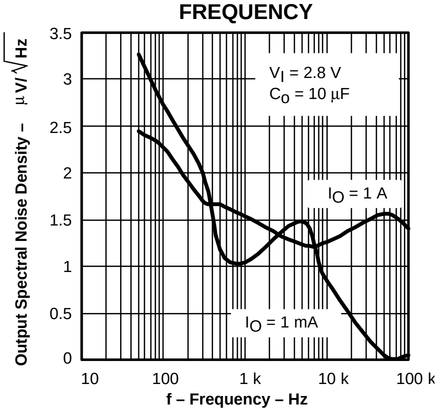


Figure 13

OUTPUT IMPEDANCE
vs
FREQUENCY

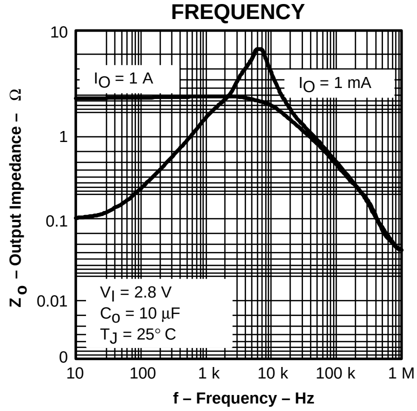


Figure 14

TPS72518
RIPPLE REJECTION
vs
FREQUENCY

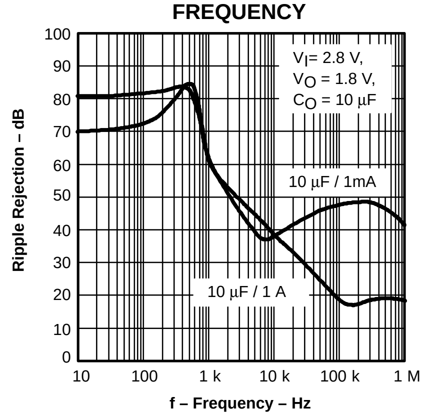


Figure 15

CURRENT LIMIT
vs
INPUT VOLTAGE

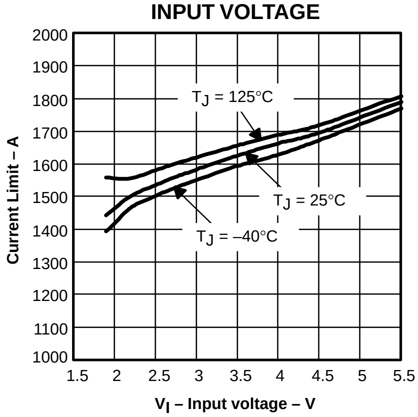


Figure 16

TPS72515
GROUND CURRENT
vs
INPUT VOLTAGE

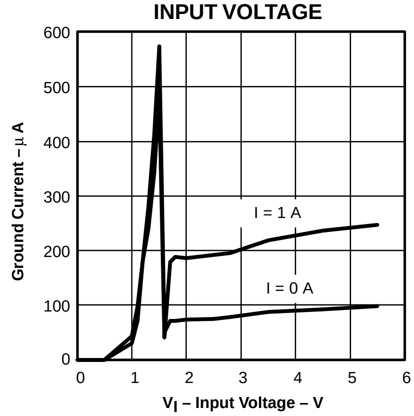


Figure 17

DROPOUT VOLTAGE
vs
INPUT VOLTAGE

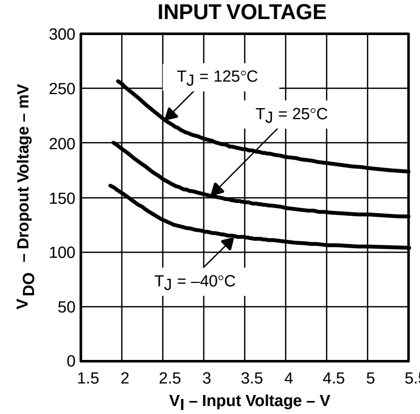


Figure 18

APPLICATION INFORMATION

The TPS725xx family of low-dropout (LDO) regulators has numerous features that make it apply to a wide range of applications. The family operates with very low input voltage (≥1.8 V) and low dropout voltage (typically 200 mV at full load), making it an efficient stand-alone power supply or post regulator for battery or switch mode power supplies. Both the active low $\overline{\text{RESET}}$ and 1-A output current, make the TPS725xx family ideal for powering processor and FPGA supplies. The TPS725xx family also has low output noise (typically 150 μV_{RMS} with 10-µF output capacitor), making it ideal for use in telecom equipment.

EXTERNAL CAPACITOR REQUIREMENTS

A 1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS725xx, is required for stability. To improve transient response, noise rejection, and ripple rejection, an additional 10-µF or larger, low ESR capacitor is recommended. A higher-value, low ESR input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source, especially if the minimum input voltage of 1.8 V is used.

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-µF output capacitor.

PROGRAMMING THE TPS72501 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS72501 adjustable regulator is programmed using an external resistor divider as shown in Figure 19. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

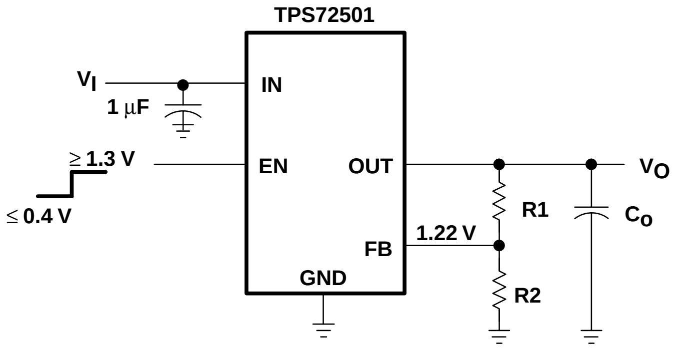
Where:

$V_{FB} = V_{ref}$ = 1.22 V typical (see the electrical characteristics for V_{ref} range)

Resistors R1 and R2 should be chosen for approximately 10-µA divider current. Lower value resistors offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 120 kΩ to set the divider current at 10 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

APPLICATION INFORMATION



OUTPUT VOLTAGE PROGRAMMING GUIDE
(Standard 1% Resistor Values)

PROGRAM VOLTAGE	R1 (KΩ)	R2 (kΩ)	ACTUAL VOLTAGE
1.8 V	56.2	118	1.801
2.5 V	127	121	2.500
3.3 V	196	115	3.299
3.6 V	205	105	3.602

Figure 19. TPS72501 Adjustable LDO Regulator Programming

REGULATOR PROTECTION

The TPS725xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS725xx also features internal current limiting and thermal protection. During normal operation, the TPS725xx limits output current to approximately 1.6 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 145°C, regulator operation resumes.

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D max = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \tag{3}$$

Where:

$V_{I(avg)}$ is the average input voltage.

$V_{O(avg)}$ is the average output voltage.

$I_{O(avg)}$ is the average output current.

$I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 20 illustrates these thermal resistances for (a) a SOT223 package mounted in a JEDEC low-K board, and (b) a DDPAK package mounted on a JEDEC high-K board.

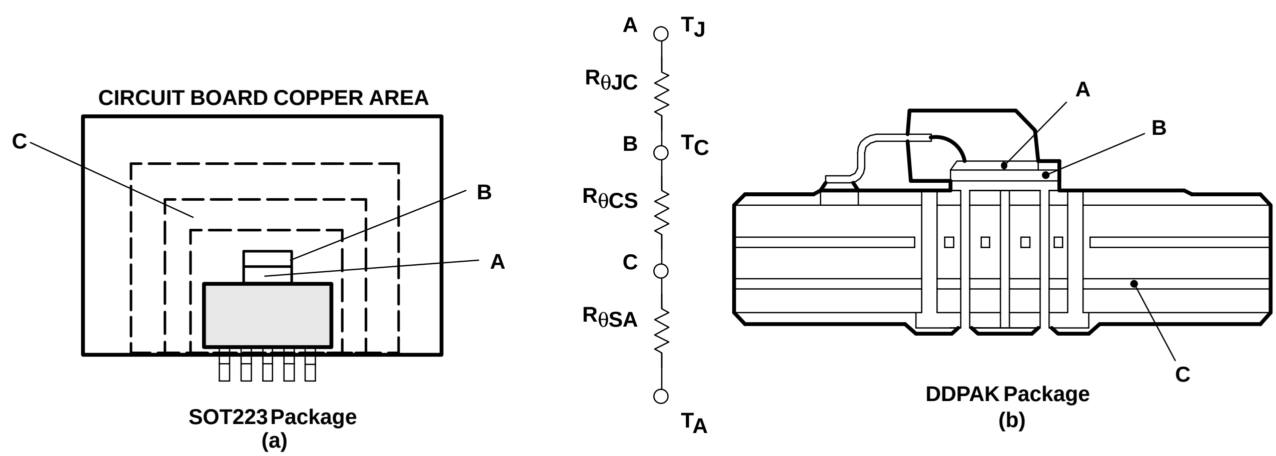


Figure 20. Thermal Resistances

THERMAL INFORMATION

Equation 4 summarizes the computation:

$$T_J = T_A + P_D\text{max x}\left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \tag{4}$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\theta CS}$ of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 4 simplifies into equation 5:

$$T_J = T_A + P_D\text{max x } R_{\theta JA} \tag{5}$$

Rearranging equation 5 gives equation 6:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D\text{max}} \tag{6}$$

Using equation 5 and the computer model generated curves shown in Figure 21 and Figure 24, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

THERMAL INFORMATION

DDPAK POWER DISSIPATION

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

To illustrate, the TPS72525 in a DDPAK package was chosen. For this example, the average input voltage is 5 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (5 - 2.5)\ V \times 1\ A = 2.5\ W \quad (7)$$

Substituting $T_J max$ for T_J into equation 6 gives equation 8:

$$R_{\theta JA} max = (125 - 55)°C / 2.5\ W = 28°C/W \quad (8)$$

From Figure 21, DDPAK Thermal Resistance vs Copper Heatsink Area, the ground plane needs to be 1 cm^2 for the part to dissipate 2.5 W. The operating environment used in the computer model to construct Figure 21 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 22 shows the side view of the operating environment used in the computer model.

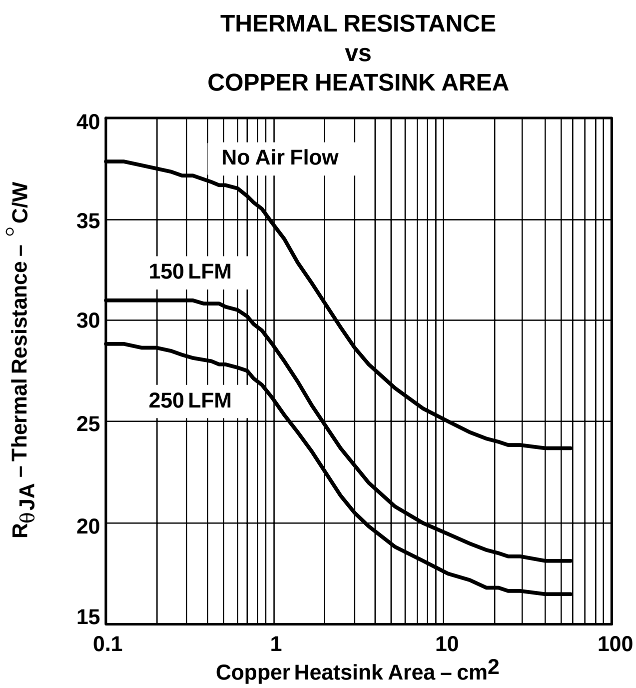


Figure 21. DDPAK Thermal Resistance vs Copper Heatsink Area

THERMAL INFORMATION

DDPAK POWER DISSIPATION (CONTINUED)

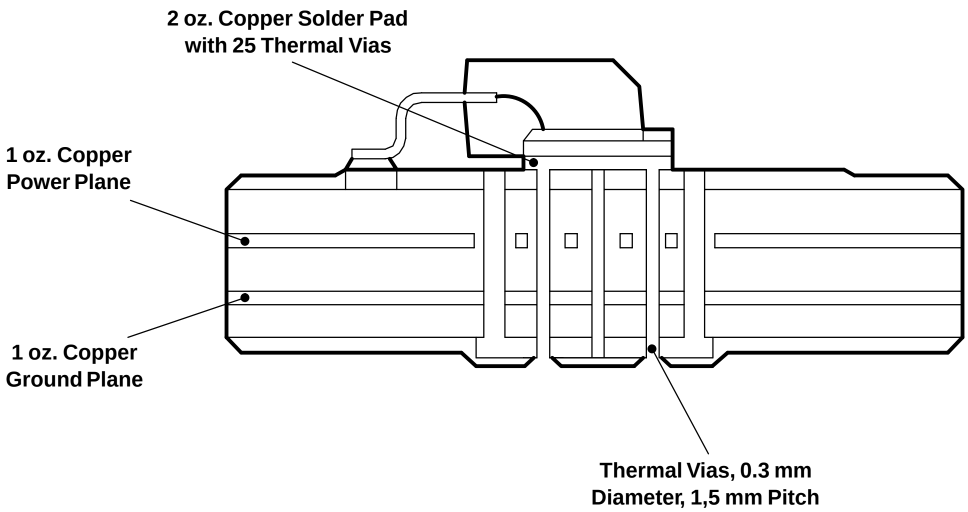


Figure 22. DDPAK Thermal Resistance

From the data in Figure 23 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

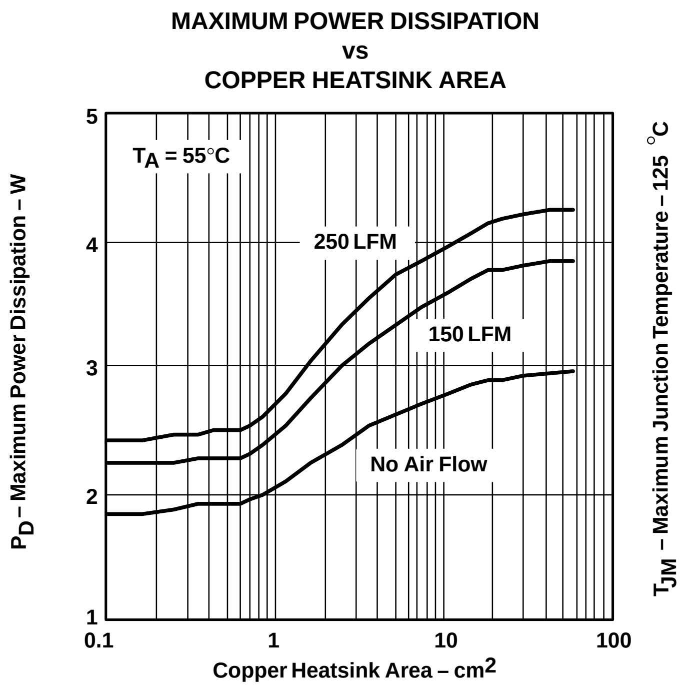


Figure 23. Maximum Power Dissipation vs Copper Heatsink Area

THERMAL INFORMATION

SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS72525 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (3.3 - 2.5)\ V \times 1\ A = 800\ mW \tag{9}$$

Substituting $T_J$max for T_J into equation 6 gives equation 10:

$$R_{\theta JA} max = (125 - 55)°C/800\ mW = 87.5°C/W \tag{10}$$

From Figure 24, $R_{\theta JA}$ vs PCB Copper Area, the ground plane needs to be 0.55 in^2 for the part to dissipate 800 mW. The operating environment used to construct Figure 24 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

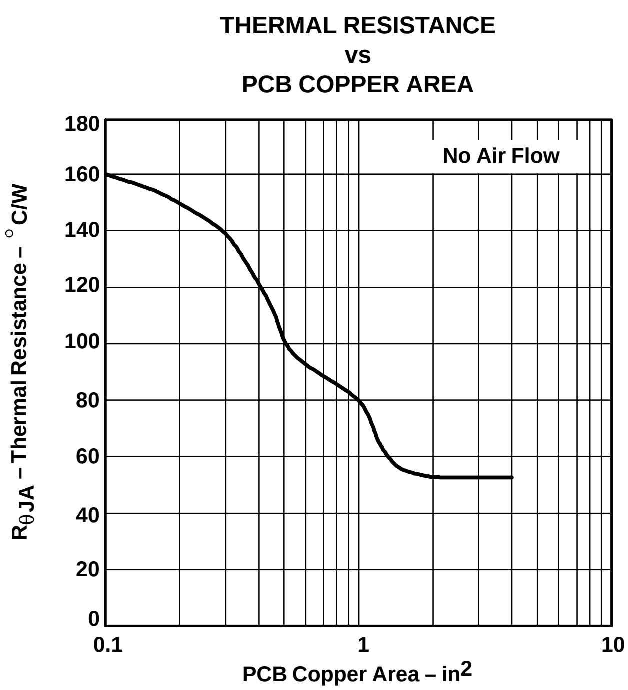


Figure 24. SOT223 Thermal Resistance vs PCB AREA

THERMAL INFORMATION

SOT223 POWER DISSIPATION (CONTINUED)

From the data in Figure 24 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (see Figure 25).

MAXIMUM POWER DISSIPATION vs COPPER HEATSINK AREA

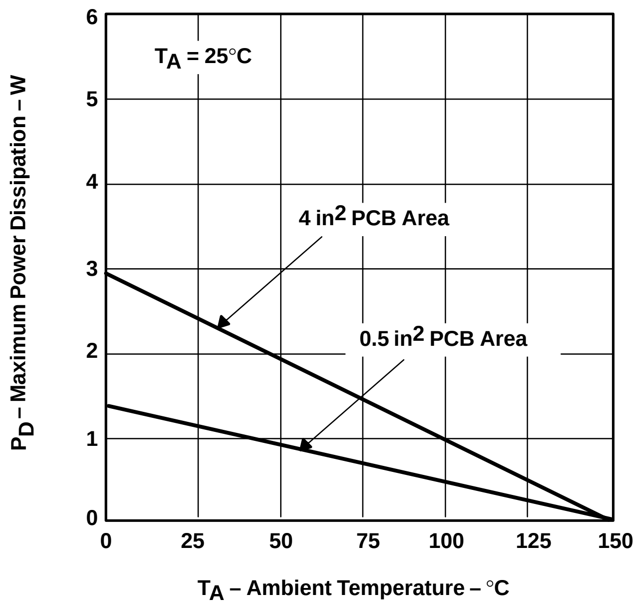
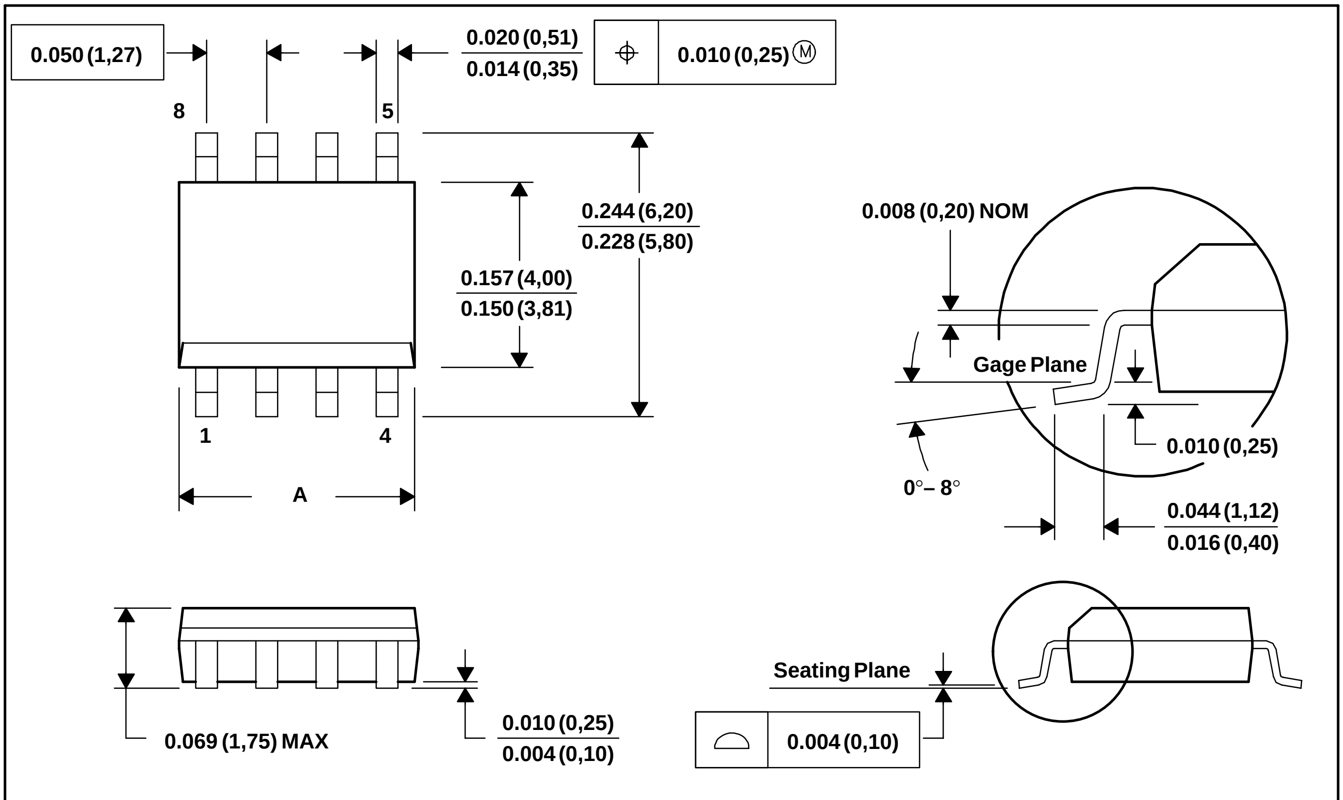


Figure 25. SOT223 Power Dissipation

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



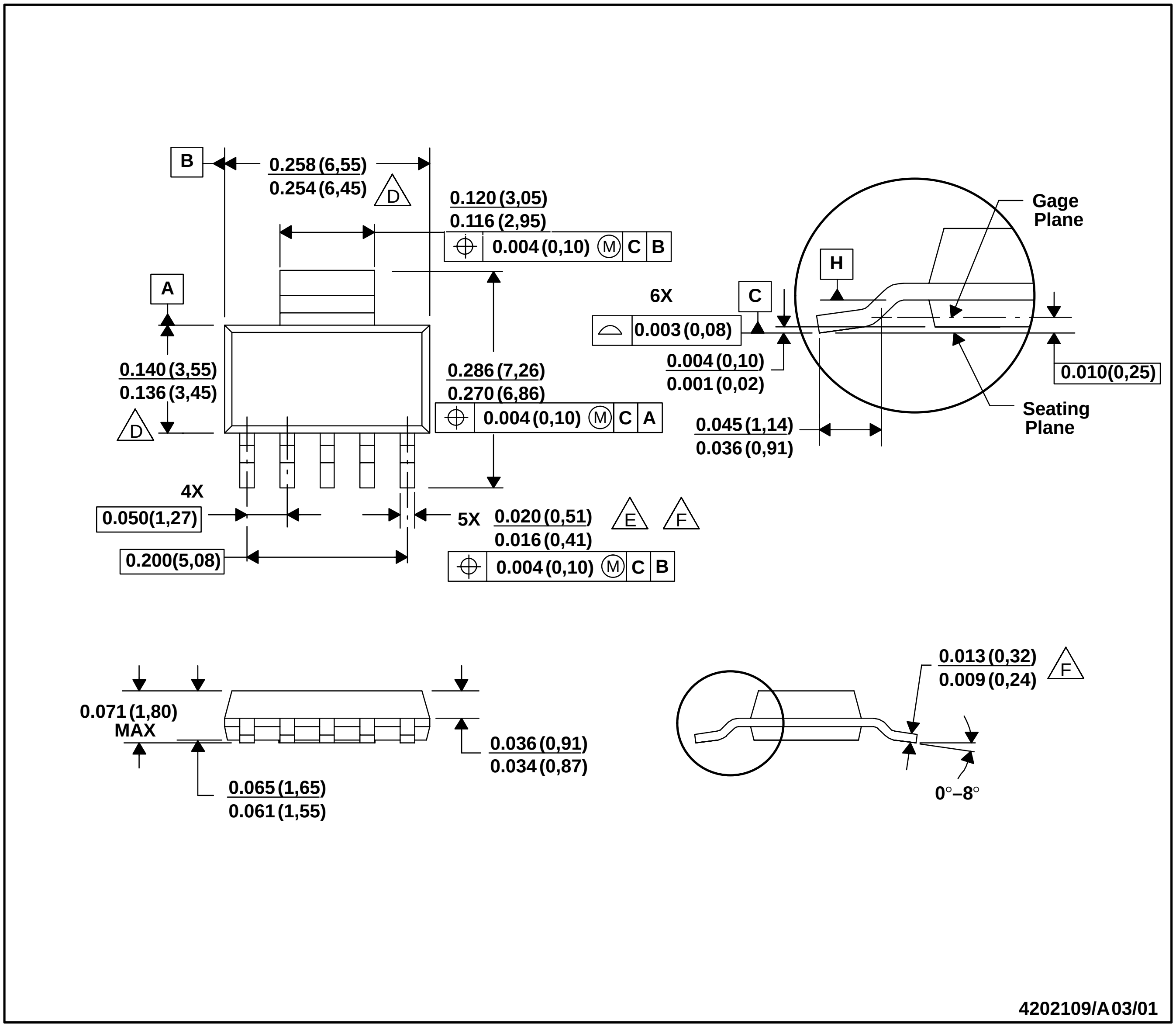
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

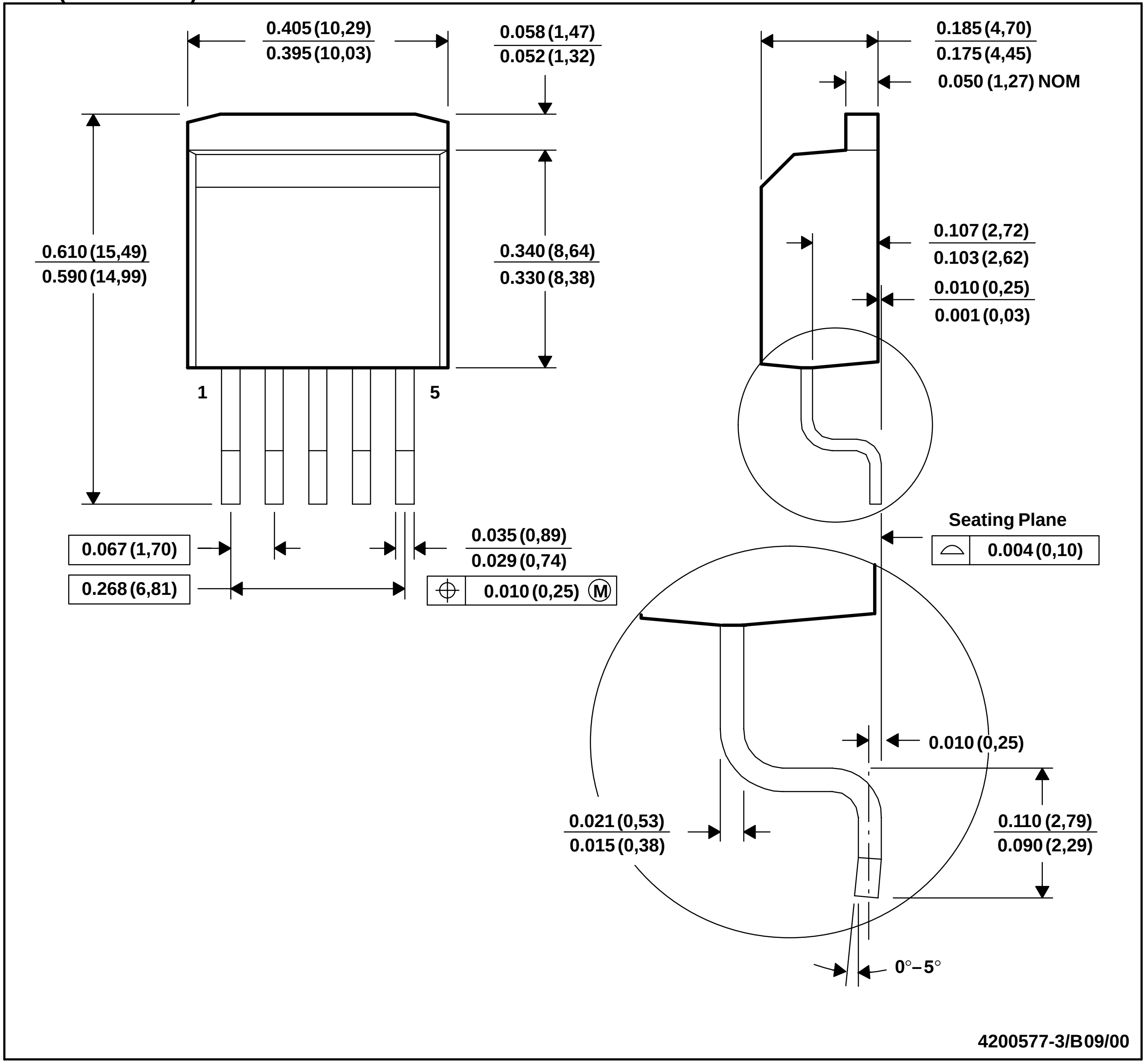
DCQ (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension in inches
D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
E. Lead width dimension does not include dambar protrusion.
F. Lead width and thickness dimensions apply to solder plated leads.
G. Interlead flash allow 0.008 inch max.
H. Gate burr/protrusion max. 0.006 inch.

MECHANICAL DATA

KTT (R-PSFM-G5) **PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

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