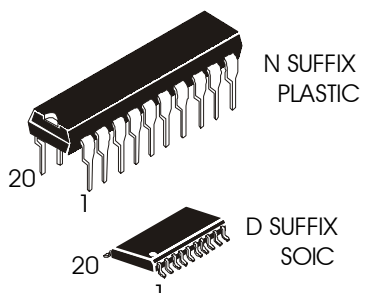


IN74LV245

OCTAL BUS TRANSCEIVER (3-State)

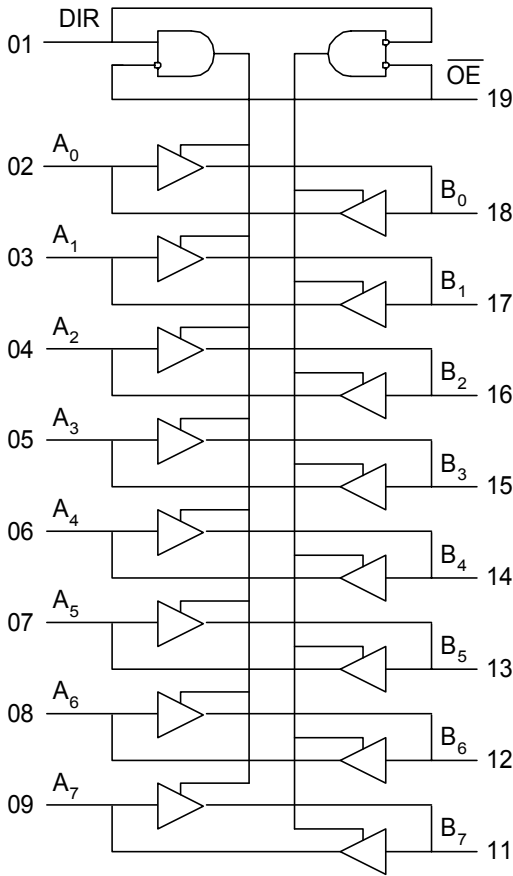
By pinning IN74LV245 are compatible with IN74HC245A and IN74HCT245A series. Input voltage levels are compatible with standard CMOS levels.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL ICs
- Supply voltage range: 2.0 to 3.2 V
- Low input current: 1.0 μ A; 0.1 μ A at T = 25 °C
- Output current 8 mA
- Latch current value: not less 150 mA at T = 125 °C
- ESD acceptable values: not less than 2000 V as per HBM and not less 200 V as per MM
-



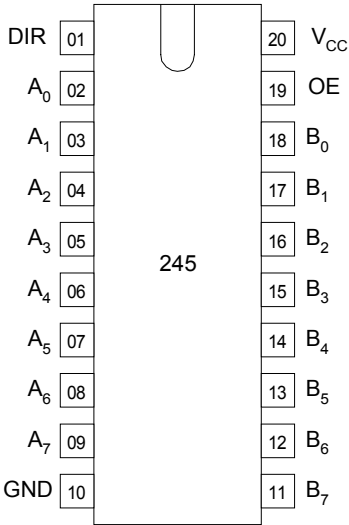
ORDERING INFORMATION
 IN74LV245N Plastic DIP
 IN74LV245D SOIC
 T_A = -40° to 125° C
 for all packages

BLOCK DIAGRAM



Pin 20 = V_{CC}
 Pin 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Inputs/Outputs	
$\overline{\text{OE}}$	DIR	A	B
L	L	A=B	input
L	H	input	B=A
H	X	Z	Z

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 to +5.0	V
I_{IK}^{*1}	Input diode current	± 20	mA
I_{OK}^{*2}	Output diode current	± 50	mA
I_O^{*3}	Output source or sink current	± 35	mA
I_{CC}	V_{CC} current	± 70	mA
I_{GND}	GND current	± 70	mA
P_D	Power dissipation per package: Plastic DIP ^{*4} SOIC ^{*4}	750 500	mW
Tstg	Storage temperature range	-65 to +150	°C

* In absolute maximum ratings modes functioning is not guaranteed. Upon lifting the absolute maximum ratings functioning is guaranteed at the recommended operating conditions.

^{*1} Provided $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$.

^{*2} Provided $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$.

^{*3} Provided $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$.

^{*4} When operating in the temperature range of 70°C to 125°C power dissipation value decreases:
- for Plastic DIP by 12 mW/°C
- for SOIC by 8 mW/°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	1.2	3.6	V
V_{IN}	Input voltage	0	V_{CC}	V
V_{OUT}	Output voltage	0	V_{CC}	V
T_A	Operating ambient temperature range. For all package types	-40	125	°C
t_{LH}, t_{HL}	Input rise and fall times $V_{CC} = 1.2\text{ V}$ $V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 3.6\text{ V}$	0	1000 700 500 400	ns

DC CHARACTERISTICS

Symbol	Parameter	Test conditions	V _{CC} , V	Limits						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V _{IH}	HIGH level input voltage	V _O = V _{CC} -0.1 V	1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V _{IL}	LOW level output voltage	V _O = 0.1 V	1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V _{OH}	HIGH level output voltage	V _I = V _{IH} or V _{IL} I _O = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
		V _I = V _{IH} or V _{IL} I _O = -8 mA	3.0	2.48	-	2.34	-	2.20	-	V
V _{OL}	LOW level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.09	-	0.09	
		V _I = V _{IH} or V _{IL} I _O = 8 mA	3.0	-	0.33	-	0.4	-	0.5	V
I _I	Input current	V _I = V _{CC} or 0 V	3.6	-	±0.1	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state current	3-state outputs V _I = V _{IL} or V _{IH} V _O = V _{CC} or 0 V	3.6	-	±0.5	-	±5	-	±10	μA
I _{CC}	Supply current	V _I = V _{CC} or 0 V I _O = 0 μA	3.6	-	8.0	-	80	-	160	μA

AC CHARACTERISTICS($C_L=50$ pF, $t_{LH} = t_{HL} = 6.0$ ns)

Symbol	Parameter	Test conditions	V_{CC} , V	Limits						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL} , t_{PLH} from An to Bn, from Bn to An	Propagation delay	Figure 1	1.2	-	100	-	125	-	140	ns
			2.0	-	23	-	28	-	34	
			3.0	-	14	-	18	-	21	
t_{PHZ} t_{PLZ} from OE, DIR to An, Bn	3-state output enable time	Figure 2	1.2	-	120	-	140	-	160	ns
			2.0	-	30	-	37	-	43	
			3.0	-	20	-	24	-	28	
t_{PZH} t_{PZL} from OE to An, Bn	3-state output disable time	Figure 2	1.2	-	120	-	140	-	160	ns
			2.0	-	28	-	35	-	43	
			3.0	-	17	-	21	-	26	
t_{THL} , t_{TLH}	HIGH-to-LOW and LOW-to HIGH transition time	Figure 1	1.2	-	60	-	75	-	90	ns
			2.0	-	15	-	20	-	24	
			3.0	-	10	-	13	-	15	
C_I	Input capacitance	For inputs 01,19	3.0	-	7	-	-	-	-	pF
$C_{I/O}$	Input capacitance	For inputs/ outputs 02-09, 11-18	3.0	-	20	-	-	-	-	
C_{PD}	Power dissipation capacitance (per one channel)	$V_I = 0$ V or V_{CC}	3.0	-	50	-	-	-	-	

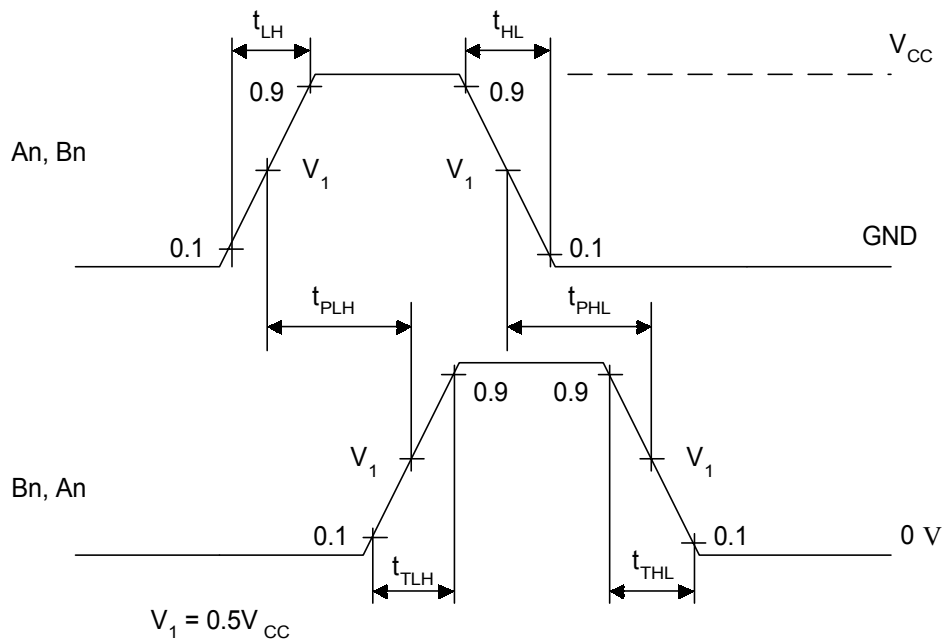


Figure 1 -Time diagram of AC parameters control t_{PLH} , t_{PHL} .

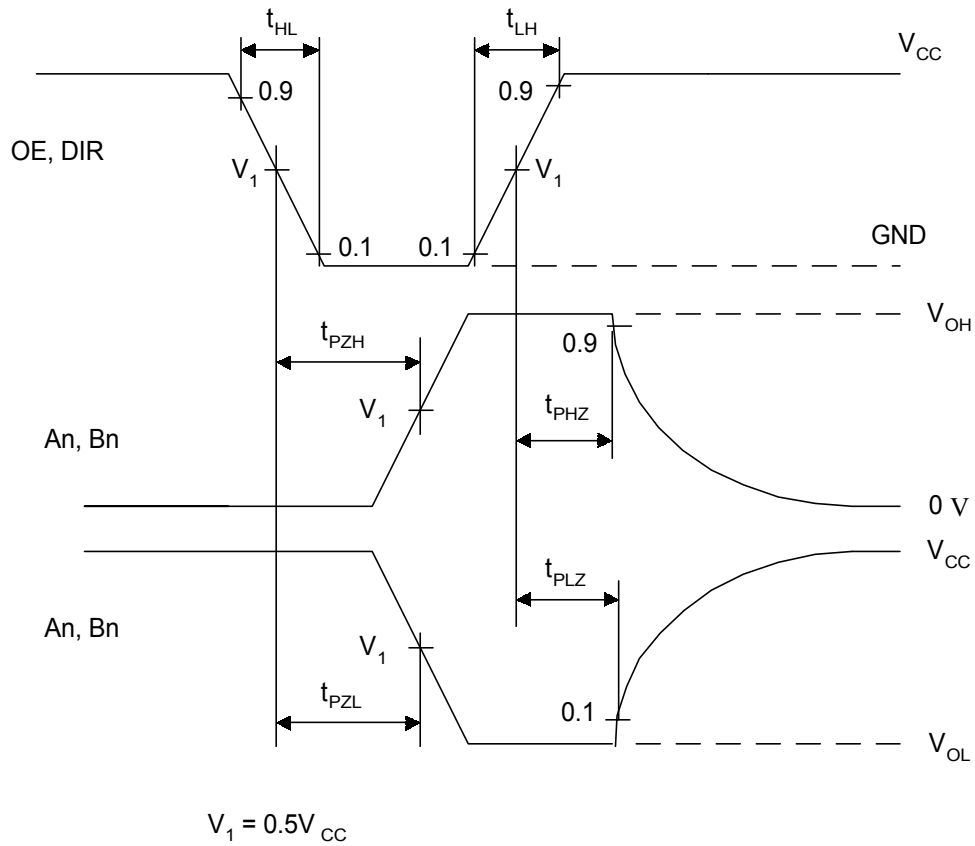
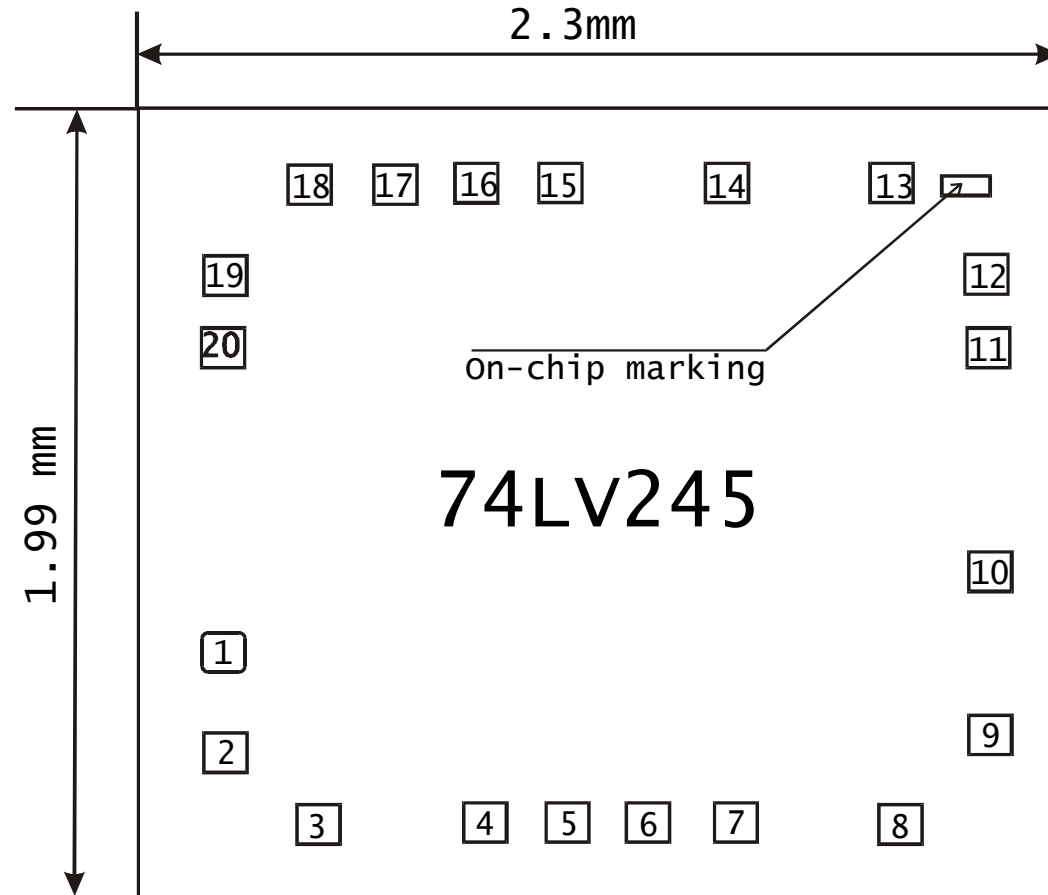


Figure 2 - Time diagram of t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} . AC parameters control

Drawing of the chip



Pads allocation Table

Pad number	coordinates (counted from lower left corner), mm		Pad size, mm
	X	Y	
01	0.140	0.573	0.108 x 0.108
02	0.140	0.315	0.108 x 0.108
03	0.370	0.140	0.108 x 0.108
04	0.790	0.140	0.108 x 0.108
05	1.000	0.140	0.108 x 0.108
06	1.200	0.140	0.108 x 0.108
07	1.417	0.140	0.108 x 0.108
08	1.833	0.140	0.108 x 0.108
09	2.060	0.354	0.108 x 0.108
10	2.060	0.760	0.108 x 0.108
11	2.060	1.340	0.108 x 0.108
12	2.060	1.520	0.108 x 0.108
13	1.833	1.750	0.108 x 0.108
14	1.415	1.750	0.108 x 0.108
15	1.000	1.750	0.108 x 0.108
16	0.790	1.750	0.108 x 0.108
17	0.580	1.750	0.108 x 0.108
18	0.370	1.750	0.108 x 0.108
19	0.140	1.544	0.108 x 0.108
20	0.140	1.375	0.108 x 0.108